Mater. Res. Soc. Symp. Proc. Vol. 870E © 2005 Materials Research Society H2.7.1

Nanocrystalline Silicon Thin Film Transistors on Optically Clear Polymer Foil Substrates

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Abstract

We have fabricated TFTs of nanocrystalline silicon (nc-Si) at 150°C on clear polymer substrates (coefficients of thermal expansion, α~45 to 55ppm/K), on Kapton® 200E (α=17ppm/K), and on Corning 1737 glass (α=3ppm/K) for comparison. Because thermally stable polymers, such as Kapton® 200E polyimide, have glass transition temperatures as high as 325°C, they are candidates for direct substitution of display glass. The stresses developed in the substrate and device layers, due to α, are reduced by decreasing the thickness of the active layers, by cutting the layers into islands separated by exposed substrate, and by designing stresses, via plasma conditions, into the SiN_x passivating layers. By using these three techniques we have made nc-Si TFTs on high T_g, and high α, clear polymer foils with electron mobilities of up to 18cm^2/Vs. When integrated with bottom-emitting organic light emitting diodes, such devices will allow for a 10x reduction in pixel TFT areas, compared to TFTs of amorphous silicon.

Introduction

Flexible displays are the next technology generation for flat-panel displays. Therefore interest is growing in building high-performance TFT backplanes on flexible substrates. Flexible polymer foils are attractive for large area displays, because they are lightweight and allow for the possibility of roll-able displays. Ideally, a flexible backplane will be made using fabrication processes that already have been developed for glass with only minor changes. Nanocrystalline silicon (nc-Si) TFTs are capable of both n- and p-type operation, have at least ten times the n-channel ON current of amorphous silicon (a-Si) TFTs, and can be plasma deposited at temperatures upwards of 150°C. This makes them CMOS capable and good candidates for pixel circuits in active-matrix organic light emitting diode (AMOLED) displays. There is growing interest in AMOLED displays because active-matrix addressing allows for high pixel count and long OLED life [1]. For AMOLED displays with TFT pixel drivers and bottom-emitting OLEDs mounted on the same plane, the substrate must be optically clear. When polymer substrates are heated that high though, the thermal expansion mismatch between silicon TFT materials and the polymer substrate becomes a challenge. The effects of mismatch become more pronounced as process temperature is increased and this mismatch, and built-in stresses in the device films, can combine to fracture TFT structures during processing.

Today pixel circuits for AMOLED displays on polymer substrates are conceived with hydrogenated amorphous-silicon thin film transistors (a-Si TFTs) [2,3]. a-Si TFTs have been fabricated at temperature as low as ~100ºC [4] and have been produced on clear polymers such as poly-ethylene terephthalate (PET) [5]. However since PET has a glass transition temperature (T_g) <100ºC, the maximum process temperature is limited and the TFTs exhibit low electron mobilities of up to 0.12cm^2/Vs [5]. Hydrogenated nanocrystalline silicon (nc-Si) TFTs, on the other hand, can be fabricated at temperatures as low as 150ºC, exhibit ten times the ON current as a-Si TFTs, and are build using similar techniques to those of a-Si on glass. nc-Si TFTs on glass exhibit hole and electron mobilities of 0.35cm^2/Vs and 40cm^2/Vs respectively [6]. The p-

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channel operation promises CMOS integration and all its advantages vis à vis power consumption and system-on-panel design [6]. In fact CMOS inverters of nc-Si with hole and electron mobilites of $0.35cm^2/Vs$ and $30cm^2/Vs$ respectively, have been fabricated on flexible, DuPont™ Kapton® 200E polymer foil [7]. Polymers such as Kapton® 200E have a T_g high enough for quality TFT deposition, but are absorbing in the blue and therefore cannot be used with bottom-emitting OLEDs. Also nc-Si TFTs are currently limited by the poor quality of the SiO_2 gate dielectric made at low temperatures. The SiO_2 is a strong motivation for processing at "glass temperatures." This temperature requirement rules out PET, for its T_g, and rules out Kapton ® 200E, for its color. Hence we are working with experimental clear polymers (CP), which have a T_g~325°C. This group of polymers also has a large α~45-50x10^{-6}/K.

The high α of these CP substrates introduces a new challenge to TFT fabrication on flexible polymer substrates. When the α of the substrate is much greater than that of the device films ($\alpha_{\text{device films}}$~2-3ppm/K) a high thermal mismatch strain (ε_{TH}) is introduced into the structure according to:

$$\varepsilon_{TH} \cong (\alpha_{substrate} - \alpha_{film}) \cdot (T_{room} - T_{depositiom}) \; [8]. \qquad (1)$$

This formulation assumes that the structure is free of strain at growth and the strain develops as the sample is cooled from process temperature down to room temperature. For all our films a deposition temperature of 150ºC is used to keep ε_{TH} low while allowing for reasonable TFT characteristics. As the sample cools the polymer substrate contracts more than the device thin films. This causes high compressive stresses (~1GPa) in the thin films and high tensile stresses in the polymer substrate. The nc-Si device films can only be strained to a critical value, beyond which the films and substrate crack, as shown in Figure 1. It is know that for a-Si thin films compressive failure occur at strains of 2% [9], whereas for nc-Si the number is unknown. By using various stress compensation techniques, we have fabricated n-channel nc-Si TFTs on the CP. Figure 2 displays a batch of these devices.

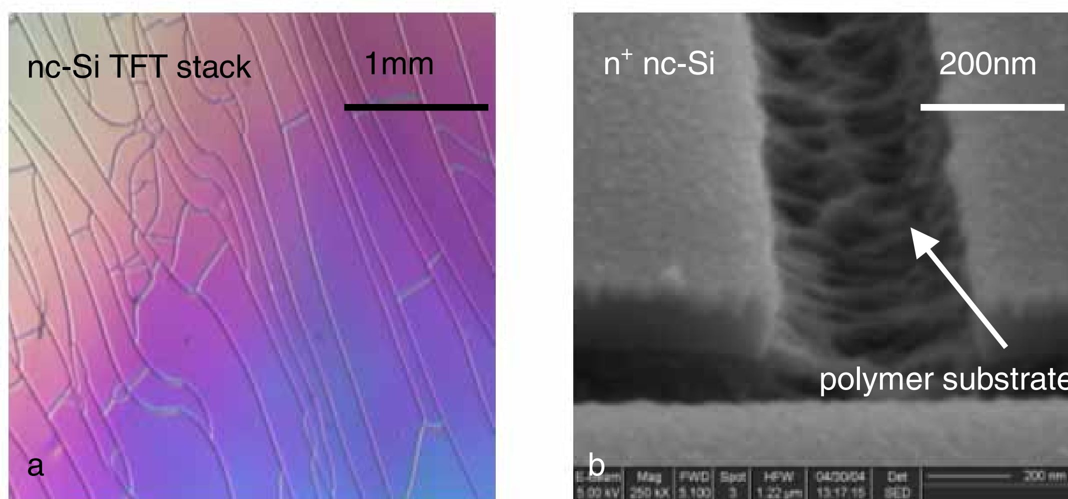

Figure 1. a) Optical image of a cracked TFT stack, on a clear polymer substrate with a large α. b) The micrograph, of the same layers, shows that the cracks penetrate into the polymer substrate.

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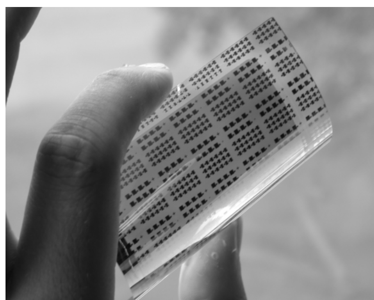

Figure 2. A batch of n-channel nc-Si TFTs on CP substrate over a $25cm^2$ area.

Techniques for Stress Compensation and Reduction

Since $\alpha_{CP} >> \alpha_{film}$, as the substrate cools from the deposition temperature down to room temperature the substrate contracts more than the films. This places a compressive strain on the films and a tensile strain on the substrate. The total strain in the thin films is: [8]

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{TH} + \varepsilon_{CH}, \tag{2}$$

where ε_0 is the built-in strain, ε_{TH} is the strain due to $\Delta\alpha$, and ε_{CH} is the strain due to moisture absorption by the polymer substrate. Since $\Delta\alpha$ is large for the CP, we observe that the thermal strain dominates. We employ three techniques to help reduce stress and build crack-free structures.

The first technique we use is to decrease the thickness of the device layers. The stress in the thin film is dependent on the temperature excursion during deposition (ΔT), $\Delta\alpha$, and thickness of the film [10]. For a *rigid* thin film on a *rigid* substrate, and in the absence of built-in stress, the total stress is: [10]

$$\sigma_f \propto (\alpha_{substrate} - \alpha_{film}) \cdot (T_{room} - T_{deposition}) \cdot \sqrt{d_{film}}\ , \tag{3}$$

where d_{film} is the thin film thickness. The exact relation for compliant substrates like CP and Kapton ® 200E is yet unknown, but it is known that films under stress fracture more easily as their thicknesses are increased. Therefore, we minimize the device film thicknesses until the electrical performance of the TFT is affected.

By building the TFTs on SiN_x islands the compliant substrate is allowed to strain beneath and between the rigid SiN_x islands. Therefore the large average stress across the substrate is reduced [11]. This in turn reduces the probability of crack formation. The concept of island patterning to reduce the effects of the stress has been used on devices built on externally deformed substrates [11].

The final method makes use of controlled stress in the SiN_x passivation layers. These layers serve to chemically isolate the substrate and act as adhesion promoters for the device layers. The SiN_x can be deposited with a range of built-in strains depending on the plasma power density [8]. The built-in strain is used to partially compensate the thermal strain, decreasing the

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total stress according to equation 2. We use a low plasma power density to deposit a tensile SiN_x layer on the front-side of the substrate. This serves to compensate part of the compressive stress in the device films due to the $\Delta\alpha$, according to equation 1.

nc-Si TFT Process

We made nc-Si TFTs at 150°C on a clear polymer (α = 45 to 55ppm/K), on Kapton® 200E (α = 17ppm/K), and on Corning 1737 glass (α = 3ppm/K) for comparison. The n-channel nc-Si TFTs were built in a staggered top gate, bottom source drain structure, Figure 3. No passivation layers or SiN_x islands were used on the glass substrate.

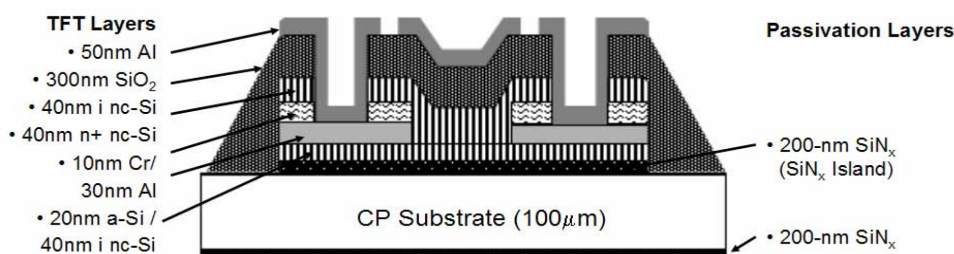

Figure 3. Cross-section schematic of the n^+ nc-Si TFT built onto a SiN_x island.

200nm of SiN_x is deposited by PECVD at 150°C on the backside and then on the front-side of the substrate. This is followed by an i nc-Si seed layer. The seed layer is used to introduce nucleation sites and produce good crystallinity in very thin channel layers [7]. It is deposited by VHF-PECVD from H_2 and SiH_4. Dichlorosilane (DCS) is included to compensate native oxygen donors and lower the conductivity and thereby the TFT OFF current [12]. The source / drain metal is deposited by thermal evaporation, 30nm of Al and 10nm of Cr on the CP substrate. 50nm Cr is substituted on the Kapton® 200E and glass substrates. Etching down to the substrate defines the SiN_x islands. Next the n^+ nc-Si, source / drain contact layer is deposited by VHF-PECVD using PH_3 dopant gas. Patterning the source / drain exposes the seed layer upon which the channel layer will be deposited. The i nc-Si channel layer is deposited by VHF-PECVD from H_2, SiH_4, and DCS. This is immediately followed by a 150ºC SiO_2 deposited by PECVD from a He diluted N_2O and SiH_4 source [13]. Next source / drain contact holes are patterned and 50nm Al is thermally evaporated on the CP sample, whereas 200nm Al is used on the Kapton® 200E and glass samples. Finally the top Al is patterned to define the gate and the devices are complete. Table 1 displays the layer thicknesses used on the three different substrates.

Table 1. Thicknesses in nm of the nc-Si TFT layers on the three types of substrate.

TFT Layers	Material	Corning 1737 Glass	Kapton® 200E	CP
Passivation	backside SiN_x	-	200	200
Passivation	frontside SiN_x	-	200	200
Seed	i nc-Si	60	60	50
S/D contact	Al	-	-	30
S/D contact	Cr	50	50	10
S/D doped	n^+ nc-Si	50	50	40
Channel	i nc-Si	50	50	40
Gate dielectric	SiO_2	300	300	300
Gate metal	Al	200	200	50

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Results

The transfer characteristics of the nc-Si TFTs are evaluated using a HP4155A parameter analyzer. The devices measured have the following dimensions W=90µm (CP), W=180µm (Kapton® 200E and glass) and L=45µm. An SiO_2 dielectric constant of 3.7 was measured by C-V at 1MHz on Al/SiO_2/n-type Si wafer. Figure 4 displays the drain current (I_{DS}) versus the gate-source voltage (V_{GS}) for a drain-source voltage (V_{DS}) of 10V, for a nc-Si TFT on glass and on Kapton® 200E. The transfer characteristics for the n-channel nc-Si TFT on the CP were measured in a similar manner, and are displayed in Figure 4.

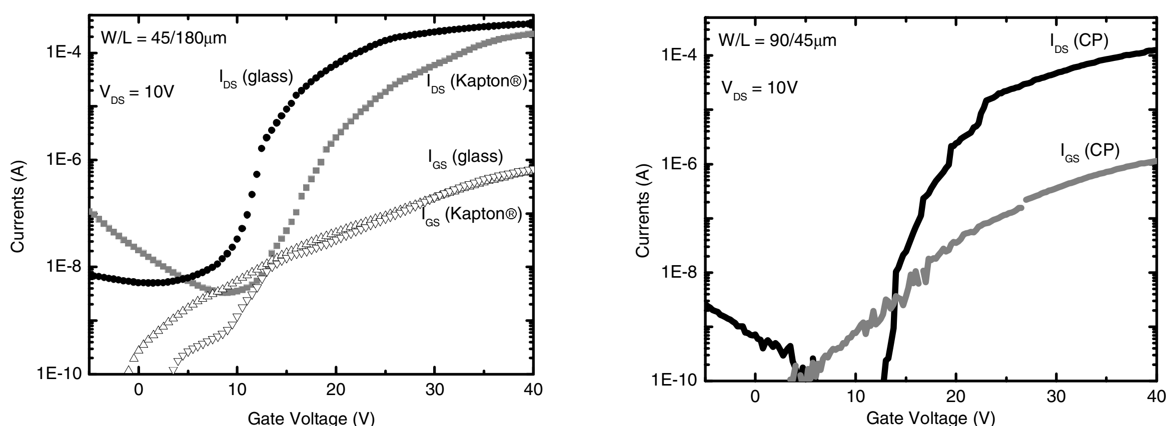

Figure 4. Transfer characteristics for n-channel nc-Si TFTs on glass and Kapton® 200E (left). Transfer characteristics for n-channel nc-Si TFTs on CP (right).

Table 2. Results for n-channel nc-Si TFTs fabricated on glass, Kapton® 200E, and CP.

Substrate	α (ppm/K)	I_{ON}/I_{OFF}	$\mu_{h\text{-}sat}$ (cm²/Vs)	$\mu_{e\text{-}sat}$ (cm²/Vs)
Corning 1737 Glass	2.5	10^5	0.35	40
Kapton ® 200E	17	10^5	0.35	30
CP	45-55	10^5	-	18

Table 2 shows the results for the devices on the 3 types of substrate. All the TFTs have an I_{ON}/I_{OFF} ~10^5. The nc-Si TFT on the glass has slightly lower V_T and a higher μ_e than that of the nc-Si TFT on Kapton® 200E. This is probably due to fluctuations in chamber conditions rather than a fundamental difference in the devices from a substrate effect. The TFT on the CP exhibits characteristics similar those on the glass and Kapton® 200E. It has a V_T~12V and μ_e ~18cm^2/Vs. The lower mobility may be due to the fact that thin device films were used on CP, see Table 1. The thin S/D metal may cause an increase in the contact resistance. The gate leakage, though still large, has been reduced from previous results by use of He dilution during deposition, but further improvements are necessary [13]. A higher quality SiO_2 gate dielectric and improvements in the SiO_2 / i nc-Si interface must be made to reduce gate leakage current, V_T, and V_T drift.

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Conclusions

We have produced nc-Si TFTs on a clear polymer substrate after adjusting the process to deal with the large α of the substrate. By building the devices on SiN_x islands and by carefully controlling the plasma conditions we have been able to reduce the effects of stress and prevent cracking. The TFTs on clear polymer perform similarly to those on the glass and Kapton® 200E. Such TFTs may become useful in AMOLED displays where both TFTs and bottom-emitting OLEDs are fabricated on the same plane and where high fill factors and drive currents are necessary.

Acknowledgments

We would like to thank The DuPont Company and The New Jersey Commission on Science and Technology for research support, along with the Princeton Plasma Physics Laboratory (PPPL) for a PPST Fellowship.

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