transport, then air-annealed at different temperatures transform the bound exciton emission. Specifically, the I_4 intensity decreases significantly as annealing temperature increases. Conversely, this I_4 emission increases dramatically with hydrogenation, regaining almost all the intensity lost due to anneali ng. To detect Hall variations, given the small - tens of nanometers - SIMS-measured penetration depth of the H-plasma ions, we employed two approaches: (1) reducing the initial bulk carrier concentration by compensating via Li in-diffusion, (2) using an epitaxial thin film of ZnO on sapphire to minimize the thickness of the conductive layer relative to the diffusion depth of hydrogen species. Li doping removed the I_4 line and subsequent hydrogenation reintroduced broader emission in the I_4 region. Li doping removed the initial $>10^{17}$ cm^{-3} carrier concentration whereas hydrogenation restored detection of the conductivity and Hall coefficient. For a hydrogenated thin film grown on sapphire by molecular beam epitaxy, we observed an order of magnitude increase from ~ $2x10^{17}$ to $2x10^{18}$ cm^{-3} in the number of donors created by hydrogenation. Thus remote hydrogen plasma treatment can control ZnO transport and excitonic properties. Fu rthermore, it identifies the shallow donor with a hydrogen-related impurity.1. C.G. Van de Walle, Phys. Rev. Lett. v. 85, 1012 (2000).

2:30 PM

I4, Microstructure and Nucleation Behavior of Heteroepitaxial GaN Films Grown on Mesa-Patterned 4H-SiC Substrates: *Nabil D. Bassim*[1]; J. A. Powell[4]; Mark E. Twigg[1]; Charles R. Eddy[1]; Richard L. Henry[1]; Ronald T. Holm[1]; James C. Culbertson[1]; Philip G. Neudeck[2]; A. J. Trunek[3]; [1]Naval Research Laboratory, Elect. Sci. & Tech., Code 6812, 4555 Overlook Ave. SW, Washington, DC 20375 USA; [2]NASA Glenn Research Center, Cleveland, OH USA; [3]OAI, Cleveland, OH USA; [4]Sest, Inc., Cleveland, OH USA

Thin heteroeptiaxial GaN films grown on (0001) 4H-SiC mesa surfaces with and without atomic scale steps were studied by transmission electron microscopy, atomic force microscopy, and polarized light microscopy. Analysis of a mesa that was completely free of atomic-scale surface steps prior to III-N film deposition showed that these GaN layers (grown with a HT AlN nucleation layer) had a wide variation in island height (1 µm to 3 µm) and included the presence of pit-like defects on the film surface. This sample had a low dislocation density (5 x 108/cm2) as compared to conventionally-grown samples on unpatterned (0001) on-axis 4H-SiC (2 x 109/cm2), coupled with a 3-5 times increase in grain size. Comparison of GaN films grown simultaneously on step-free and stepped 4H-SiC mesa regions showed that the presence of surface steps reduced the overall grain size of the film from 7-10 µm to a grain size of about 2 to 3 µm. Because GaN films grow via a Volmer-Weber mechanism, a decrease in the number of substrate steps acting as heterogeneous nucleation sites may allow the growth of large GaN islands before coalescence, thus reducing the number of threading dislocations. An analysis of the effects of cleaning of the 4H-SiC wafers prior to growth on the nucleation behavior of the AlN film, as well as the effect of growth interrupts during deposition will be discussed. The development of a technique to grow large-grained films with fewer extended defects is promising for the microstructural design of unique GaN device structures grown on 4H-SiC substrates.

2:50 PM Student

I5, Drift Dominated AlGaAs Solar Cells for High Temperature Application: *Yanning Sun*[1]; Aristo Yulius[1]; Michael P. Young[1]; Eric S. Harmon[2]; Jerry M. Woodall[1]; [1]Yale University, Elect. Engrg., PO Box 208284, New Haven, CT 06520 USA; [2]LightSpin Technologies, Inc., 314 Main St., Norfolk, MA 02056 USA

We investigate an AlGaAs (Eg = 1.7 eV) solar cell grown on GaAs substrate for high temperature applications by applying a drift dominated design. This unique design can build an internal electric field throughout the active region by varying the doping concentration, which allows us to collect photo-generated carriers by drift due to this electrical field instead of diffusion associated with conventional p-n junction devices. Since MBE grown AlGaAs is known to have non-radiative traps, this drift dominated device design is expected to be more efficient in transporting minority carriers. We have already demonstrated this concept on highly defected cells by the quantum efficiency measurement on drift dominated InP photodiodes grown on GaP substrate. The results show that even with 8% lattice mismatch, we've still achieved excellent spectral response especially in the UV-visible region where we have higher than 75% internal quantum efficiency and only about 10% degradation from InP on InP substrate devices. The structure of our drift dominated AlGaAs solar cell can be described as follows: we vary the beryllium doping concentration from $10^{15}cm^{-3}$ at the junction to $10^{20}cm^{-3}$ at the surface to achieve drift fields of 5000-10000 volts/cm in the 500 nm p-type top layer. After that we have 500nm intrinsic AlGaAs layer which is fully depleted and provide another larger than 10^4 volts/cm drift field. Electrons generated in these two top layers will transport with their saturation drift velocity (~10^7 cm/s) and can get through these layers in less than picoseconds. The 200nm n-type AlGaAs region is right under the intrinsic region and the doping concentration is also graded from $10^{16}cm^{-3}$ at the junction to $5*10^{18}cm^{-3}$. Therefore all together we have drift fields in the top 1200nm region as the active region of the device. We also have 5nm heavily p-doped GaAs layer on the top for good ohmic contact. AlGaAs characterization structures and cells have been fabricated and tested. We used electrochemical C-V profiler (ECV) to profile the carrier concentration as a function of sample depth. The profile confirms that the carrier concentration has been graded as expected. The dark current-voltage characteristics have been measured. The idea factor extracted from the J-V curve in the forward direction is about 1.78, and reverse saturation current is very low, about $0.2nA/cm^2$. The spectral response on the AlGaAs drift cell shows 40-45% internal quantum efficiency at green and orange and 20-35% at longer wavelengths. However, the response at blue-UV range is very low, which we currently think is due to the carriers generated by UV-blue photon absorption recombining via interstitial Be traps in the heavily p-doped ($10^{20}cm^{-3}$) region near the AlGaAs surface. Details of the high-energy-photon loss mechanism will be presented at the conference.

3:10 PM Break

Session J: Si-Based Heterojunctions and Strained Si: Growth, Characterization and Applications

Wednesday PM Room: 141
June 23, 2004 Location: DeBartolo Hall

Session Chairs: Sarah H. Olsen, University of Newcastle-upon-Tyne, Newcastle NE1 7RU UK; Doug Webb, ATMI, Meza, AZ 85210 USA

3:30 PM

J1, High Electron Mobility Transistor Structures on Sapphire Substrates Using CMOS Compatible Processing Techniques: *Carl H. Mueller*[1]; Samuel A. Alterovitz[2]; Edward T. Croke[3]; George E. Ponchak[4]; [1]Analex Corporation, 21000 Brookpark Rd., MS 7-1, Brookpark, OH 44135 USA; [2]NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA; [3]HRL Laboratories, 3011 Malibu Canyon Rd., RL63, Malibu, CA 90265 USA; [4]NASA Glenn Research Center, 21000 Brookpark Rd., MS 54-5, Cleveland, OH 44135 USA

System-on-a-chip (SOC) processes are under intense development for high-speed, high frequency transceiver circuitry. As frequencies, data rates, and circuit complexity increases, the need for substrates that enable high-speed analog operation, low-power digital circuitry, and excellent isolation between devices becomes increasingly critical. SiGe/Si modulation doped field effect transistors (MODFETs) with high carrier mobilities are currently under development to meet the active RF device needs. However, as the substrate normally used is Si, the low-to-modest substrate resistivity causes large losses in the passive elements required for a complete high frequency circuits. These losses are projected to become increasingly troublesome as device frequencies progress to the Ku-band (12 - 18 GHz) and beyond. Relative to Si, the high electrical resistivity of sapphire enables superior performance in passive device such as inductors, and less cross-talk between devices. Sapphire is an excellent substrate for high frequency SOC designs because it supports excellent both active and passive RF device performance, as well as

low-power digital operations. We are developing high electron mobility SiGe/Si transistor structures on r-plane sapphire, using either in-situ grown n-MODFET structures or ion-implanted high electron mobility transistor (HEMT) structures. Advantages of the MODFET structures include high electron mobilities at all temperatures (relative to ion-implanted HEMT structures), with mobility continuously improving to cryogenic temperatures. We have measured electron mobilities over 1,200 and 13,000 cm^2/V-sec at room temperature and 0.25 K, respectively in MODFET structures. The electron carrier densities were 1.6 and $1.33x10^{12}$ cm^{-2} at room and liquid helium temperature, respectively, denoting excellent carrier confinement. Shubnikov de-Haas oscillations were observed, thus confirming the 2D nature of the carriers. Conversely, HEMT structures using ion-implanted processing are appealing because they are compatible with existing CMOS processing, and thus would be attractive for complex, highly integrated circuitry. Using this technique, we have observed electron mobilities as high as 900 cm^2/V-sec at room temperature at a carrier density of $1.3x10^{12}$ cm^{-2}. The temperature dependence of mobility for both the MODFET and HEMT structures provides insights into the mechanisms that allow for enhanced electron mobility as well as the processes that limit mobility, and will be presented. Using the MBE Sb doped structures, transistors with varying source-to-drain distances and gate lengths (1 - 5 µm) were fabricated. Although the design is not optimized, the initial results are promising. The I-V behavior indicated the saturated drain current region extended over a wide drain voltage range, with knee voltages of approximately and 0.5 V and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation.

3:50 PM Student

J2, Temperature Sensitivity of DC Operation of Sub-Micron Strained-Si MOSFETs: *Valerio Gaspari*[1]; *Kristel Fobelets*[1]; Sarah H. Olsen[2]; Jesus Enrique Velazquez-Perez[3]; Anthony G. O'Neill[2]; Jing Zhang[4]; [1]Imperial College London, Elect. & Elect. Engrg., MailStop EEE-OSD, Exhibition Rd., London, England SW7 2BT UK; [2]University of Newcastle upon Tyne, Elect. Engrg., Newcastle NE1 7RU UK; [3]Universidad de Salamanca, Dept. de Física Aplicada, Edificio Trilingue, P.za de la Merced s/n, Salamanca E-37008 Spain; [4]Imperial College London, Physics, Exhibition Rd., London SW7 2AZ UK

The DC performance of sub-micrometer Strained-Si n-type surface channel MOSFETs has been investigated for operating temperatures ranging from 10 K to 300 K. The strained-Si layer that constitutes the active region of the devices was grown on strain-relaxed constant-composition SiGe buffer layer, preceded by a linearly graded SiGe virtual substrate. The final Ge concentration in the devices presented in this study ranges from 10% to 30%. Si control devices were produced as performance references. Devices were fabricated using industry-standard CMOS processing techniques, with a reduced thermal budget to preserve the integrity of the layer structure. The low-field maximum transconductance of strained-Si devices is found to be higher that that of the corresponding Si control device for all temperatures and all virtual substrate Ge concentrations greater than 10%, indicating an increased value of mobility in the strained Si layer. The largest relative performance gain (with respect to the Si control) is observed in the device with a 20% Ge virtual substrate. The relative transconductance increase in strained-Si devices decreases with decreasing temperature down to approximately T = 100 K, below which it remains constant. This seems to indicate that the importance for performance increase of reduced inter-valley phonon scattering in strained Si decreases as the relative importance of phonon scattering processes as a mobility-limiting factor decreases. The remaining amount of performance gain below T = 100 K is attributed to reduced in-plane effective mass and Coulomb scattering in strained Si in comparison with the Si control device. The sub-threshold slope of strained-Si devices is found to be approximately insensitive to virtual substrate Ge concentration, up to a Ge content of 20%. Higher concentrations of Ge in the virtual substrate were observed to result in an increase in the minimum sub-threshold slope over the entire temperature range. The sub-threshold slope in high-Ge-content devices was limited by relatively large off-state currents, which we attribute to the presence of leakage paths through the virtual substrate.

4:10 PM Student

J3, MOS Capacitors on Epitaxial Ge/$Si_{1-x}Ge_x$ with High-k Dielectrics: *Sachin V. Joshi*[1]; Xiao Chen[1]; David Q. Kelly[1]; Tat Ngai[1]; James Chen[1]; Sanjay K. Banerjee[1]; [1]University of Texas, Microelect. Rsch. Ctr., Bldg. 160, 10100 Burnet Rd., Austin, TX 78758 USA

High K dielectrics on Ge can reduce gate leakage while taking advantage of the high mobility of Ge. However Ge substrates have poor mechanical and thermal properties, high cost, and process complexity. Epitaxial Ge layers, of about inversion layer thickness could confine electrons or holes under a gate bias enabling high mobility MOSFETs. Ge/$Si_{1-x}Ge_x$ MOS capacitors were fabricated on p-type silicon substrates. ≈60A° Ge or $Si_{1-x}Ge_x$ (x=0.9) epitaxial layers were deposited by remote plasma-assisted chemical vapor deposition (RPCVD) at ≈300°C. ≈50A° RPCVD HfO_2 was then deposited in another chamber without breaking the vacuum, at ≈250°C using hafnium t-butoxide precursor. Subsequently post-deposition annealing, TaN sputtering, capacitor patterning and etch, backside metallization and sintering were done, at or below 400°C. MOS capacitors directly on Si were fabricated using the same procedure. Physical and electrical characteristics were investigated. Using X Ray Diffraction (XRD) and XRD simulation we confirmed that ≈50A° Ge epitaxial layer with over 90% compressive strain on Si substrate is grown. Owing to the low temperature meta-stable RPCVD growth, ≈65A° epitaxial Ge layer is achieved, well beyond the equilibrium Critical Layer Thickness (CLT (<10A°)) as seen from cross-sectional High Resolution Transmission Electron Microscopy (HRTEM). The RMS roughness for Ge and $Si_{1-x}Ge_x$ epitaxial layers is ≈1.5A°, indicating a smooth surface for HfO_2 growth. The interfacial layer is ≈ 10A° on Si, but less than 5 A° on Ge layer probably because Ge oxides are volatile at high temperature and high vacuum. Low-frequency curves were simulated using the NCSU CVC program from the measured high-frequency capacitance with QM correction. EOT of HfO_2 on Ge is determined to be 9.7A°, half of that on Si (20A°), due to the lower interfacial thickness between HfO_2 and Ge. The interface state density (D_{it}) in HfO_2 /Si stack is $\approx 10^{11}/cm^2/eV$. The $D_{it's}$ in HfO_2 /Ge/Si and HfO_2 / Si_{1-x} Ge_x /Si stacks are of the order of $10^{12}/cm^2/eV$, probably due to the less stable interface between HfO_2 and Ge/Si_{1-x} Ge_x. Leakage currents densities of these HfO_2 films at -1V are $\approx 10^{-2}$ A/cm^2 with reasonably well behaved J-V characteristics. These values are comparable with recent values with similar EOTs for gate stacks of HfO_2 on Si, and are 3 orders of magnitude lower than those reported for HfO_2 on Ge for similar EOTs. We attribute this leakage reduction to the epitaxial Ge layer and high-k dielectric layer being grown without breaking the vacuum, thus avoiding interfacial contamination. Thus, low temperature MOS capacitor stacks with strained epitaxial Ge or Si_{1-x} Ge_x (x=0.9) layer directly on Si substrates, and with HfO_2 (EOT=9.7A°) as dielectric, both using RPCVD is demonstrated. Well behaved MOS capacitors show that RPCVD process is a promising technique for low thermal budget, high performance applications.

4:30 PM Student

J4, Uniaxially-Tensile Strained Ultra-Thin Silicon-On-Insulator with Up to 1.0% Strain: *R. L. Peterson*[1]; H. Yin[1]; K. D. Hobart[2]; T. S. Duffy[3]; J. C. Sturm[1]; [1]Princeton University, Dept. of Elect. Engrg., E-Quad, Olden St., Princeton, NJ 08544 USA; [2]Naval Research Laboratory, Washington, DC 20375 USA; [3]Princeton University, Dept. of Geoscis., Guyot Hall, Princeton, NJ 08544 USA

Low uniaxial tensile strain of <0.04% has been recently reported to increase both PMOS and NMOS silicon-on-insulator (SOI) effective mobilities by ~15%,[1] much more than that expected by comparable biaxial strain.[2] We have demonstrated uniaxial tensile strain in SOI of 0.6% using stress balance of a SiGe/Si bi-layer structure.[3] In this study, record uniaxial strain of 1.0% has been achieved by thinning the Si film in the bi-layer. This increased strain level should allow for even greater device performance enhancement. SiGe and Si films are transferred to a BPSG (borophosphorosilicate glass)-coated Si wafer by a wafer bonding and Smart-Cut™ layer transfer process described previously,[4] forming 30nm $Si_{0.7}Ge_{0.3}$ / 10-25nm Si / BPSG. After transfer, the Si film remains relaxed and SiGe commensurately compressively strained. The SiGe/Si layers are patterned into islands with <100> edges. Upon high-temperature annealing BPSG viscosity decreases substantially and the SiGe expands laterally to relax its compressive strain, stretching the underlying Si film to create tensile strain. The bi-layer structure thus reaches an equilibrium state of stress balance.[5] Strain is measured by micro-Raman spectroscopy at 488 or 514nm.[6] For islands of edge length L, lateral relaxation occurs according to the time constant, $\tau \propto L^2$.[4] Small square islands result in biaxially-symmetric strain, while rectangular islands maintain their initial strain in the long dimension (here, 150µm) but

quickly expand in the short dimension (≤ 20μm), yielding uniaxial tensile Si strain. The net strain change is identical for the Si and SiGe films because of their coherent interface.[5] That the two layers move together is clearly demonstrated for 20μmx150μm islands of 30nm SiGe/25nm Si/200nm BPSG, before and after 30min at 800°C in nitrogen: $\Delta\varepsilon_{Si} \approx \Delta\varepsilon_{SiGe} = 0.75\%$. To obtain larger uniaxial Si strain we use a thinner layer of Si: 30nm SiGe/10nm Si/5.5nm SiN_x / 1μm BPSG. SiN_x is added to suppress dopant out-diffusion from BPSG.[5] After 15min at 750°C, SiGe strain in the short-dimension direction changes from 1.2% to 0.2% (i.e., from full compressive strain to almost complete relaxation) in agreement with predicted SiGe strain of 0.2% based on stress balance. The resulting uniaxial tensile strain in the underlying 10nm Si layer is directly measured to be 1.0%, again confirming a coherent SiGe/Si interface. For stress balance of the same bi-layer, uniaxial Si strain is greater than biaxial Si strain (~0.7%) due to the long island dimension constraint, which causes all the expansion to take place in the short dimension. [1]B.M. Haugerud, et. al., Journal of Applied Physics, 94, 4102 (2003) [2]S. Takagi, et. al., IEDM Digest, Washington, DC (2003), pp.57-60 [3]H. Yin, et. al., MRS Fall Meeting, Boston, MA (2003) [4]H. Yin, et. al., Journal of Applied Physics, 91, 9716 (2002) [5]H. Yin, et. al., IEDM Digest, Washington, DC (2003) [6]S.C. Jain, et. al., Physical Review B, 52, 6247 (1995).

4:50 PM Student

J5, Influence of the Si-Ge Interdiffusion in $NiSi_{1-u}Ge_u$ on Morphological Stability: *Johan Seger*[1]; Tobias Jarmar[2]; Fredric Ericson[2]; Ulf Smith[2]; Shi-Li Zhang[1]; [1]KTH, Dept. of Microelect. & Info. Tech., PO Box E229, Kista SE-164 40 Sweden; [2]Uppsala University, The Ångström Lab., Matl. Sci., PO Box 534, Uppsala SE-751 21 Sweden

In order to meet the requirements specified in the International Technology Roadmap for Semiconductors (ITRS), for realization of the aggressive downscaling, new materials need to be introduced. The regions of interest here are the source/drain (S/D) where shallow junctions need to be combined with low sheet resistance and low resistivity contacts, and the channel where high mobility is essential for high performance nano-MOSFETs. This so-called "material scaling" leads to a requirement for the integration of new materials in standard Si processing technology. One of the most promising candidates for the "material scaling" approach is $Si_{1-x}Ge_x$. The incorporation of compressively strained $Si_{1-x}Ge_x$ in a MOSFET, i.e. in the channel region or in S/D, has made the study of phase and morphology stabilities in $NiSi_{1-u}Ge_u$ on $Si_{1-x}Ge_x$ particularly interesting. The poor morphological stability of $NiSi_{1-u}Ge_u$ formed on $Si_{1-x}Ge_x$ is of a serious concern when forming contacts based on self-aligned silicide (salicide) technology. Our recent studies show that the agglomeration of $NiSi_{1-u}Ge_u$ begins already around 550 °C and is independent of the crystallinity of the underlying $Si_{1-x}Ge_x$ film, polycrystalline or single-crystal. We have identified that interdiffusion of Si and Ge inside the germanosilicide grains is a major cause for agglomeration. In the present work, we study the Si-Ge interdiffusion in $NiSi_{1-u}Ge_u$ using various single-crystal $Si_{1-x}Ge_x$ films of different compositions and different thickness combinations.Compressively-strained $Si_{1-x}Ge_x$ layers were grown epitaxially on Si(100) with chemical vapor deposition. Nickel films were deposited by means of electron-beam evaporation. The samples were annealed rapid thermally. A four-point probe was used to measure the sheet resistance in order to monitor the solid-state interaction as well as to correlate the resistance variation to the evolution of the surface morphology. Phase identification was carried out using X-ray diffraction. Scanning transmission electron microscopy in combination with energy dispersive spectroscopy was used to detail the morphology of the interface region. Our results show that a substantial interdiffusion of Si and Ge inside the $NiSi_{1-u}Ge_u$ grains already occurs at 600 °C. The atomic movement of the least mobile species at such low temperatures results in a rapid composition homogenization of a $NiSi_{0.78}Ge_{0.22}$/NiSi bilayer structure and a hindrance of the undesired $NiSi_2$-formation. It also leads to an improved morphological stability of the $NiSi_{0.78}Ge_{0.22}$/NiSi structure on Si, compared to the stability of $NiSi_{0.78}Ge_{0.22}$ on $Si_{0.78}Ge_{0.22}$. Our investigation als o shows that the film texture of $NiSi_{1-u}Ge_u$ is strongly affected by the characteristics of the $Si_{1-x}Ge_x$ layer and it is found that the layer sequence of the various $Si_{1-x}Ge_x$ layers influences the film texture. Ni interaction with the $Si_{0.78}Ge_{0.22}$/Si structure leads to a preferentially orientated textured $NiSi_{1-u}Ge_u$ film whereas $NiSi_{1-u}Ge_u$ formed on the Si/$Si_{0.78}Ge_{0.22}$ system gives a randomly orientated silicide film.

Session K: Quantum Dots in III-V and Group IV Compounds

Wednesday PM Room: 136
June 23, 2004 Location: DeBartolo Hall

Session Chair: Ben Shanabrook, Naval Research Laboratories, Nanostructures Section, Washington, DC 20375-5000 USA

1:30 PM

K1, Thermal Processing of InAs and InGaAs Quantum Dots for Device Integration: Forrest Kaatz[1]; *Jeff Cederberg*[1]; [1]Sandia National Laboratories, PO Box 5800, Albuquerque, NM 87185 USA

Semiconductor quantum dots are being investigated to take advantage of the effects of three-dimensional quantum confinement for optoelectronic devices. We are investigating InAs and InGaAs quantum dots formed by metal-organic chemical vapor deposition. The incorporation of quantum dots into integrated devices requires evaluation of their optical properties after thermal treatments used to modify the ground state energy. The InAs quantum dots investigated have a ground state at 1130 meV (1100 nm) when grown directly on GaAs layers. Investigations looked at a matrix of thermal treatments ranging from 600 to 900 C and times from 15 seconds to 1 hour. For samples annealed in contact with a GaAs wafer (proximity capping), we have observed a blue shift in the peak energy of 40 meV at 600 C for treatment times of 10 minutes. Extending this treatment out to 1 hour produces a 112 meV shift in the ground state. The emission intensity is retained for temperatures up to 650 C for the times investigated, but higher temperatures res ulted in significant intensity degradation, possibly due to non-radiative recombination at point defects formed during treatment. Quantum dot emission is not observed when the sample is annealed at 900 C for any length of time, setting a maximum processing temperature. Samples capped with PECVD SiO2 and annealed have similar annealing characteristics, however, the magnitude of the blue shift is reduced compared to the proximity capped samples. The origin of this effect is not clear, since SiO2 capping is known to enhance the disordering of quantum well structures. In0.40Ga0.60As quantum dots emitting at 1050 nm, treated using similar conditions, will be compared to the InAs structures to evaluate their thermal stability. Our results will be contrasted with results from the literature. Support from the Division of Materials Science and Engineering, Office of Science, U.S. Department of Energy, is gratefully acknowl edged. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

1:50 PM

K2, Thermal Effect on the Luminescence Properties of InP Quantum Dots Coupled with an InGaP Quantum Well Through a Thin InAlGaP Barrier: *X. B. Zhang*[1]; J. H. Ryou[1]; G. Walter[2]; N. Holonyak[2]; R. D. Dupuis[1]; [1]Georgia Institute of Technology, Sch. of Electric & Computer Engrg., Atlanta, GA 30332 USA; [2]University of Illinois, Micro & Nanotech. Lab., Urbana, IL 61801 USA

InP self-assembled quantum dots (SAQDs or simply QDs) on InGaP matrices have been studied by several research groups and on InGaAlP and InAlP matrices by the present authors. Lasers emitting in the red spectral region operating CW at 300K were realized by using In0.5(Al0.6Ga0.4)0.5P as the confining layer. We have demonstrated that by using an auxiliary InGaP quantum well (QW) coupled to InP QDs through a thin InAlGaP barrier layer (QW+QD structure), the carrier collection efficiency and the operation of QD lasers can be markedly improved. The QW with a thin barrier used here not only helps the thermalization of injected hot carriers in QW before they tunnel into the QDs but also helps the carrier injection in QDs. Furthermore, the thin barrier between the QW and QD layers can be used to adjust the uniformity and the density of QDs. This improved laser operation was also realized in the InAs QW+QD system. On the other hand, by directly