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Strain Engineering in SiGe/Si-on-Insulator Structures using Compliant Substrate and Stress Balance Approaches

J.C. Sturm[1], Haizhou Yin[1], R L. Peterson[1], K.D. Hobart[2], and F.J. Kub[2],

[1]Princeton Institute for the Science and Technology of Materials and Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA, sturm@princeton.edu
[2]Naval Research Laboratory, Washington, DC 20357 USA

1. Introduction

Since the role of strain was first made clear in altering the band alignment in Si/SiGe heterostrucutures [1], there has been a nearly 20-year search for technological approaches to achieve virtual substrates – layers with in-plane lattice constants different than those of the Si substrates, on top of which pseudomorphic layers could be grown. The usual approaches for such virtual substrates involve growing a "relaxed" layer such as SiGe by lattice-mis-matched epitaxy. The mismatch must be taken up by misfit dislocations, and their inevitable interaction leads to threading defects which reduce the quality of such layers. Typical densities in modern approaches are still $\sim 10^5$ cm^{-2}. In this work, we describe an approach for achieving relaxed SiGe layers and strained Si based on transferring a fully-strained pseudomorphic layer to a borophosphorosilicate (BPSG) layer, which can then allow the strain to relax at elevated temperature due to BPSG softening. The critical feature of the process is that in principle no dislocations are required, so that low-defect virtual substrates can be achieved. Relaxed buffer layers with Ge content up to >0.5 have been achieved, and the approach has also been used to achieve strained-Si-on-insulator with a thickness as low as 10 nm.

2. Process Overview and Critical Features

The approach begins with the deposition of BPSG (0.2 to 1.0 um) on top of a handle wafer, and the epitaxial growth of a pseudomorphic SiGe (in the most straightforward case) on a sacrificial wafer. The wafers are joined by low-temperature bonding, and the sacrificial wafer is removed by the Smart-cut process © and selective etching, to leave the SiGe layer on the BPSG layer [2]. At temperatures as low as 800 °C, the viscosity of the BPSG drops quickly, and when the viscosity is on the order of 10^{10} Ns/m^2, the SiGe layer can expand laterally to relieve its compressive strain. The time scale for the desired lateral expansion of the islands scales as the square of its edge length. There is a parasitic buckling process which also relieves strain, and it is mainly prevention of this phenomena which requires that the SiGe be patterned into islands (~100 microns in size at present) [3]. The strain throughout the process can be locally probed with micro-Raman spectroscopy [4].

3. Stress Balance

Once a SiGe film has been transferred to the BPSG, another layer can be grown on top of it either before or after it is relaxed. Upon annealing, a stress balance condition between the two layers can be achieved (Fig. 1). Using this approach, tensile Si on top of SiGe can be achieved. That the change in strain in one layer of a bilayer stack (e.g. the Si) changes exactly as the strain in the other layer (e.g. the SiGe) shows that they remain coherent (within a strain uncertainty of $\sim 3 \times 10^{-4}$), and that few if any dislocations form between the two layers (Fig.2) [5]. The time dependence of the change in strains in any one sample shows a similar correspondence. Besides growing tensile Si on top of the original SiGe, after relaxation, the average Ge content can be increased by growing a SiGe layer of higher Ge content, or by oxidizing the SiGe due to the rejection of the Ge from the growing SiO_2 [6].

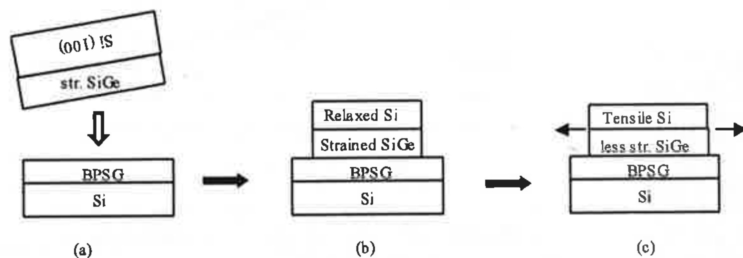

Fig. 1. Schematic process of (a) transfer of SiGe layer, (b) silicon epi and patterning, and (c) relaxation to form tensile silicon. Alternatively one could relax the SiGe first and then grow strained Si on top of the SiGe.

The tensile Si structure of Fig. 1 still contains a SiGe layer underneath, which may complicate processing due to implant annealing, silicide formation, oxidation, or other concerns such as device effects. If the original transferred layer has a thin Si epi layer (unstrained) on top of the strained SiGe, then the strained Si layer under the SiGe can be achieved after annealing. The SiGe can then be removed by selective etching to yield only a tensile strained Si-on-insulator layer. Strains of 1%, Si thicknesses as low as 10 nm, and NMOS mobility enhancements of 60% have been achieved (Fig. 4) [7].

4. Conclusions

The relaxation of transferred Si/SiGe layers on compliant BPSG layers offers new possibilities for engineering the strain in Si-based heterostructures with very low defect densities. Challenges currently under investigation to be reported involve mitigating any outdiffusion of dopants from BPSG with ultra-thin barriers, quantification of defect densities, increasing the island sizes, and uniaxial vs. biaxial strain.

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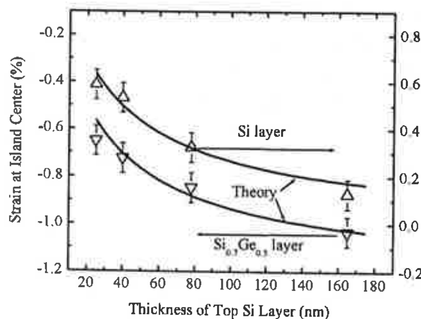

Fig. 2. Strain in both Si and SiGe after annealing at 800 °C of a bilayer 30 nm $Si_{0.3}Ge_{0.7}$/Si as a function of silicon thickness, showing consistent tracking between the two strains and coherency between the two layers [5].

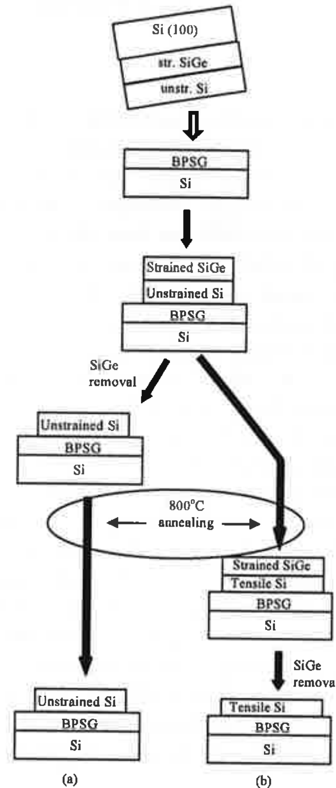

Fig. 3. Process flow for ultrathin (a) unstrained and (b) strained Si on insulator.

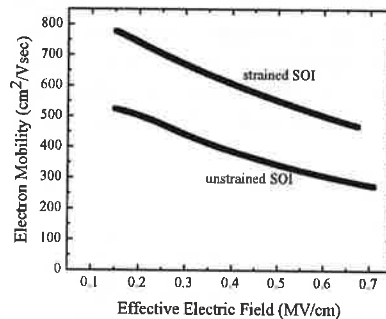

Fig. 4. Electron mobility in long-channel FET's on 30-nm strained (0.6% tensile) and unstrained Si on BPSG vs. vertical electric field.