# Session N: Materials Integration: Wafer Bonding and Alternative Substrates - II

Wednesday PM Room: Auditorium
June 25, 2003 Location: Olpin Union Building

*Session Chairs:* Karl Hobart, Naval Research Laboratory, Washington, DC 20375 USA; Matthew Seaford, RF Micro Devices, Greensboro, NC 27409 USA

**1:30 PM Student**
**N1, Scanning Photocurrent Measurements for the Nondestructive Evaluation of Waferbonded Interfaces**: *Phil Mages*[1]; Justin Bickford[2]; L. S. Yu[2]; D. Qiao[2]; T. Suni[3]; K. Henttinen[3]; I. Suni[3]; S. S. Lau[2]; P. K.L. Yu[2]; [1]University of California, San Diego, Matls. Sci./ECE, MC 0418, 9500 Gilman Dr., La Jolla, CA 92093-0418 USA; [2]University of California, San Diego, ECE, MC 0407, 9500 Gilman Dr., La Jolla, CA 92093-0407 USA; [3]VTT Centre for Microelectronics, PO Box 1208, 02044 VTT Finland

Unlike bonding techniques using reactive interlayers or surface oxides, hydrophobically bonded samples allow for the creation of conductive bonded interfaces, which are often regarded as a being perfect enough interface to have little effect on the devices made from such material. This advantage of the hydrophobically bonded interface, however, carries with it also the need for evaluation of the electronic properties of the interface. Though techniques such as infrared transmission photography and Scanning Acoustic Microscopy (SAM) allow for the non-destructive, large-scale mapping of physical features, such as interfacial bubbles, these techniques give no information about the electronic behavior of the interface. To obtain this information wafers must often be diced and processed so as to isolate different sections of the wafer for conventional current-voltage analysis. Since larger scale production would benefit from the ability to scan the wafers without such processing, we have developed a promising technique for probing the electronic properties of the interface using a small light beam scanned across the whole area of the wafers. The basic technique consists of monitoring the steady-state photocurrent generated locally as the wavelength of the monochromatic light beam is varied at each position on the unbiased sample. Using this method we have reported the ability to detect different interface behavior in samples of p-type Si initially bonded hydrophobically in normal room air, as compared to identical samples bonded in a dry nitrogen ambient.[1] Our initial simplified model describes the variation of photocurrent in terms of the change in photon penetration depth vs. wavelength and interfacial band bending due to the presence of charged interface states. Considering the variation of recombination velocity at the interface due to differing interface state densities, we present a deeper interpretation that is more directly related to localized states likely produced during the bonding process. Using these models we discuss photocurrent data and maps collected on samples having different bonding histories, bias conditions and background photon densities. Besides showing the obvious advantages of being able to differentiate between two interfaces which appear identical under SAM, we present data showing how the photocurrent vs. wavelength scans using different bias/illumination conditions allow for more detailed investigation of the interface state populations at the interface. Variations of such data over the area of bonded wafers having slight interface inhomogeneities are displayed. [1]L. S. Yu, P. Mages et. al., Applied Physics Letters, To be published 17 February 2003.

**1:50 PM Student**
**N2, Integration of Lattice-Mismatched Semiconductors with Si using $SiO_2$ CMP Layers and Wafer Bonding Ge/GeSi/Si Virtual Substrates**: *Arthur J. Pitera*[1]; Gianni Taraschi[1]; Minjoo L. Lee[1]; Chris W. Leitz[2]; Eugene A. Fitzgerald[3]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Rm. 13-4154, Cambridge, MA 02139 USA; [2]AmberWave Systems Corporation, 13 Garabedian Dr., Salem, NH 03079 USA; [3]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Engrg., 77 Massachusetts Ave., Rm. 13-5153, Cambridge, MA 02139 USA

High-quality Ge and III-V semiconductors fabricated on Si can significantly improve the functionality of CMOS electronics while providing the economic benefits of monolithic device fabrication on large diameter wafers. The Ge/GeSi/Si virtual substrate is a versatile platform for such integration of low defect density Ge and III-V semiconductors with Si. However, in order to make this approach practical, the thick graded buffer between the Si substrate and integrated layer must be removed. Wafer bonding virtual substrates to Si provides a solution for fabrication of lattice-mismatched layers in close proximity to the Si substrate without the limitation of small Ge or III-V wafers that are used in traditional bulk wafer bonding. Until recently, the virtual substrate bonding approach has been limited by the ability to CMP Ge virtual substrates. To circumvent this problem, we have planarized our virtual substrates through a low-temperature-oxide (LTO) CMP layer, which could be readily CMPed prior to wafer bonding. The CMP layer also serves to protect the Ge surface during post-CMP and pre-bond cleaning. Use of oxide CMP layers results in a Ge or III-V/oxide/Si structure which could also be applied to Ge-on-insulator (GOI) electronics. Furthermore, by depositing the insulating layer on the seed wafer, the bond interface is isolated far away from the device region thereby minimizing carrier scattering. Since our layers are transferred using hydrogen-induced layer exfoliation, the surface of the transferred Ge film suffers mechanical damage during the process. To remove this damaged region we have developed a novel technique to strip the top layer of Ge using chemical etching and a strained $Ge_xSi_{1-x}$ etch-stop layer. This approach provides extremely precise control of the transferred layer thickness allowing the possibility for future fabrication of ultra-thin GOI structures. We have determined that the thermal budget of buried $Ge_{0.6}Si_{0.4}$ etch-stop layers have a thermal budget of 650°C while maintaining a very high peroxide etch selectivity of >100:1 relative to Ge. In addition, densification of LTO on our Ge virtual substrates also has a temperature constraint of <650°C, therefore our film-transfer process has been tailored to stay within these thermal limitations. Current progress in device fabrication on these substrates will also be presented.

**2:10 PM Student**
**N3, Stress Balance of Si/SiGe and $SiO_2$/SiGe on Compliant Substrates**: *Haizhou Yin*[1]; K. D. Hobart[2]; S. R. Shieh[3]; T. S. Duffy[3]; F. J. Kub[2]; J. C. Sturm[1]; [1]Princeton University, Dept. of Electl. Engrg., E-Quad, Olden St., Princeton, NJ 08540 USA; [2]Naval Research Laboratory, Washington, DC 20375 USA; [3]Princeton University, Dept. of Geoscis., Princeton, NJ 08544 USA

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. However, the compliancy mechanism is not yet well understood. In this talk, we report stress balance observed in epitaxial Si/SiGe bi-layers on a compliant borophosphorosilicate glass (BPSG). Such stress balance in epitaxial multilayers on a compliant substrate has not been previously observed. This work indicates that the compliancy, in this case, originates from the viscous flow of the BPSG, instead of defect formation as observed in graded SiGe buffers. Previous work has focused on a single SiGe layer on BPSG.[1, 2] Here we first verify a coherent interface between SiGe and Si films on BPSG during relaxation process. We then successfully predict strains in Si/SiGe and $SiO_2$/SiGe stacks upon equilibrium based on stress balance between the layers. These results show that defects do not play a role in the relaxation of SiGe on BPSG. A wafer with 30 nm fully strained $Si_{0.7}Ge_{0.3}$ relaxed 25 nm Si/200 nm BPSG was fabricated by wafer bonding and Smart-cut as in ref. 1. Square SiGe islands of edge length 30 µm were then patterned. Upon annealing to reduce the viscosity of BPSG and thus remove the mechanical constraint from the substrate, the compressively strained SiGe layer expands to lessen the strain and the Si layer is stretched to become tensile. The observation of the same increase in the strain of both layers clearly implies an absence of slippage or misfit dislocations between the Si and SiGe layers. In addition, the final strains of the annealed samples confirm equilibrium stress balance between the layers. The stress balance theory is further verified by examining the final strains of the SiGe and Si films for various Si layer thickness. Lateral shrinkage of SiGe/Si islands was also examined during the stress balance process. A 30 µm SiGe island on BPSG was initially fully relaxed by lateral expansion, followed by a deposition of a commensurately strained Si layer by chemical vapor deposition (CVD. After annealing to reach

equilibrium, stress balance again accurately predicts the final strains. Stress balance with an amorphous oxide layer was observed. A $SiO_2$ cap was deposited on a fully strained SiGe layer on BPSG by plasmas-enhanced CVD. The $SiO_2$/SiGe stack was patterned to 30 µm islands and annealed to reach an equilibrium state. Good agreement between experimental data and stress balance theory is again observed, with the elastic constant of oxide as the single fitting parameter. Such oxide caps are of direct technological interest because oxide caps stiffen the SiGe layers and prevent film buckling.[3] This reduces the amount of strain relaxation of the SiGe layers. However, this drawback can be overcome by multiple cycles of cap thinning and further annealing. Stress balance of Si/SiGe and $SiO_2$/SiGe on BPSG shows that defect formation does not play a role in the SiGe relaxation on BPSG. Therefore this can be used to produce high quality relaxed SiGe layers. This work is supported by DARPA and ARO. [1]K.D. Hobart, et. al. Journal of Electronic Materials, 29, 897 (2000). [2]H. Yin, et. al. Journal of Applied Physics, 91, 9716 (2002). [3]H. Yin, et. al. MRS Spring Meeting, San Francisco, CA (2002).

**2:30 PM Student**

**N4, Adhesive Wafer Bonding of GaAs on Si and its Effect of SeS2 Treatments on the Structural Modification Changes of n-GaAs(100) Substrate**: *Premchander Perumal*[1]; *Krishnan Baskar*[1]; Arivuoli Dhakshnamoorthy[2]; [1]Anna University, Crystal Growth Ctr., Chennai, Tamil Nadu 600025 India; [2]Anna University, School of Electrical and Electronics Engineering, Anna University, Guindy campus, Chennai, Tamil Nadu 600025 India

Gallium Arsenide treated with chalcogenide has attracted recently in Opto-electronics and photovoltaic applications. In the present study we report the characteristics of GaAs treated with Selenium(IV)sulfide. LEC grown n-GaAs(100) doped with silicon has been used as a substrate. The carrier concentration was 1.1x1018 cm-3. The substrate was ultrasonically cleaned with Tricholoethylene(TCE), Acetone, Methanol and deionised water. It was chemically etched in H2SO4: H2O: H2O2 (4:1:1) solution and then in HCl for one minute. Substrates were immersed into SeS2/CS2 chemical solution bath with specific timings of 5s, 10s, 15s respectively. All the passivated samples were annealed at 350°C. The group-VI elements, such as S and Se treatments have distinct advantages in wafer bonding and passivation technologies. Recent reports show that Se can be easily incorporated in GaAs by making use of dangling bonds on the surface and result in Ga-Se related phases. These stable phases were analyzed by X-ray diffraction (XRD), Photoluminescence (PL) and Scanning Electron Microscopy(SEM) measurements and the results will be presented in detail. The SeS2 captured layers on GaAs can reduce the disorder induced interface states when bonded with other substrates such as silicon. The low temperature wafer bonded compliant wafers were confirmed by SEM.

**2:50 PM N5, Late News**

**3:10 PM Break**

**3:30 PM Student**

**N6, Wafer-Fused nAlGaAs-pGaAs-nGaN Heterojunction Bipolar Transistors**: *Sarah Marie Estrada*[1]; Huili Xing[2]; Andrew Huntington[1]; Andreas Stonas[2]; Larry Coldren[2]; Steven DenBaars[1]; Umesh Mishra[2]; Evelyn Hu[2]; [1]University of California, Santa Barbara, Matls. Dept., Santa Barbara, CA 93106-5050 USA; [2]University of California, Santa Barbara, Electl. & Compu. Engrg. Dept., Santa Barbara, CA 93106 USA

Recently we reported the first AlGaAs-GaAs-GaN heterojunction bipolar transistor (HBT), a device that might combine the high-breakdown voltage of an nGaN collector with the high mobility of a more technologically mature AlGaAs-GaAs emitter-base. Because the high degree of lattice mismatch between GaAs (lattice constant of 5.65A) and GaN (3.19A) precludes an all-epitaxial formation of this device, we formed the GaAs-GaN heterostructure via wafer fusion, also called direct wafer bonding. Our initial device was formed by fusion at a high temperature (750°C) and demonstrated low output current (~100A/cm2) and low common-emitter current gain (0.5).[1] This talk will describe a systematic variation of fusion temperature (550-750°C) in the formation of the HBT, and will reveal the correlation between fusion temperature, base-collector leakage, and emitter-base degradation. With reduced fusion temperature, devices demonstrate improvements in leakage, output current (~1kA/cm2), and common-emitter current gain (>1). The AlGaAs-GaAs emitter-base was grown by molecular beam epitaxy. A sacrificial layer (0.5um) of undoped AlAs was grown on (100) n+GaAs substrate, followed by a contact layer (0.1um n+GaAs, 1e19 cm-3 Si), the device emitter (0.18um graded nAlGaAs, 5e17 cm-3 Si), and finally the device base (0.15um p+GaAs, 1e19 cm-3 C). Carbon, rather than beryllium, was chosen as the p-type dopant in order to minimize dopant diffusion during the high-temperature fusion procedure. The uid-GaN collector (nominal 5e16 cm-3 Si) was grown by metal-organic chemical vapor deposition on c-plane (0001) sapphire. The GaN and GaAs structures were fused at systematically varied temperatures (550-750°C) for one hour under a uniaxial pressure of 2 MPa in a nitrogen ambient. After removal of the GaAs substrate and sacrificial AlAs, emitter (1e-5 cm2) and base mesas (5e-5 cm2) were defined. Emitter contacts were NiAuGe, base contacts were ZnAu, and collector contacts were AlAu. Gummel plots and common-emitter I-V characteristics were measured. Additionally, we are studying HBT structures with a reduced base thickness of 100 nm and a setback layer of two different thicknesses (20 or 50 nm). By introducing a GaAs base-collector setback layer, we hope to shift the fused GaAs-GaN interface slightly into the collector, decreasing the barrier prior to the possible spike at the fused heterojunction. Also, by utilizing lower fusion temperatures, the device is less susceptible to dopant diffusion, which should allow the use of a thinner base. [1]Sarah Estrada, Huili Xing, Andreas Stonas, Andrew Huntington, Umesh Mishra, Steven DenBaars, Larry Coldren, and Evelyn Hu, Wafer-fused AlGaAs/GaAs/GaN heterojunction bipolar transistor, Applied Physics Letters 82 (5), 820-2 (2003).

**3:50 PM**

**N7, Wafer-Bonding and Epitaxial Transfer of GaInAsSb/GaSb to GaAs Substrates for Monolithic Series Interconnection of Thermophotovoltaic Cells**: *Christine A. Wang*[1]; D. A. Shiau[1]; P. G. Murphy[1]; P. W. O'Brien[1]; M. K. Connors[1]; R. K. Huang[1]; A. C. Anderson[1]; D. Donetsky[2]; S. Anikeev[2]; G. Belenky[2]; D. M. Depoy[3]; G. Nichols[3]; [1]Massachusetts Institute of Technology Lincoln Laboratory, 244 Wood St., Lexington, MA 02420 USA; [2]State University of New York, Stony Brook, NY 11794 USA; [3]Lockheed Martin Corporation, Schenectady, NY 12301 USA

Thermophotovoltaic (TPV) devices are of interest for power generation from thermal radiation, and both lattice-matched GaInAsSb/GaSb and lattice-mismatched InGaAs/InP epitaxial materials are being developed for 0.5- to 0.6-eV TPV cells. In order to build open-circuit voltage and reduce I2R losses, it is desirable to monolithically interconnect the TPV cells in series. Such interconnection requires electrical isolation of the epitaxial device layers from the substrate, which can easily be achieved for InP materials by epitaxial growth on a semi-insulating (SI) substrate. However, the small bandgap (0.72 eV) of GaSb precludes the attainment of SI GaSb substrates. Therefore, alternative approaches for electrical isolation must be developed. This work reports the wafer bonding and epitaxial transfer of GaInAsSb/GaSb TPV epilayer structures to SI GaAs handle wafers. GaInAsSb/GaSb TPV structures with a lattice-matched InAsSb etch-stop layer were grown by organometallic vapor phase epitaxy. The epitaxial layers were bonded to SI GaAs substrates using SiOx/Ti/Au. This dielectric/metal reflector serves as both the bonding layer and as an internal reflector, which can enhance the performance of the TPV cell and provide spectral control of below bandgap photons. The bonding layer was designed to provide high reflectivity while minimizing internal stress in the final structure. To complete the epitaxial transfer, the GaSb substrate was either chemically or mechanically thinned to remove over 80% of the GaSb substrate, and then the remaining GaSb and InAsSb etch-stop layer were removed by selective chemical etching. Characterization of the wafer-bonded and transferred GaInAsSb/GaSb epilayers by high-resolution x-ray diffraction indicates minimal residual stress. Furthermore, photoluminescence (PL) and time-resolved PL measurements show enhancement in optical efficiency and minority carrier lifetime. Finally, wafer-bonded GaInAsSb/GaSb/GaAs TPV cells were fabricated and monolithically interconnected in series. Nearly linear voltage building is reported. At a short-current density of 0.4 A/cm2, the open-circuit voltage for a single TPV device is 0.2 V, compared to 0.37 and 1.8 V for 2- and 10-junction devices, respectively. This paper will discuss the design, growth, fabrication, characterization, and performance of wafer-bonded GaInAsSb/GaSb/GaAs TPV devices.

**4:10 PM Student**

**N8, III-V on Insulator Composite Substrates**: *Sumiko Lynn Hayashi*[1]; Rajinder Singh Sandhu[2]; David Bruno[1]; Mike Wojtowicz[2]; Mark S. Goorsky[1]; [1]University of California, Los Angeles, Dept. Matls. Sci. & Engrg., 2521 Boelter Hall, 420 Westwood Plaza, Los Angeles, CA 90095