ICSI3

Third International Conference on SiGe(C) Epitaxy and Heterostructures

March 9 to 12, 2003

Derek Houghton, Chair

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M.J. Palmer, M.J. Prest, T.J. Grasby, P.J. Phillips, E.H.C. Parker, T.E. Whall, Department of Physics, University of Warwick, Coventry, UK.

4 30 — **Characterization of High Ge Fraction SiGe-Channel MOSFET with Ultrashallow Source/Drain Formed by Selective B-Doped SiGe CVD,** Shnobu Takehiro [a], Doohwan Lee [a], Masao Sakuraba [a], Junichi Murota [a] and Toshiaki Tsuchiya [b] [a]Research Institute of Electrical Communication, Tohoku University, Sendai, Japan. [b] Interdisciplinary Faculty of Science and Engineering, Shimane University, Shimane, Japan

Session X — SHORT PRESENTATIONS FOR POSTER SESSION II

Session Chair: Yashiro Shiraki, University of Tokyo

4 45 — **A Novel Mobility Spectrum Computational Analysis using a Maximum Entropy Approach and its Applications for Magnetotransport Phenomena in Pseodo- and Metamorphic p-Si $_{1-x}$Ge $_x$ / Si $_{1-y}$Ge $_y$ / (001)Si MODFET Structures**, O.A. Mironov, M. Myronov, Department of Physics, University of Warwick, Coventry, UK

4 48 — **The Inverter as an Example of the Vertical Tunnel FET Circuit Design.** Th. Nirschl[1], S. Sedlmaier[2], P.-F. Wang[1], W. Hansch[1], I. Eisele[2], and D. Schmitt-Landsiedel[1] [1] Technical University Munich, Institute of Technical Electronics, Munich, Germany. [2] University of the Bundeswehr Munich, Institute of Physics, Neubiberg, Germany.

4 51 — **High Mobility Hole Gases in Ge Modulation Doped Quantum Wells**, G. Isella[a], D. Chrastina[a], B. Rößner[b], E. Müller[b], M. Bollani[c], M. Kummer[b] and H. von Känel[a, b] a - INFM- Dip. di Fisica, Politecnico di Milano, Como, Italy, b - Laboratorium für Festkörperphysik, ETH Zürich, Switzerland, c - INFM-Dip. Scienza dei Materiali, Milano Italy

4 54 — **In-Line Ordered Ge/Si Islands on Patterned Substrates,** T. Stoica, L. Vescan, E. Sutter[1], and C. Dieker[2] Institut für Schichten und Grenzflächen, Forschungszentrum Jülich GmbH, Jülich, Germany [1]Colorado School of Mines, Golden, CO, USA; [2]University of Ausburg, Germany

4 57 — **Low Temperature Wafer Cleaning and Manufacturing of SiGe Virtual Substrates,** H.M. Buschbeck, A. Erhart, Y.Goeggel, C. Rosenblad, S. Wiltsche, J. Ramm, Unaxis Semiconductors, Balzers, principality of Liechtenstein, A. Dommann, M. Kummer, Interstate University of Applied Science, Buchs, Switzerland

5 00 — **Strain Relaxed SiGe Virtual Substrate Grown at Various Temperatures,** H.H. Cheng[1], X.S. Wu[2], Z.P. Yang[1], H.M. Lo[3], P. Lin[3], C.W. Kuo[3], and K.M. Huang[3] [1]Center for Condensed Matter Sciences and Institute of Electronic, Taiwan University, Taipei, Taiwan, [2]Department of Electrical Engineering, Durham University, Durham, England, U.K, [3]Department of Electronics Emgineering, National Kaohsiung University of Applied Sciences, Kaohsiung, Taiwan

5 03 — **Impact of the Annealing Temperature on the Homogeneity of SiGe-on-insulator** N. Usami, K. Kutsukake, K. Fujiwara, T. Ujihara, G. Sazaki, S. Ito, B. P. Zhang [*]and K. Nakajima, nstitute for Materials Research (IMR), Tohoku University, Sendai, Japan [*]Photodynamics Research Center, The Institute of Physical and Chemical Research (RIKEN), Sendai, Japan

5 06 — **Very Thin SiGe Buffer Layer Growth by Thermally-Driven Relaxation,** Sang-Hoon Kim, Young-Joo Song, Kyu-Hwan Shim, Jin-Young Kang, SiGe Device Team, Wireless Communication Devices Department, ETRI, Daejeon, Korea

5 09 — **Strained-Si-on-Insulator MOSFET without Relaxed SiGe Buffer Layer,** H. Yin[1], K.D. Hobart[2], R.L. Peterson[1], S.R. Shieh[3], T.S. Duffy[3] and J.C. Sturm[1], [1]Center for Photonics and Optoelectronic Materials and Dept. of Electrical Eng., Princeton University, Princeton, NJ, [2]Naval Research Laboratory, Washington, DC, [3]Dept. of Geosciences, Princeton University, Princeton, NJ, USA

5 15 to 6 30 — **POSTER SESSION II**

7 30 — **BANQUET**

WEDNESDAY MARCH 12

Session XI — DEVICE PHYSICS AND NOVEL STRUCTURES

Session Chair: Erich Kasper, University of Stuttgart, Germany

8 30 Invited — **Si/SiGe(C) Epitaxy by RTCVD for Advanced Electronics**, D.Dutartre, A. Talbot, F. Deléglise, C. Fellous, ST Microelectronics, Crolles, France

Strained-Si-on-Insulator MOSFET without Relaxed SiGe Buffer Layer

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ABSTRACT

Strained Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) have drawn increasing attention for superior carrier mobility. These are typically grown on relaxed SiGe buffer layers or on top of thin relaxed SiGe layers that are transferred to an insulator for a SiGe-on-insulator structure. In this work, we demonstrate strained Si MOSFETs fabricated on compliant borophosphorosilicate glass (BPSG) without an underlying SiGe buffer layer. This overcomes any potential process or device drawbacks due to presence of a SiGe layer.

We first investigate the relaxation of SiGe on BPSG, which indicates that dislocations do not contribute to the strain relief. We then show that a bi-layer structure can improve surface roughness during relaxation. In addition, we observe stress balance of bi-layer structures on BPSG, which enables tensile Si using a SiGe/Si/BPSG structure. Finally, we fabricate n-MOSFETs on tensile Si/BPSG and observe mobility enhancement due to the strain.

EXPERIMENTS AND ANALYSIS

Strained SiGe on BPSG films were fabricated by wafer bonding and Smart-cut® processes [1]. The host wafer was a silicon wafer on which 30 nm commensurately strained $Si_{0.70}Ge_{0.30}$ was grown followed by 2 nm Si cap. This wafer was then implanted with H_2^+ at an ion energy of 180 keV and a dose of 4.5×10^{16} cm^{-2}. The handle wafer was coated with 200 nm BPSG (4.4% B and 4.1% P by weight). The wafers were cleaned and bonded at room temperature. The wafer pair was annealed at 250°C for four hours to enhance bond strength and then annealed at 550°C in N_2 ambient to separate the top layer from the host substrate at the depth of the hydrogen implant. The remaining silicon on top of the SiGe was removed by selective etching to leave approximately 30 nm compressively strained $Si_{0.70}Ge_{0.30}$ on the BPSG. The SiGe was then patterned to square islands of various sizes from 10 to 200 μm to study relaxation.

Lateral expansion and buckling simultaneously contribute to strain relaxation of SiGe islands on BPSG when the BPSG is softened during anneals [2]. Lateral expansion initiates at the boundary of islands, whereas buckling occurs near the center of islands where it is difficult to relieve strain by lateral expansion. Fig. 1 shows an optical micrograph of a corner of a 100 μm × 100 μm SiGe island on BPSG after 90 min anneal at 790°C. It shows three distinct relaxation regions: (1) Buckling is entirely avoided in the corner of the island where lateral expansion takes place quickly to relax strain, (2) buckling appears in areas where lateral expansion only releases strain along one

direction, i.e., normal to the edge, and (3) buckling appears in the island center where strain is only relaxed by buckling.

To improve surface roughness caused by buckling during relaxation anneals and to achieve large flat islands, a bi-layer structure was adopted. A bi-layer is effectively more rigid than a single layer, and thus less prone to buckling. Prior to SiGe relaxation, a Si/SiGe bi-layer structure was formed by deposition of an epitaxial Si layer on top of SiGe/BPSG using rapid thermal chemical vapor deposition (RT-CVD) at 700°C. Figure 2 shows the dramatic improvement of surface roughness after relaxation anneals when a Si/SiGe bi-layer structure is employed; rms roughness of less than 1 nm can be achieved. The final strain in the SiGe and Si films upon equilibrium is governed by stress balance between the layers, namely zero net stress between the SiGe and Si films in any vertical plane. For the first time, stress balance between layers on compliant substrates is observed. Figure 3 shows good agreement between experimental data and the stress balance theory, which assumes no dislocations. To further determine dislocations' possible role in the SiGe relaxation on BPSG, defect etching of 90 nm $Si_{0.7}Ge_{0.3}$ grown on relaxed 30 nm $Si_{0.7}Ge_{0.3}$/BPSG and on regular Si was performed (Fig. 4). An observed defect density less than 1×10^5 cm^{-2} on SiGe/BPSG shows that dislocation-induced relaxation is not dominant and that SiGe relaxation on BPSG is a good approach to achieve high quality relaxed SiGe.

We now use this approach to create strained Si on insulator without SiGe (Fig. 5). A structure of a relaxed 25 nm Si cap on fully strained 30nm $Si_{0.7}Ge_{0.3}$ was transferred to 200 nm BPSG on a handle wafer, so that the unstrained Si layer was on the bottom after the transfer. Then the continuous SiGe/Si films were patterned into square islands of sizes from 80 μm to 200 μm. During a 90 min anneal at 800°C, the SiGe/Si islands expanded laterally to move toward stress balance, resulting in tensile Si on the bottom. Finally, the top SiGe film was selectively etched to yield tensile Si on BPSG.

N-channel MOSFETs were fabricated using the tensile Si as the device channel. The gate stack includes 300 nm SiO_2 and 80 nm poly-Si, both deposited at 625°C by LPCVD. The poly gate and source/drain were doped by phosphorus ion implantation (25keV at dose 1×10^{15} cm^{-2}). Dopants were activated by a 30 min anneal at 700°C. Unstrained Si n-MOSFETs on BPSG were fabricated in the same batch for comparison. An electron mobility enhancement of approximately 20% was clearly seen in the strained Si n-MOSFETs compared to the unstrained Si devices based on the measured transconductance (Fig. 6).

SUMMARY

We demonstrate relaxed SiGe and strained Si on insulator by a compliant BPSG film. Stress balance in Si/SiGe films on BPSG is observed and used to realize strained Si on insulator without SiGe. Finally, strained Si on insulator n-MOSFETs are fabricated and electron mobility enhancement is observed.

This work is supported by DARPA and ARO.

Reference:

1. K.D. Hobart, *et. al. Journal of Electronic Materials*, 29, 897 (2000).
2. H. Yin, *et. al. Journal of Applied Physics*, 91, 9716 (2002)

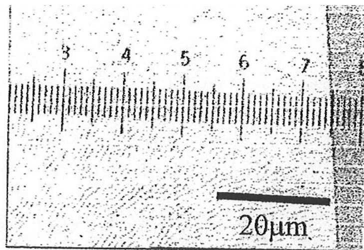

Fig. 1. Optical micrograph of a corner of 100 μm × 100 μm $Si_{0.7}Ge_{0.3}$ island after a 90 min anneal at 790°C in nitrogen

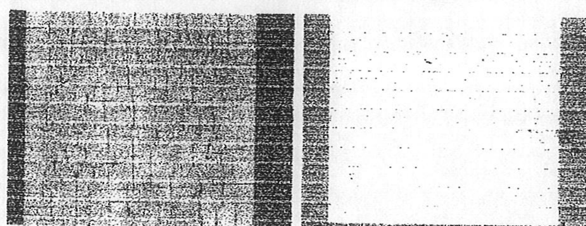

Fig. 2(a) Fig. 2(b)

Fig. 2. Optical micrograph of 500 μm islands after long anneals (a) 30 nm $Si_{0.7}Ge_{0.3}$/BPSG (b) 31 nm Si/30 nm $Si_{0.7}Ge_{0.3}$/BPSG

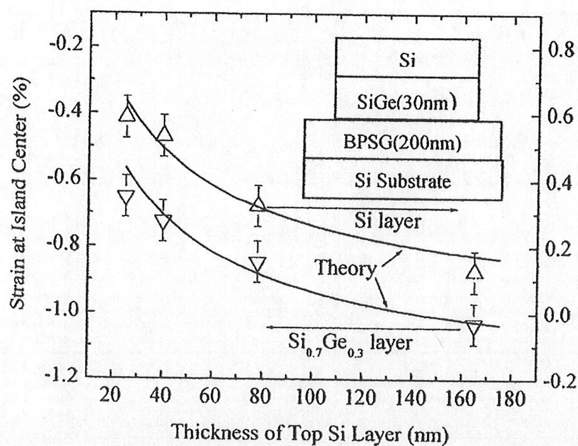

Fig. 3. Equilibrium biaxial strain of 30nm $Si_{0.7}Ge_{0.3}$ and Si films at the center of a 30 μm x 30μm island as a function of Si film thickness. Open symbols are experimental data. Lines are theoretical calculations of stress balance. The strain was measured by micro-Raman spectroscopy.

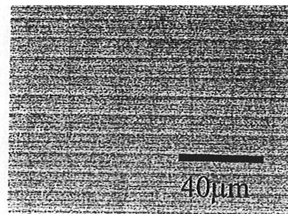

Fig. 4(a)

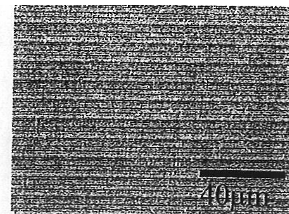

Fig. 4(b)

Fig. 4. Defect etch of annealed 90 nm $Si_{0.7}Ge_{0.3}$ grown on (a) 20 μm islands of relaxed 30 nm $Si_{0.7}Ge_{0.3}$/BPSG and (b) Si substrate

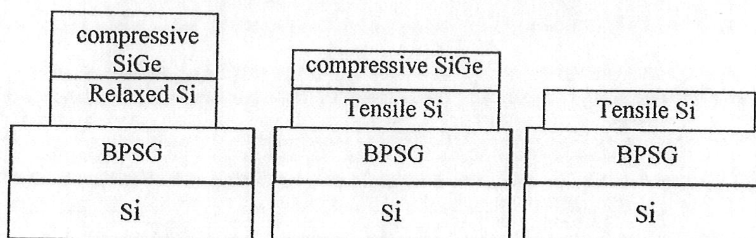

Fig. 5(a) Fig. 5(b) Fig. 5(c)

Fig 5: Stress balance enables tensile Si on BPSG: (a) SiGe/Si islands on BPSG were fabricated by SiGe epitaxy, wafer bonding, Smart-cut and RIE etch; (b) SiGe and Si films expand towards stress balance in a 90 min anneal at 800°C in N_2; (c) Removal of the top SiGe film results in strained Si on insulator.

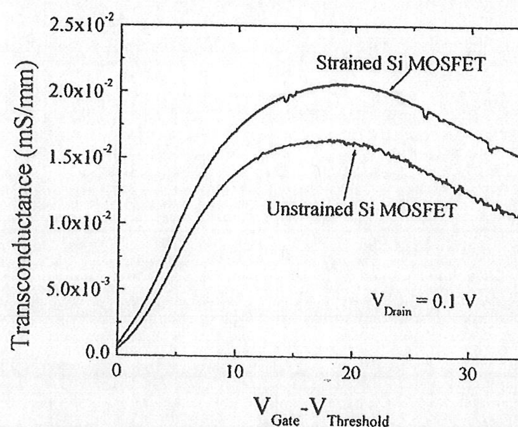

Fig. 6. Transconductance as a function of gate voltage for strained and unstrained Si n-MOSFETs (L = 20 μm, W = 200 μm). The high gate voltages are due to a very thick (300 nm) gate oxide.