P-channel Thin Film Transistor of Microcrystalline Silicon Directly Deposited at 320°C

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We report the first p-channel thin-film transistor made in directly-deposited microcrystalline silicon (μc-Si). The channel silicon is made by plasma-enhanced vapor deposition (PECVD) in a process similar to the deposition of hydrogenated amorphous silicon (a-Si:H). The deposition temperature for the μc-Si is 320°C and the highest post-deposition TFT process temperature is 280°C. The p-channel TFT is made possible by the low-temperature deposition of μc-Si with near-intrinsic properties. Because making p-channel TFTs of *a-Si:H* has not been possible to date, the p-channel μc-Si TFT represents a breakthrough in low-temperature Si TFT technology.

The TFTs were fabricated in the top-gate configuration on unpassivated Corning 7059 glass substrates. The μc-Si layer was deposited by plasma enhanced CVD using a mixture of SiH_4, SiF_4 and H_2. A four-level mask process with specially designed masks was used in the TFT fabrication. The schematic cross section of the TFT structure is shown in Figure 1. First the 300 nm thick μc-Si layer and a 60 nm p^+ μc-Si layer were grown without breaking vacuum. Next we patterned (1) the intrinsic layer island and (2) the p^+ μc-Si source and drain using reactive ion etching (RIE). After depositing 300nm thick SiN_x by PECVD at 280°C as the gate insulator, we patterned the SiN_x gate and opened contact holes to the p^+ source and drain using RIE. Then we thermally evaporated Al, and in a last step patterned the gate, source and drain electrodes using an Al wet-etchant. The fabricated TFTs were annealed in $H_2 + N_2$ at 200 °C for 1 hour.

Figure 2 and Figure 3 show the transfer and output characteristics of the p-channel TFT. In Figure 2 the drain current I_d is plotted against gate voltage V_{gs} for drain voltage V_{ds} at -0.1 V, -4 V and -10 V. In Figure 3 the drain current is plotted against the drain voltage for gate voltage from 0 to -30 V. In Figure 2 for V_{ds} = -10 V the ON/OFF current ratio is 2.5 x 10^3 when V_{gs} varies from -5 V to -25 V and for V_{ds} = -4 V the ON/OFF current ratio is > 10^5. The threshold voltage is -13 V, and the subthreshold slope S = 2.8 V/dec. The linear and saturated hole mobilities of the TFT are 0.026 and 0.041 cm^2/Vs respectively. While these mobilities are low, they demonstrate p-channel operation. We are analyzing the TFT characteristics and experimenting with fabrication to improve TFT performance.

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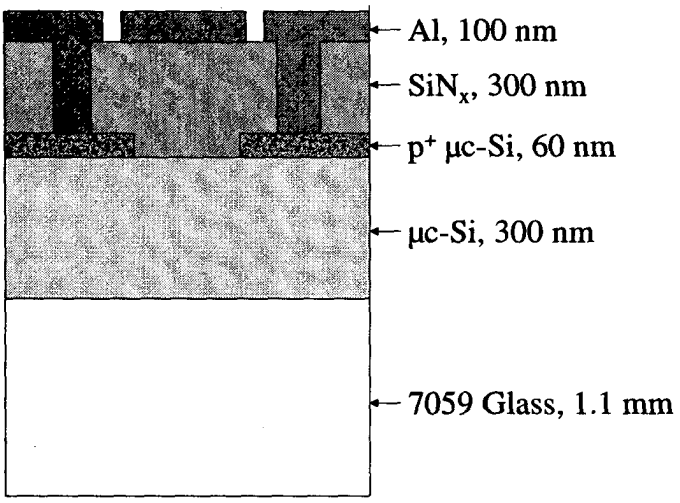

Figure 1. Schematic cross section of the p-channel TFT

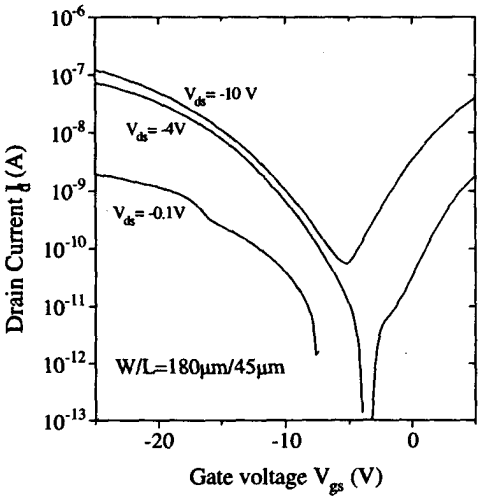

Figure 2. TFT transfer characteristics

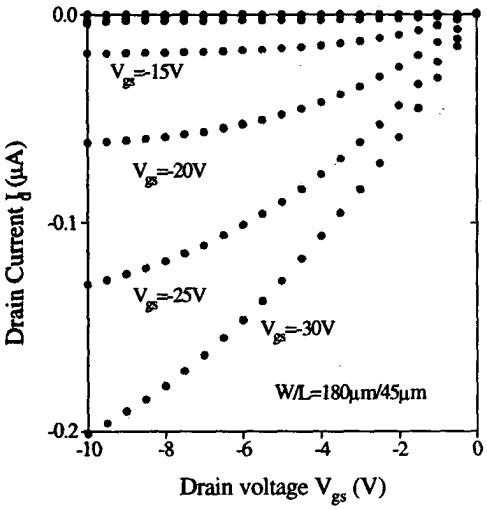

Figure 3. TFT output characteristics