MATERIALS RESEARCH SOCIETY
SYMPOSIUM PROCEEDINGS VOLUME 525

Rapid Thermal and Integrated Processing VII

Symposium held April 13–15, 1998, San Francisco, California, U.S.A.

EDITORS:

Mehmet C. Öztürk
North Carolina State University
Raleigh, North Carolina, U.S.A.

Fred Roozeboom
Philips Research Laboratories
Eindhoven, The Netherlands

Paul J. Timans
AG Associates
San Jose, California, U.S.A.

Sylvia H. Pas
Texas Instruments
Dallas, Texas, U.S.A.

Materials Research Society
Warrendale, Pennsylvania

Materials Research Society Symposium W
San Francisco, CA, Apr. 13-15, 1998

Novel Applications of Rapid Thermal Chemical Vapor Deposition for Nanoscale MOSFET's

J.C. Sturm, M. Yang, C.L. Chang, and M.S. Carroll, Center for Photonics and Optoelectronic Materials, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA

Abstract

In this paper we examine several applications of Rapid Thermal Chemical Vapor Deposition (RTCVD) for the fabrication of sub-100 nm MOSFET's. Vertical dual-gated MOSFET's are used as a test vehicle to implement FET's of very short channel length. To realize such devices, the ability of epitaxial $Si_{1-x-y}Ge_xC_y$ layers for suppressing the thermal diffusion, transient enhanced diffusion, and oxidation enhanced diffusion of boron both in the $Si_{1-x-y}Ge_xC_y$ and in nearby Si layers is very useful. Novel gate electrodes deposited by RTCVD also showed the ability to greatly reduce boron penetration in p-type polycrystalline gates for p-channel FET's.

Introduction

For many years a primary driving force behind Rapid Thermal Chemical Vapor Deposition (RTCVD) has been the growth of epitaxial silicon/silicon-germanium alloy layers for silicon-based heterostructures. The applications of such heterostructures include heterojunction bipolar transistors (HBT's) [1] and silicon-based optoelectronic devices such as infrared detectors and emitters. While SiGe HBT's are now entering commercial production, the vast majority of the integrated circuit field is now focused on CMOS because of its low power dissipation and resulting high integration levels. Considerable work in the field of RTCVD has been directed at MOS structures as well. A partial list of driving forces and key results to date have included the ability to form gate stacks without breaking vacuum [2], the use of polycrystalline SiGe gate electrodes to shift work function [3, 4], selective epitaxy or selective polycrystalline Si/SiGe growth for raised source/drains and/or low resistance source/drain contacts [5], and heterostructures for high mobility p-channel and n-channel devices [6,7].

In this paper, we further consider long-term applications of RTCVD towards MOSFET's, focusing on channel lengths under 100-nm. Issues discussed in the paper are the use of substitutional carbon in $Si_{1-x-y}Ge_xC_y$ to dramatically suppress boron diffusion, vertical dual-gated MOSFET's, and SiGeC polycrystalline gates to suppress boron penetration through gate oxides.

Boron Diffusion and $Si_{1-x-y}Ge_xC_y$

The rapid diffusion of boron in silicon due to its high intrinsic diffusion coefficient, transient enhanced diffusion (TED) due to damage created by ion implants, and oxidation enhanced diffusion (OED) due to interstitials injected by oxidation are a severe problem

Mat. Res. Soc. Symp. Proc. Vol. 525 © 1998 Materials Research Society

for short channel MOS scaling. For example, they affect p-channel devices by affecting the source/drain profile and n-channel devices through the motion of the boron in the channel region. During the past few years, it has been documented that carbon-doped silicon has a much lower rate of boron diffusion in all of the above cases than silicon without carbon [8-11]. The carbon has been introduced both by ion implantation and by direct incorporation during the molecular beam epitaxy (MBE) growth of silicon. The details of the mechanism are still not clear, but apparently the C traps the interstitials that lead to boron diffusion. Ion implantation is not attractive, however, since the location of the carbon cannot be precisely controlled with nm precision, and MBE of C-doped epitaxial layers is not attractive for manufacturing. Therefore the RTCVD of C-doped epitaxial layers is an attractive alternative for such work.

$Si_{1-x-y}Ge_xC_y$ by RTCVD was first reported in 1993 [12], and at Princeton we then investigated its application as the base of a HBT because of its potential greater critical thickness on Si (100) for a given bandgap than $Si_{1-x}Ge_x$ [13,14]. The films used in the work described in this paper were grown RTCVD at 6 torr from dichlorosilane, germane, and methylsilane in a hydrogen carrier from 575 - 625 °C [15]. Fig. 1 shows the X-ray diffraction spectra of a pseudomorphic SiGeC layers grown on Si for increasing levels of methylsilane flow, leading to increased levels of substitutional carbon (and a smaller lattice constant). As the methylsilane flow is increased, the diffraction peak moves back towards that of the Si substrate, indicating a reduction in strain in the layer as carbon is incorporated onto substitutional sites. From the magnitude of the shift, the substitutional carbon level can be inferred. All of the carbon levels quoted in this paper are substitutional carbon levels measured as such, assuming that one substitutional carbon atom compensates for the strain of 8.3 Ge atoms.

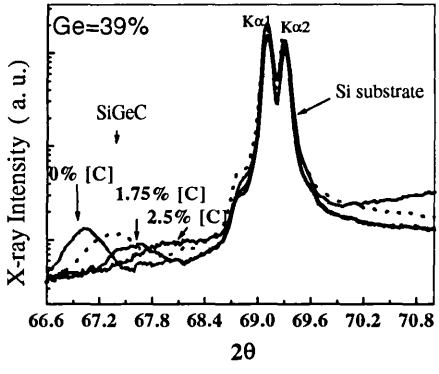


Fig. 1: (004) X-ray diffraction spectra for $Si_{1-x-y}Ge_xC_y$ pseudomorphic thin films on Si (001). The two substrate peaks are due to both Cu $K_{\alpha 1}$ and Cu$K_{\alpha 2}$ X-ray lines, and the Ge fraction is 0.395 [14].

In HBT's the diffusion of boron in the base is a crucial issue, and it was found that as in silicon, small (e.g. 0.5%) carbon levels in SiGe lead to a vastly reduced diffusion coefficient of boron compared to that without carbon, both in cases of intrinsic diffusion and also transient-enhanced diffusion [16]. Fig. 2 shows the dramatic effect that carbon can have on such diffusion through the secondary ion mass spectroscopy profiles (SIMS) of boron, carbon, and germanium in the base of $Si/Si_{1-x-y}Ge_xC_y/Si$- HBT's, after the top 50 nm of the 300 nm Si emitter has been implanted with a heavy dose of As^+ and the entire structure was annealed at 755 °C for 15 min in nitrogen. The nominal Ge fraction is 0.2. Fig. 2(a) shows the usual effects of TED on boron from the overlying implant, with the diffusing wings of boron clearly visible. In contrast, in the structure of Fig. 2(b), with 0.5% C added to the SiGe, the boron profiles after annealing are indistinguishable from those before annealing, without boron tails. The structure of Fig.2(c) has boron-doped SiGe without C outside the C-doped region in the center of the base, yet in this case there is still no evidence of TED, even though no C exists in the regions from which the diffusing B should come. This shows that the effect of C on diffusion are non-local – i.e. that carbon in one location can reduce boron diffusion some distance away.

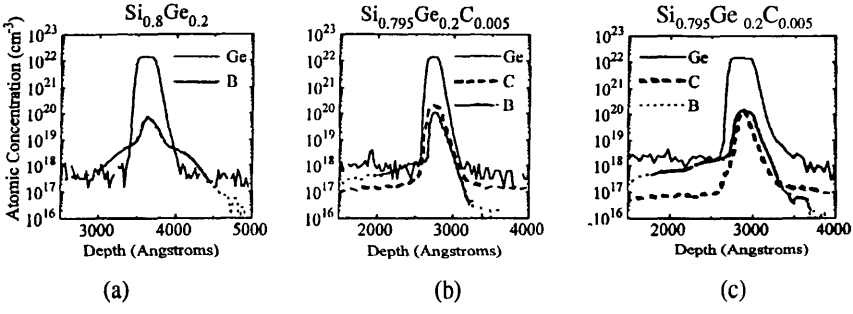
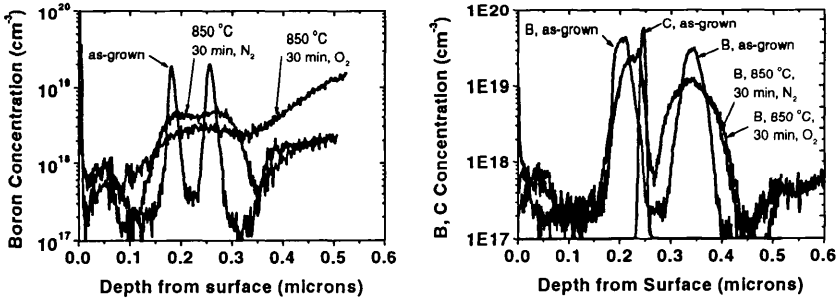


Fig. 2. SIMS profiles of B, Ge, and C in the base of $Si/Si_{1-x-y}Ge_xC_y/Si$ HBT's after the emitter was implanted with As^+ (1.8×10^{15} cm^{-2}) and the structure annealed at 755 °C for 15 min in nitrogen. As grown, the structures have undoped SiGe (a,c) or undoped $Si_{1-x-y}Ge_xC_y$ (b) 5 nm spacers on either side of the doped region. The structure of (c) has 0.5% C only in the central part of the base, with 5 nm doped SiGe regions without C on either side of the doped $Si_{1-x-y}Ge_xC_y$ region. [16].

To further explore this ability of $Si_{1-x-y}Ge_xC_y$ to greatly reduce boron diffusion some distance away from the $Si_{1-x-y}Ge_xC_y$ itself, a test structure was grown by RTCVD with two narrow B-doped silicon marker layers grown in-situ. An undoped SiGeC layer of varying Ge and C concentration was grown between the two B-doped Si layers. With this structure the effect of SiGeC could be studied on the overlying and underlying B doped Si layers. Samples were then annealed in either nitrogen or oxygen and dopant profiles were analyzed by SIMS. Fig. 3 shows SIMS profiles in such a structure, both with and without a SiGeC layer between the two boron doped silicon layers, as-grown and after annealing in

nitrogen and oxygen at 850 °C for 30 min. Note that the lower B peak diffuses in both samples after nitrogen annealing, and in the sample of Fig. 3(a) (silicon-only) the diffusion in the case of oxygen annealing is much greater than that for nitrogen. Modelling of the measured profiles shows that the diffusion coefficient of the lower B peak in 3(a) is 10 times larger for oxygen annealing than that for nitrogen annealing, an example of the severity of the OED effect. The sample of Fig. 3 (b) has a SiGeC layer with 0.5% C inserted between the two boron peaks. This layer effectively prevents any interstitials created by oxidation from reaching the lower B-doped Si layer, completely suppressing the OED effect. Further experiments are in progress to numerically correlate carbon levels and boron diffusion suppression under various conditions.



(a) (b)

Fig. 3. SIMS profiles of boron-doped Si layers as grown and after annealing in nitrogen or oxygen for 30 min at 850 °C. In the sample of Fig. 3(b) a SiGeC layer with 0.5 % C has been inserted between the two boron peaks as shown.

Vertical Dual-Gated MOSFET's

As FET's are scaled below 0.1 um, it is natural to explore other FET structures with potentially improved scaling properties besides the usual lateral, top-gate configuration. One attractive alternative is the dual-gated structure, in which gates are placed both on top and below a thin silicon film. If the film is thin, the gates effectively control the potential throughout the film, and short-channel effects such as punchthrough and threshold barrier lowing can be overcome [17] without the necessity for high levels of channel doping. For structures with a channel length much below 0.1 um, this thickness should be on the order of the channel length. Fabricating this structure in a horizontal orientation is difficult due to the difficulty of fabricating and patterning a lower gate under a silicon thin film. One alternative is to make such a structure in a vertical orientation as shown in Fig. 4. In this method the source/channel/drain structure is grown epitaxially, so that the channel length is then defined by epitaxy, not by lithography. The thickness of the silicon film (a lateral dimension in a vertical FET) would have to be defined by lithography, however. Fig. 4 shows a possible fabrication process for such a structure

which we are pursuing. First, an opening is defined in a field oxide, through which a source/channel/drain structure is grown by selective epitaxy. After the field oxide is removed, one can then grow gate oxide and deposit the gate, pattern it using self-aligned techniques, and finally add contacts. Fig. 5 shows a long-channel test structure (L ~ 1 um) grown by RTCVD after the field oxide has been removed and before the gate oxidation/polysilicon deposition step.

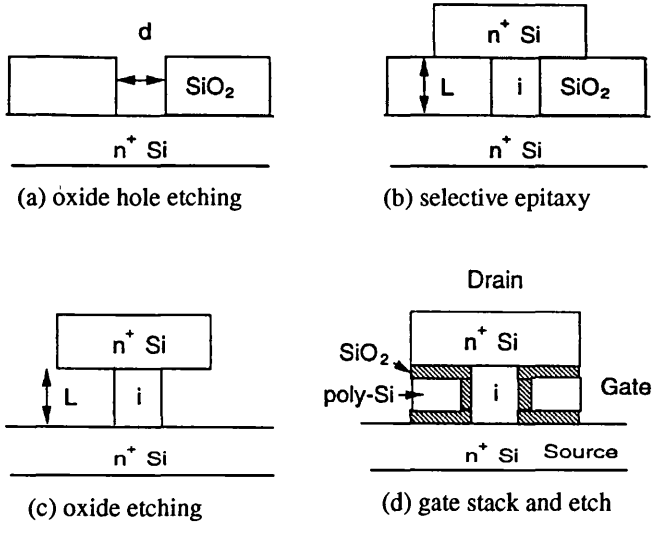


Fig. 4. Schematic diagram and fabrication process for vertical dual-gated MOSFET's: (a.) field oxide hole formation, (b.) selective epitaxy, (c.) field oxide removal, (d.) gate stack and etch.

Well-behaved current voltage curves for a vertical p-channel device with a 0.5 micron channel length and 9 nm gate oxide are shown in Fig. 6. Because we have not yet combined the vertical FET structure with a very thin vertical pillar (to prevent short-channel effects), this device had a channel which was doped n-type in-situ with phosphorus to prevent punchthrough. Efforts to scale this device to channel lengths of 0.1 um or less were unsuccessful, however. Simulation showed that this was due to the diffusion of the boron source/drain dopant during the gate oxidation cycle (which was typically 750 °C on the order of 30 minutes), and the diffused dopant led to a short between source and drain. Simulation also showed that the oxidation enhancement of the boron diffusion was largely responsible for this excessive boron diffusion.

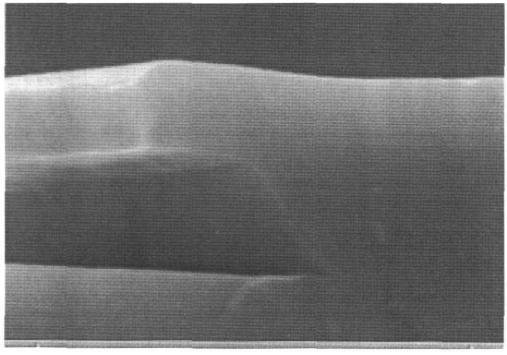


Fig. 5. Cross section of a long-channel test structure for vertical dual-gated MOSFET's after removal of the field oxide and before gate oxide/gate deposition. Distance between bottom of overhang and substrate is ~0.7 um.

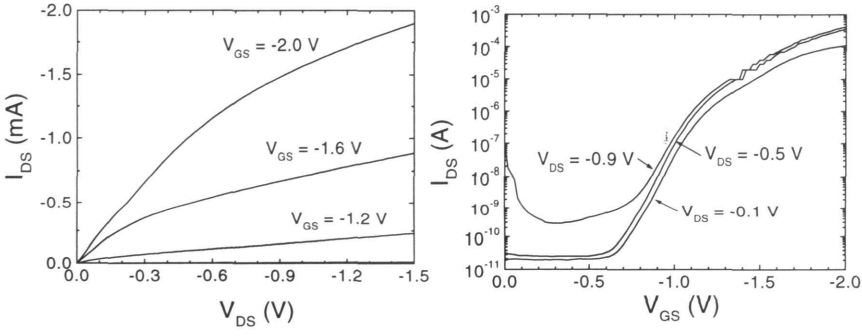


Fig. 6. Characteristics of long-channel (0.5 um) vertical p-channel MOSFET grown by RTCVD.

To achieve devices with short L, thin (10 nm) SiGeC regions were then incorporated above and below the doped S/D regions to suppress B diffusion. The high carrier concentrations in a FET make the effect of any bandgap offset negligible at room temperature. With this step to reduce diffusion of the source-drain dopant, devices with L down to 60 nm have been fabricated (Fig. 7). Further work is required to achieve a narrow pillar width in addition to the short channel length to realize the ultimate dual-gate MOSFET structures, however.

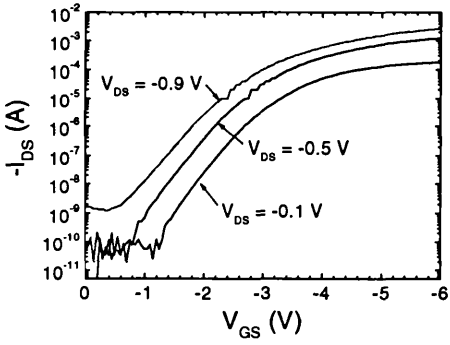


Fig. 7. Subthreshold I-V curves of L = 60 nm p-channel vertical FET with SiGeC diffusion barriers.

$Si_{1-x-y}Ge_xC_y$ Polycrystalline Gates

In early CMOS processes, the gate for both n-channel and p-channel devices was typically heavily doped n-type polycrystalline silicon. To achieve a reasonable low threshold voltage for the p-channel devices, it was then necessary to dope the channels p-type with boron to create buried channel devices. Because buried channel devices do not scale well to short channel lengths, in modern processes a p-type polysilicon gate (heavily doped with boron) is preferred for the p-channel devices so that a reasonable threshold can be achieved in surface channel devices. The n-channel devices still have an n-type gate. In such "dual-gate" processes, the diffusion of boron through the thin gate oxide is a substantial problem for device integration. If boron penetrates the thin gate oxide it results in a positive shift in the threshold voltage of the p-channel device. We therefore investigated the application of thin polycrystalline SiGeC blocking layers (20 nm) between the usual (0.4 um) polysilicon gate in structures with 8-9 nm gate oxides.

All polycrystalline layers were deposited undoped, and then the top polysilicon surface was implanted with 60 keV BF_2^+ at a dose of 5 x 10^{15} cm^{-2}, resulting in a boron profile approximately 0.1 um deep. The samples were then annealed at 900 °C for various times to drive the boron through the polycrystalline layers. The threshold voltage was then measured by C-V measurements on MOS capacitors (n-type substrates) to evaluate any shifts due to boron penetration through the gate oxide. The details are reported elsewhere [Chang, 1998], but one of the main results is presented in Fig. 8. It shows the threshold voltage as a function of anneal time for an all-Si control structure, and structures with either a SiGe or SiGeC blocking layer of 20 nm thickness. The superiority of the sample with the SiGeC blocking layer is clear. While boron penetration through the gate

oxide is effectively suppressed with the $Si_{1-x-y}Ge_xC_y$ blocking layer, quasi-static C-V measurements indicate that gate depletion did not occur for negative gate biases, indicating a high boron doping in the SiGeC layer, a result supported by SIMS. The seeming contradiction between the ability of the SiGeC to block boron penetration through the gate and its ability to be highly doped at the oxide interface is further addressed in other work [18].

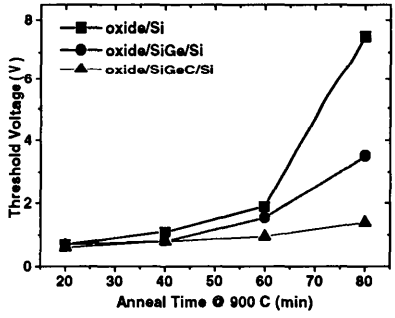


Fig. 8. Threshold voltage vs. anneal time for capacitors with different gate electrode structures: polysilicon gate; SiGe barrier layer + poly Si gate;, SiGeC barrier + poly Si gate.

Summary

Scaling MOSFET's to channel lengths deep below 100 nm requires careful control of diffusion and makes the investigation of novel FET structures attractive. In this paper the application of rapid thermal chemical vapor deposition to address such issues has been demonstrated through vertical FET structures (L down to 60 nm at present) and through the ability of SiGeC layers to greatly suppress boron diffusion in both bulk Si and in polycrystalline gate stack structures. Because of the ability of RTCVD to deposit a variety of high quality semiconductor and insulating layers with nanometer precision, further such applications are to be expected in the coming years.

Acknowledgments

The support of DARPA (ONR 66001-97-1-8904), ONR (N00014-96-1-0034), and the USAF AASERT program are greatly appreciated.

References

1. C.A. King, J.L. Hoyt, C.M. Gronet, J.F. Gibbons, M.P. Scott, and J. Turner, IEEE Elec. Dev. Lett. 10, 52 (1989).

2. J.C. Sturm, C.M. Gronet, C.A. King, S.D. Wilson, and J.F. Gibbons, IEEE Elec. Dev. Lett. **7**, 577 (1986).
3. T-J. King, J.R. Pfiester, J.D. Shott, J.P. McVittie, and K.C. Saraswat, Tech. Dig. IEDM, 253 (1990).
4. M. Cao, A. Wang, and K. Saraswat, J. Electrodchem. Soc. **142**, 1566, (1995).
5. D.T. Grider, M. C. Ozturk, S. P. Ashburn, J. J. Wortman, G. Harris, and D. Maher, J. Elec. Mat. **24**, 1369 (1995)
6. P.M. Garone, V. Venkataraman, and J.C. Sturm, IEEE Elec. Dev. Lett. **13**, 56 (1992).
7. K. Ismail, B.S. Meyerson, S. Rishton, J. Chu, S. Nelson, and J. Nocera, IEEE Elec. Dev. Lett. **13**, 229 (1992).
8. P.A.Stolk, D.J. Eaglesham, H.-J. Gossman, and J.M. Poate, Appl. Phys. Lett. **66**, 1370 (1995).
9. P.A. Stolk, H.J. Gossmann, D.J. Eaglesham, D.C. Jacobson, C.S. Rafferty, G.H. Gilmer, J. Jaraiz, J.M Poate, H.S. Luftman, and T.E. Haynes, J. Appl. Phys. **81**, 6031 (1997).
10. S. Nishikawa, A. Tanaka, and T. Yamaji, Appl. Phys. Lett. **60**, 2270, (1992).
11. I. Ban, M.C. Ozturk, E.K. Demirlioglu, IEEE Trans. Elec. Dev. **44**, 1544 (1997
12. J.L. Regolini, F. Gisbert, G. Dolino, and P. Boucaud, Materials Lett. **18**, 57 (1993).
13. A. St. Amour, C.W. Liu, J.C. Sturm, Y. LaCroix and M.L.W. Thewalt, Appl. Phys. Lett. **67**, 3915 (1995).
14. C.L. Chang, A. St. Amour, and J.C. Sturm, Tech. Dig. Int. Elec. Dev. Mtg, 257 (1996).
15. C.W. Liu, A. St. Amour, J.C. Sturm, Y.R.J. Lacroix, M.L.W. Thewalt, C.W. Magee, and D. Eaglesham, J. Appl. Phys. **80**, 3043 (1996).
16. L.D. Lanzerotti, J.C. Sturm, E. Stach, R. Hull, T. Buyuklimanli and C. Magee, Appl. Phys. Lett. **70**, 3125 (1997).
17. D. Frank, S.E. Laux, and M.V. Fischetti, Tech. Dig. IEDM, 553 (1992).
18. C.L. Chang and J.C. Sturm, Proc. Symp. Mat. Res. Soc. **525**, to be published (1998).