Proceedings of the 18th International Conference on Amorphous and Microcrystalline Semiconductors (ICAMS 18)
Snowbird, Utah, Aug. 23-27, 1999

ELSEVIER

Journal of Non-Crystalline Solids 266–269 (2000) 1284–1288

JOURNAL OF NON-CRYSTALLINE SOLIDS

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High-performance polysilicon thin film transistors on steel substrates

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Abstract

We fabricated thin film transistors in polycrystalline silicon on steel substrates. The polycrystalline silicon films were made by thermally annealing hydrogenated amorphous silicon precursor films, which had been deposited on stainless steel coated with ~0.5 μm thick 810°C-annealed SiO_2. We employed annealing temperatures ranging from 600°C, which is the furnace annealing temperature limit for conventional glass substrates, to 750°C. Films were crystallized at 650°C in 1 h with 1-h hydrogen plasma seeding, at 700°C in 10 min either with or without hydrogen plasma seeding, and at 750°C in 2 min. The best top-gate transistors were made from films crystallized at 650°C and had an average electron field-effect mobility of 64 cm^2/V s in both the linear and saturated regimes. Thus steel substrates permit a substantial reduction in crystallization time over conventional glass substrates, and produce polycrystalline silicon with an electron mobility greater than other substrates.

1. Introduction

The fabrication of the thin film transistor (TFT) backplane is an important part of the manufacture of active matrix liquid crystal displays (AMLCDs) [1]. The current TFT technology is based on hydrogenated amorphous silicon (a-Si:H), and has not been used for driver circuits because of the electron mobility in a-Si:H [2]. Polycrystalline silicon (polysilicon) TFTs are used in display backplanes because they allow integrating the matrix switches with the driver circuits [3], owing to n- and p-channel operation and larger carrier mobilities. These mobilities enable smaller TFTs with current >100 μA when on and switching frequency >4 MHz, and the capability of forming n- and p-channel devices and thus complementary metal-oxide-semiconductor (CMOS) circuits, which allow low power <1 mW consumption applications. The polysilicon formed by crystallization of a-Si:H has electrical properties that are better for devices to those of directly deposited polysilicon due to larger grains [4]. The common crystallization techniques are furnace annealing [5], or rapid thermal annealing by lamp heating [6], or laser annealing [7]. Furnace annealing is preferred, as it is isothermal and thus produces uniform transport properties over the entire glass substrate [8]. Because the strain points of affordable glass substrates lie just above 600°C [9], furnace crystallization of a-Si:H on glass substrates is restricted to 600°C or less, and conventional furnace crystallization at 600°C takes approximately one day [10]. Catalyzed [11] and pre-anneal seeding [12–14] approaches can cut this time to ~5 h, which still is

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0022-3093/00/$ - see front matter
PII: S0022-3093(99)00938-2

long when compared to the throughput of one plate per minute desired of the single-substrate cluster tools employed in the manufacture of AMLCDs [8]. Very small AMLCDs have been made with polysilicon films on substrates of quartz glass, which allows higher temperature processes [15], but quartz glass substrates are expensive. Therefore it is necessary to find a new way to fabricate TFTs in short times with acceptable and uniform performance on large and low-cost substrates [1]. This is the goal of experiments with steel substrates. Of course, steel substrates are opaque, and therefore can be used only with emissive or reflective displays.

Previous work with steel foil substrate has been limited to amorphous silicon TFTs (electron mobility $\sim$1 cm^2/V s) at temperatures $\leqslant$350°C [16,17], and only very recently has expanded to laser annealed [18] and furnace annealed [19] polysilicon TFTs. In the work described here, we made TFTs with the polysilicon films on steel substrates. The polysilicon was made by the crystallization of a-Si:H by furnace annealing at temperatures up to 750°C.

2. Experiments

200-μm thick foils of AISI grade 304 stainless steel (Fe/Cr/Ni 72/18/10 wt%) were cleaned with acetone and methanol. Then a 210-nm thick film of spin-on glass was applied to both sides, and a 270-nm thick film of SiO_2 was deposited on both sides by plasma-enhanced chemical vapor deposition (PECVD) at 250°C. The substrates then were heated from 450°C to 810°C at a rate of 5°C/min. Next, a 160-nm thick precursor film of a-Si:H was deposited at a substrate temperature of 150°C, and was furnace-annealed for crystallization. We employed four different annealing processes to reduce the crystallization time: (a) the film was exposed for 1 h to a hydrogen discharge to induce seeding [12–14] and then was annealed at 650°C for 1 h; (b) the film was annealed at 700°C for 10 min after the 1 h hydrogen discharge seeding; (c) the film was annealed at 700°C for 10 min without hydrogen plasma exposure; (d) the film was annealed at 750°C for 2 min after the 1 h hydrogen discharge seeding. The progress and completion of crystallization was monitored by measuring the ultraviolet reflectance at $\lambda = 276$ nm [5,6], with the times above being the minimum required for crystallization of the films [20]. These crystallization times are consistent with an activation energy of 2.7 eV for crystal growth in the a-Si:H precursor films when exposed in a hydrogen discharge for seeding, or of 3.7 eV for nucleation in untreated a-Si:H films, respectively [14]. The electrical conductivities in the dark of all polysilicon films were measured to determine possible doping by contamination from the metal substrate. The conductivities of polysilicon on steel substrates are 10^{-6} to 10^{-5} S cm^{-1} at room temperature with a thermal activation energy of $\sim$0.53 eV, compared to $\sim 10^{-6}$ S cm^{-1} for intrinsic polysilicon on glass [21]. We also tested the oxide-coated substrate by making bottom-gate amorphous silicon TFTs (without crystallization) with the same structure as the low temperature process [16,17]. The performance of these test transistors of a-Si:H made at 250–300°C, and the conductivities of the polysilicon films were those that we expected if the silicon films were not contaminated by the steel substrate. Therefore, we proceeded to make TFTs of the polycrystalline layers.

Because we wanted our initial TFTs to measure the quality of the polysilicon films after the recrystallization process, all post-crystallization processing was done at temperature <350°C. Thus a non-self-aligned process with a maximum process temperature of 350°C was used instead of the conventional self-aligned process, which requires an annealing at >600°C after ion implantation of the source/drain dopant. Fig. 1 shows a schematic cross-section of a top-gate polysilicon TFT made on steel. On top of the crystallized silicon layer, 75-nm thick n^+ microcrystalline silicon (μc-Si) was deposited at 350°C to serve as the eventual source/drain. Then the original polysilicon layer was patterned into TFT islands by reactive ion etching (RIE), and the n^+ μc-Si was patterned by another RIE step. Next, a 200-nm thick gate oxide was deposited by PECVD at 250°C, followed by a wet etch to open the source/drain contact windows. 200-nm of aluminum was thermally evaporated and then patterned by wet etch to form the gate

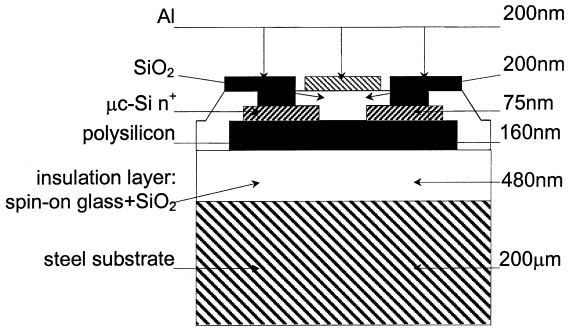

Fig. 1. Schematic cross-section of a polysilicon top-gate transistor on a passivated steel substrate, showing materials used and their thickness.

and source/drain contacts. The final step in the TFT fabrication was a 15-minute-long anneal at 250°C in a hydrogen (15 vol.%)/nitrogen (85 vol.%) mixture. This source/drain process is not practical for short-channel TFTs with smallest parasitic resistance, but is sufficient to evaluate the mobility in long channels. The relatively larger parasitic source/drain resistance in our structure does not affect the current and the extracted mobility. The channel is 45 μm long and 180 μm wide. We use such large dimensions because we print our masks with a high-resolution laser printer.

3. Results and discussion

The TFT samples were evaluated with a parameter analyzer (HP 4155A). All measurements were made with the steel foil grounded. Fig. 2 shows (a) transfer and (b) output properties. Fig. 2(a) includes a sample made of polysilicon crystallized at 650°C with hydrogen plasma seeding, a sample of 700°C polysilicon, and another without hydrogen plasma seeding. The transistor sample of Fig. 2(b) was made from the 650°C polysilicon including seeding, which had the largest average electron field effect mobility. Transistors for all three annealing conditions had well-behaved properties. Table 1 lists the principal properties of all samples made from films crystallized at all four processes. The threshold voltage and electron field effect mobility in the linear regime were extracted from the linear plot of drain source current, I_{ds}, vs

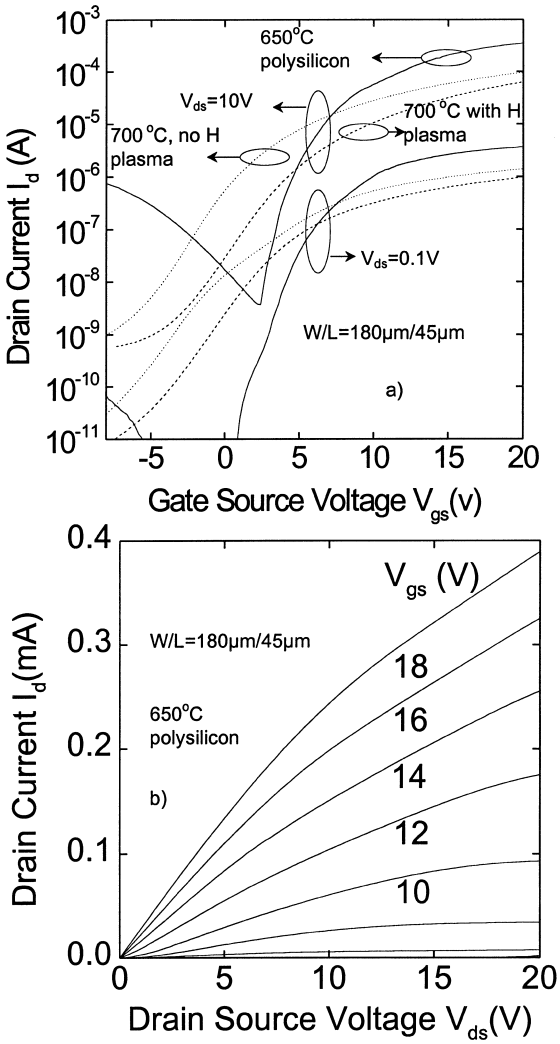

Fig. 2. (a) Transfer properties of samples made with polysilicon crystallized at 650°C after hydrogen plasma exposure and at 700°C with/without hydrogen plasma exposure; and (b) output of a transistor made with 650°C polysilicon on steel.

gate source voltage, V_{gs}, with drain source voltage, $V_{ds} = 0.1$ V, and the electron field effect mobility in the saturated regime was obtained from a plot of $I_{ds}^{1/2}$ vs V_{gs} at $V_{ds} = V_{gs}$. The largest average mobility of 64 cm^2/V s, observed both in the linear and saturated regimes, was obtained for crystallization at 650°C. One device had a mobility of 85 cm^2/Vs. This mobility is near the maximum for furnace-annealed material [8]. Typical threshold voltages and subthreshold slope (with 10 V V_{ds})

Table 1
Electrical characteristics of the polysilicon thin film transistors made on steel substrates. All electrical measurements are an average from $\geqslant 10$ devices.

Temp. of crystallization (°C)	Time of crystallization (min)	Hydrogen plasma exposure (h)	Polysilicon conductivity σ^a (S/cm)	UV reflectance ΔR^b (%)	ON current I_{ON} [c] (A)	OFF current I_{OFF} [d] (nA)	I_{ON}/I_{OFF}	Threshold voltage [e] (V)	Subthreshold slope [f] (V/decade)	Electron mobility (linear) (cm^2/V s)	Electron mobility (saturated) (cm^2/V s)
650	60	1	2.0×10^{-6}	6.2	$3.8 \times 10^{-4} \pm 0.2$	2.1 ± 1.7	$\sim 10^5$	7.2 ± 1.8	0.4 ± 0.3	63 ± 11	64 ± 11
700	10	1	0.8×10^{-6}	5.5	$5.9 \times 10^{-5} \pm 0.9$	0.59 ± 0.5	$\sim 10^5$	8.0 ± 3.7	1.8 ± 0.7	13 ± 3.5	20 ± 4
700	10	none	1.3×10^{-6}	5.5	$8.8 \times 10^{-5} \pm 1.1$	0.63 ± 1.9	$\sim 10^5$	4.8 ± 1.3	2.1 ± 0.3	13 ± 0.4	13.5 ± 1.1
750	2	1	1.4×10^{-6}	6	$3.8 \times 10^{-5} \pm 0.2$	0.69 ± 2.6	$\sim 10^5$	7.4 ± 1.4	2.7 ± 0.2	8.6 ± 0.9	10.6 ± 1.3

[a] At 300 K.
[b] UV reflectance difference from a-Si:H at 276 nm, for silicon wafer $\Delta R = 7.5\%$.
[c] At $V_{gs} = 20$ V, $V_{ds} = 10$ V.
[d] At $V_{ds} = 10$ V.
[e] At $V_{ds} = 0.1$ V.
[f] At $V_{ds} = 10$ V.

are 7.2 V and 0.4 V/decade, respectively, for the 650°C samples. Note that the minimum off currents with $V_{ds} = 10$ V are in the 10^{-9} A range, independent of the annealing processes, and this current is comparable to the off currents of TFTs on glass substrates [22,23]. This off current is important, we suggest, because the polycrystalline films and carrier generation lifetimes are not adversely affected by metal contamination from the substrate. For all four annealing processes, the threshold voltages lie in the range of 4–10 V. The mobilities were less and subthreshold slopes were larger in the samples annealed at 700°C and 750°C than those annealed at 650°C (Table 1). For example, the mobility for the 700°C sample was ~13–20 cm^2/V s, comparable to the mobilities of the polysilicon TFTs made on quartz glass substrate [24]. We assume these mobilities are due to the faster increase of the nucleation rate than of the crystal growth rate as the temperature increases [25,26], therefore the average grain size becomes smaller. Note that the differential thermal expansion between the SiO_2 passivation layer ($\alpha = 18 \times 10^{-6}$), the TFT materials ($\alpha = 4 \times 10^{-6}$), and steel ($\alpha = 4 \times 10^{-6}$) [17,27], does not seem to pose a systematic problem. A very attractive feature to us of steel foil substrates is their ruggedness and flexibility [17,27]. Therefore based on our results, we suggest that steel substrate can furnish rugged TFT backplanes with good performance.

4. Summary

Polycrystalline silicon thin-film transistors were fabricated on steel substrates with process temperatures >600°C. By tolerating higher temperature, the steel foil makes possible a reduction in furnace annealing time compared to that on glass substrates. Transistors made from 650°C material have electron field effect mobilities that are comparable to the largest reported for furnace-crystallized polysilicon on glass substrates. Leakage currents are not adversely affected by contamination from the steel substrate. The technology of polysilicon film on steel opens a new route to high throughput manufacturing of thin film transistors

with uniform characteristics on large-area, low-cost and rugged substrates.

Acknowledgements

This research is supported by DARPAs HDS and MLP programs. Ming Wu thanks the Princeton Plasma Physics Laboratory for a summer stipend.

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