Society for Information Display International Symposium, San Jose, CA, May 16-21, 1999

A Polysilicon Active Matrix Organic Light Emitting Diode Display with Integrated Drivers

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Abstract

The design of an active matrix organic light emitting diode (AMOLED) display using a polysilicon thin film transistor pixel is described. Characteristics of the OLED response in the low current regime are described and their impact on the design of integrated driver circuitry is discussed. Integrated data and select scanners which generate the signals necessary for data capture and pixel calibration are presented.

Introduction

Organic light emitting diodes (OLEDs) are presently of great interest due to their potential application in high efficiency displays.[1] One application for these devices is as the light emitting component in a passively addressed display. However, the time available to drive each pixel rapidly decreases with the number of rows, driving up the peak brightness levels and causing the row line currents to rise. It was determined that a peak brightness of 72,000 nits was necessary to achieve a split addressed, VGA display with a mean luminance of 300 nits. This translated to a peak current of 1.6 Amps on the row lines.[2] These huge currents cause large voltage drops in the row lines and push the OLED operation to higher voltages where they are less power efficient.[2] Driving the OLEDs with an active matrix leads to lower voltage operation, lower peak pixel currents, and a display with much greater efficiency and brightness. Since the brightness is proportional to the current driven through the OLED, the role of the active matrix is to provide a constant current throughout the entire frame time, eliminating the high currents encountered in the passive matrix approach.

Two primary issues were encountered during the active matrix OLED display design. First, the polysilicon thin film transistors suffer from large device to device variations due to the nature of the polysilicon crystal growth, making it difficult to generate a uniform current source at each pixel. A four transistor, autozeroing pixel that eliminates the effects of transistor threshold voltage variations was developed to overcome this issue.[3] Secondly, measurements showed that the OLEDs respond slowly to the low currents encountered in the active matrix mode of operation, mainly due to the large parallel plate capacitance created by the thin OLED layers sandwiched between the anode and cathode conductors.[4] The response of the OLEDs in the active matrix mode of operation and its impact on the display design will be described and an overall description of the integrated scanner design used to drive the four transistor, autozeroing pixel will be presented.

Four Transistor Autozeroing Pixel

The four-transistor pixel with its timing diagram is shown schematically in Figs. 1 and 2. An in depth description of this pixel is provided elsewhere[3,4], but to understand the display timing presented in the next sections, the pixel is included here.

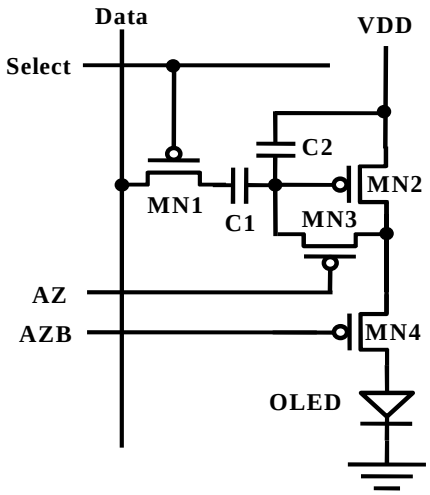

Fig. 1. Voltage programmed OLED pixel.

ISSN0099-0966X/99/3001-0180-$1.00 + .00 (c) 1999 SID

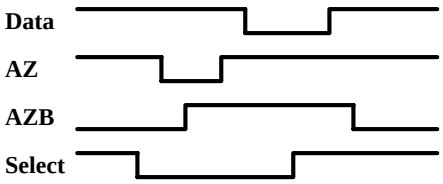

Fig. 2. Voltage programmed OLED pixel timing.

OLED Driven by an Active Matrix

The characteristics of the two transistor active matrix pixel of Fig. 3 are determined by the parallel plate capacitance of the OLED and the transistor connected in series with the OLED which acts as a current source. For a 200 µm x 100 µm pixel at typical luminance levels of 100 nits, the transistor current is only a few microamps. The capacitance for both the small molecule and polymer diodes is approximately 25 nF/cm^2, so a typical capacitance for a 200 µm x 100 µm pixel is 5 pF. A simple illustration of the impact of the large parallel plate capacitance is that it takes about 8 usec for a 3 µA current to charge 5 pF through 5 volts. This illustration shows that the time constant associated with charging the OLED parallel capacitance is large. Two other effects occurring in the OLEDs cause these time constants to increase still further. First, as the

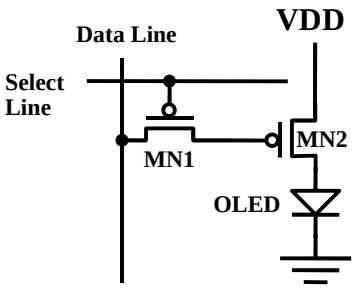

Fig. 3. Sample and Hold Active Matrix OLED Pixel.

OLED is turned on, much of the current flows directly through the diode rather than charging the parallel capacitance. The second is that the 3 µA currents are for peak brightness levels and that for lower levels, the currents are much smaller with correspondingly longer charging times. These two factors cause the OLED capacitance charging time constants to increase well beyond a row time which for a VGA display is 31.7 usec. The impact of the parallel capacitance was investigated to determine the actual charging times and their effect on the luminance response. A polysilicon transistor with dimensions W/L=400/4 µm was connected in series with a 0.1 cm^2 OLED and the current through the transistor, voltage across the OLED, and OLED luminance were measured. The voltage was measured with a high impedance Picoprobe, model 18B, to avoid discharging the diode through the oscilloscope input impedance.

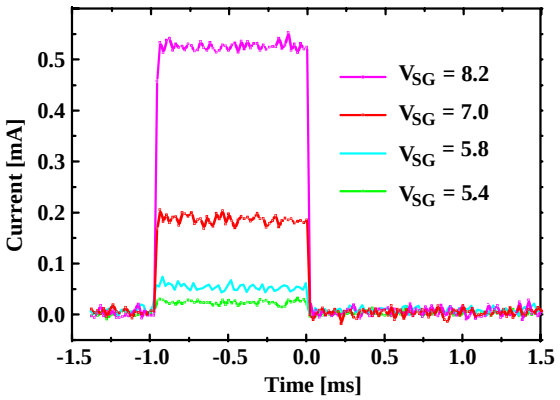

Fig. 4. Transistor current passed through a 0.1 cm^2 OLED at gate to source voltages of 5.4, 5.8, 7.0 and 8.2 V.

The polysilicon transistor acts as a constant current source, providing no surge of current to charge the OLED capacitance when turned on. This is demonstrated in Figs. 4 and 5 where the constant current provided by the transistor and the voltage across the OLED are plotted versus time for different transistor gate biases. The slow increase of the OLED voltage is shown in Fig. 5 where the rate of increase in the voltage decreases with decreasing current. The figure shows that the voltage response time of the device is several hundred µsec, indicating that the two effects mentioned above cause a significant increase in the charging times compared to a simple parallel plate capacitor charged with a constant current. The impact of the slow charging of the OLED on the luminance output is demonstrated in Fig. 6 where the normalized luminance initiates quickly for the higher current conditions while it turns on more slowly for the low current cases. Also apparent in Fig. 6 is the slow extinction of the luminance at lower current levels. When the transistor is turned off, the OLED must discharge it's own parallel capacitance. The initial discharge is rapid since the diode is turned on, but as the diode current drops into the subthreshold regime, the diode resistance increases exponentially and the discharge

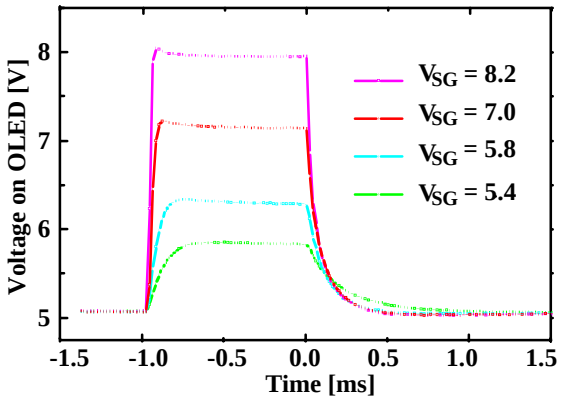

Fig. 5. OLED voltage when driven by a polysilicon TFT with gate to source voltages of 5.4, 5.8, 7.0 and 8.2 V.

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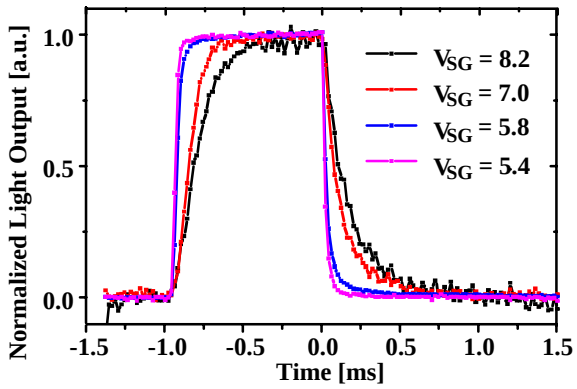

Fig. 6. OLED normalized light emission for polysilicon TFT gate to source voltages of 5.4, 5.8, 7.0 and 8.2 V.

slows. This effect is also evident in Fig. 5 where the voltage of the OLED decays rapidly after the transistor is turned off, but then the voltage decay slows as the diode turns off. The slow response of the OLED at low drive currents requires a different approach to an active matrix OLED display design compared to a passively addressed display. The OLED parallel capacitance and its slow charge and discharge through either the pixel transistor or through the diode itself forces the display designer to reconsider pixel programming techniques. The voltage across the OLED may not settle in the time available to load data into a pixel; and autozero cycles used to calibrate the data against the transistor and OLED threshold voltages may be ineffective due to the long settling times.

Display Timing

These effects were overcome in the present display design by selecting each row in the row time prior to the programming row time so the pixels turn off one row time prior to autozeroing and programming. This allows the OLED parallel plate capacitance to discharge through the organic diode, ensuring that the voltage across the diode is low enough to enable the autozero cycle. The autozero cycle relies on being able to pull the gate of MN2 down and then discharging the gate through the autozero device, MN3. If the OLED parallel plate capacitance is not discharged prior to the autozero cycle, the voltage at the drain of MN2 may be higher than the gate of MN2 and the autozero cycle will not calibrate against the threshold voltage of MN2. Turning off the pixel in the previous row time allows the OLED to discharge, ensuring that the drain of MN2 is lower than the gate of MN2 when the autozero cycle begins. The select signal now has two pulses, one to turn off the pixel to allow the OLED voltage to decay and a second pulse, one row time later, to program the row of pixels. A side effect of this mode of operation is that the select pulses are not identical for each row time, so odd and even rows must be driven differently. This is shown in the timing diagram, Fig. 7, where odd row and even row signals are necessary for SEL, AZ and AZB.

The timing diagram of Fig. 7 shows the relationship between the data logic signals and the select logic signals. The display row time is divided into two portions, the autozero section labeled Row #X AZ and the data loading section labeled Row #X DATA. The autozeroing of the four transistor pixel is performed during the AZ portion of the row time and the pixels are programmed during the DATA portion of the row time. Note that the select signals, SEL_ODD and SEL_EVEN consist of two pulses, T1 and T2. For each row, T1 occurs first, loading zero data into the pixel and discharging the OLED. The second pulse, T2, turns the select transistor on again and data is loaded during the DATA portion of the row time. For this particular design, a standard, 160 output AMLCD data

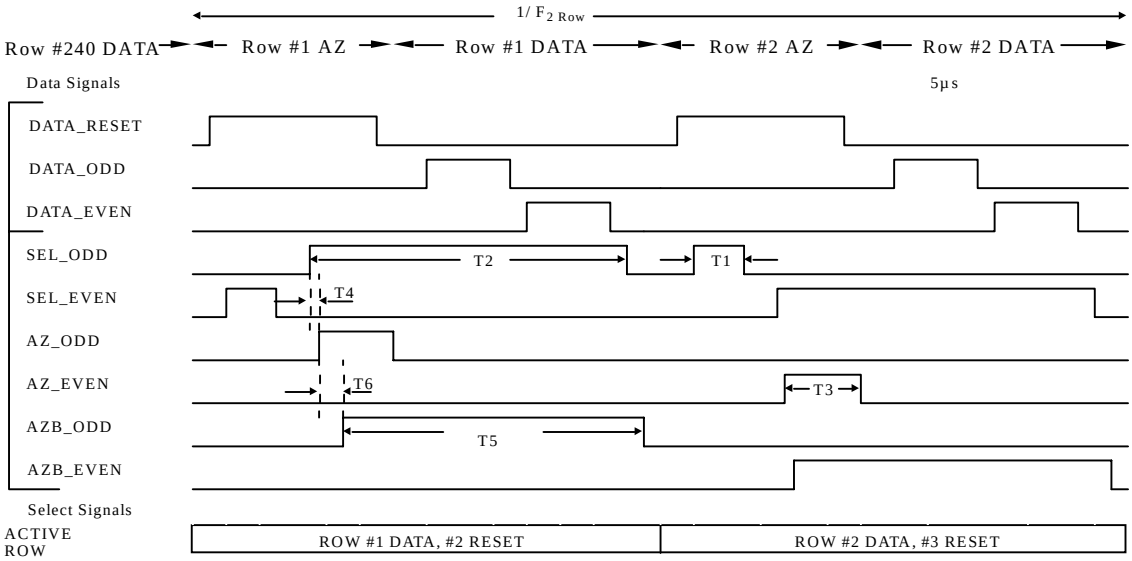

Fig. 7. Logic Timing Diagram for the QVGA AMOLED Display. SEL, AZ and AZB have even and odd signals.

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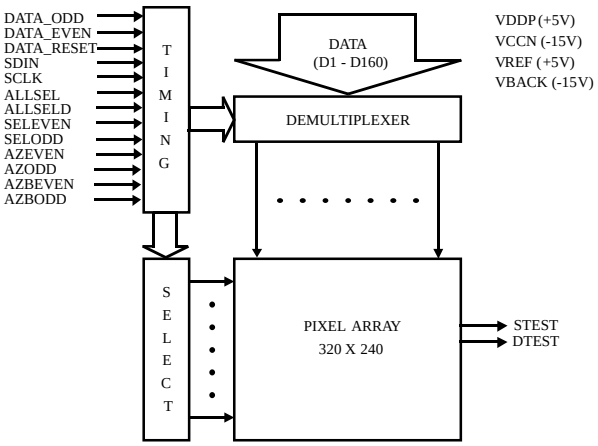

Fig. 8. QVGA display circuit block diagram

driver chip was used to provide data to the display and the data demultiplexer places data on odd and even data lines during the DATA ODD and DATA EVEN pulses, respectively.

An overall block diagram of the display is shown in Fig. 8. One hundred and sixty data lines feed data and are demultiplexed onto the 320 columns. The logic signals include the data demultiplexing control signals; the select scanner trigger and clock; the select (SEL), autozero (AZ) and autozero bar (AZB) signals; two ALLSEL signals to allow for frame at a time programming; two test signals, STEST and DTEST; and power supplies. The logic block level shifts all logic signals from [5, 0] volts to [5, -15] volts, so the display has a completely 5 volt interface except for the negative power supply. The logic block also generates all additional clocks necessary to drive the select circuit which is a shift register that controls pass gates for each of the select control signals, SEL, AZ and AZB.

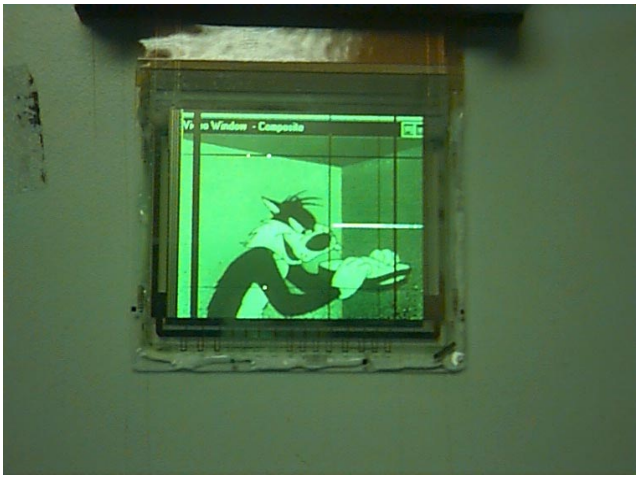

Fig. 9. QVGA Display showing video operation.

Conclusions

The electrical and optical responses of organic light emitting diodes at the voltage and luminance levels encountered in an active matrix display were characterized. The parallel plate capacitance of the OLED becomes an important issue due to its large size and the relatively long times required to charge it with the pixel current. These long charging times were taken into consideration in the design of an active matrix OLED pixel with results shown in Fig. 9. The figure shows a QVGA display with the four transistor, autozeroing pixel. The first prototypes are being operated with excellent uniformity and demonstrate that the four transistor pixel combined with an additional select pulse to discharge the OLED capacitance prior to the autozero cycle provide the uniformity necessary for high information content displays.

Acknowledgments

This work is supported by Bruce Gnade of the Defense Advanced Research Projects Agency (DARPA) under contract F33615-96-2-1944 monitored by Gurdial Saini and Darrel Hopper of Wright Laboratory, Displays Branch

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