CONFERENCE PROCEEDINGS

LEOS '98

11TH ANNUAL MEETING

IEEE Lasers and Electro-Optics Society
1998 Annual Meeting
1 - 4 December 1998

Volume 1
Tuesday - Wednesday
1 - 2 December 1998

The Walt Disney World
Swan Hotel
Orlando, Florida

IEEE CATALOG NUMBER: 98CH36243
ISSN: 1092-8081

4:45pm - 5:00pm
TuO4

Annual Meeting of the Lasers and Electro-Optics Soc. (LEOS)
Orlando, FL, Dec. 1-4, 1998

Amorphous Silicon TFT Active-Matrix OLED Pixel

M.H. Lu, E. Ma, J.C. Sturm, and S. Wagner,
Center for Photonics and Optoelectronic Materials (POEM), Department of Electrical Engineering, Olden Street, Princeton University, Princeton, NJ 08544, USA

Organic light emitting devices (OLED) have attracted enormous attention because of their potential flat panel display applications[1]. Active-matrix addressing is attractive for high information content displays. There are several developmental efforts in this area based on polysilicon TFT technology[2]. However, there is no commercial low temperature ($\leq$ 600°C) polysilicon manufacturing facility. In this paper, we report the fabrication of a video-brightness, active-matrix OLED (AMOLED), two-transistor-pixel based on amorphous silicon (a-Si) TFT technology, with a maximum process temperature of 350°C. The process should be compatible with existing a-Si TFT manufacturing for AMLCDs.

The schematic diagram of this pixel is presented in fig. 1, with signal timing similar to that in AMLCD displays. The fabrication process starts with glass substrates pre-coated with 15 Ω /□ ITO. First, the ITO is lithographically patterned and covered with a passivation SiNx. A-Si TFTs with Damascene gates[3] are fabricated by a back channel-etch process in which contact holes to the gate of T1 and ITO are opened prior to source/drain metal deposition. Another SiNx passivation layer is deposited, after which contact holes to the patterned ITO are opened. After treating the surface with an O_2 plasma[4], a single PVK/PBD/C6 layer is spin-coated, followed by Mg:Ag (10:1) as OLED cathodes[5] (fig. 2). Note the use of glass substrates pre-coated with ITO eliminates the need of depositing ITO after TFT fabrication. Since optimum ITO is typically deposited at around 350°C, depositing ITO after TFT fabrication will invariably cause de-hydrogenation of the TFTs.

The typical TFT has a saturation mobility of 0.5-0.6 cm^2/Vs, a V_T of 2.5 V and an on/off ratio of 10^6 - 10^7 (fig. 3). Before OLED integration, the source of T2 is grounded in a DC measurement to demonstrate the basic sample and hold function of the pixel. The I_{pixel} vs. data plot (fig. 4) clearly demonstrates the transistor square law characteristics. After OLED integration, the operation of the pixel is demonstrated by driving a single pixel with signal timing consistent with VGA operation (fig. 5). Pixel luminance varies with Data as expected. The measured integrated OLED external quantum efficiency is 1% (3 Cd/A). Video brightness (100 Cd/m^2) averaged over entire pixel can be achieved with V_{OLED} = -10 V, V_{DD} = 25 V, and Data $\approx$ Select = 30 V.

Our TFT process used large linewidth (10 μm) that limited the W/L which could be fit into a single pixel. Assuming typical 2-3 μm linewidths as in AMLCD processes, W/L for T2 in excess of 25 is reasonable. Combined with state of the art OLED efficiencies, transistor gate and drain voltages $\leq$ 5V appear entirely feasible (fig.6). This work shows a-Si TFT technology is an attractive alternative for low voltage AMOLED displays. This work is supported by DARPA and NSF.

1. C.W. Tang, Infor. Disp., **12**, 16, (1996).
2. R. Dawson et al., "Design of an improved pixel for a polysilicon active-matrix organic LED Display", SID'98 Digest, 11 (1998).

0-7803-4947-4/98/$10.00 ©1998 IEEE

3. E. Ma, S. Wagner, "Damascene-Gate Thin Film Transistors", presented at IEEE Device Research Conference, June, 1998.
4. C.C. Wu, C.I. Wu, J.C. Sturm, and A. Kahn, Appl. Phys. Lett. **70**, 1348 (1997).
5. C.C. Wu et al., IEEE Trans. Elec. Dev, **44**, 1269-81 (1997).

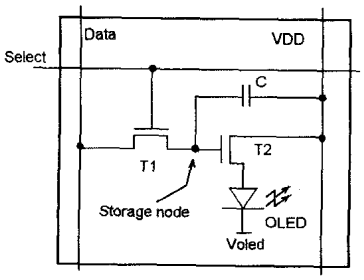

Fig. 1. Circuit diagram of the pixel. T1: switching transistor, W/L = 10/10 μm; T2: driving transistor, W/L = 80/10 μm; C: storage capacitor.

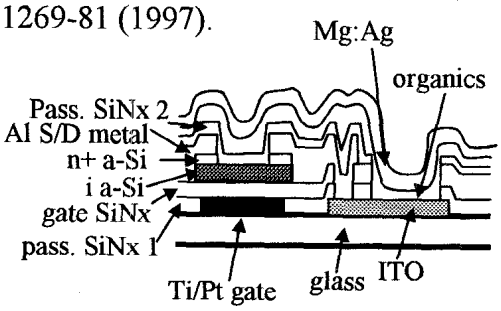

Fig.2. Cross-section of T2 and OLED. Pixel area = 250 x 250 μm^2, OLED fill factor = 40%.

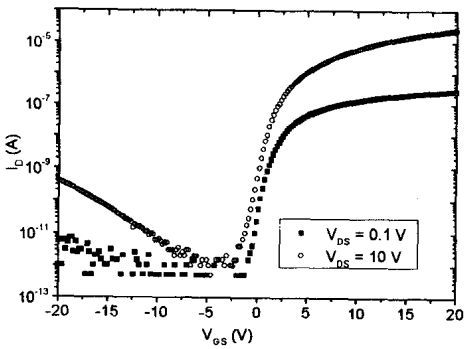

Fig. 3. Typical TFT, W/L = 80/10 μm.

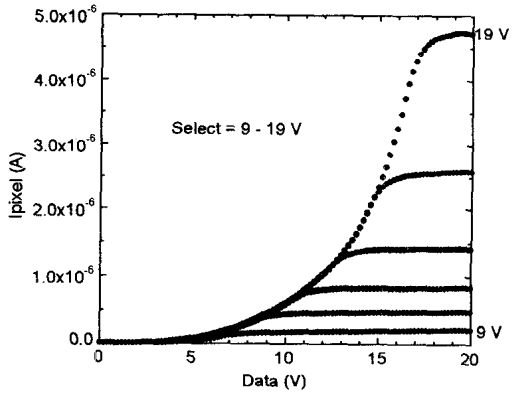

Fig. 4. Pixel driving current as a function of data and select voltages (T2 source grounded).

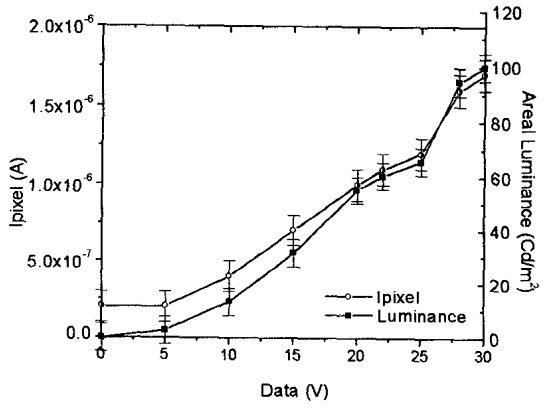

Fig. 5. Pixel luminance as a function of Data voltage, V_{DD} = 25 V, V_{OLED} = -10 V, Select = 30 V for VGA timing sequence.

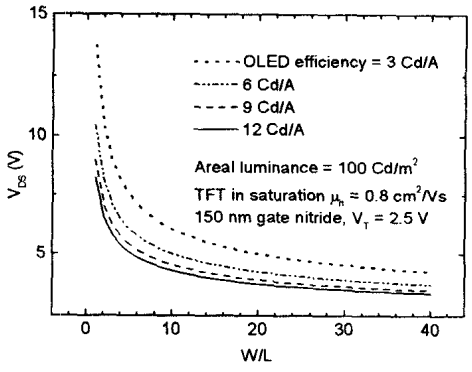

Fig. 6. Calculated V_{DS} as a function of T2 W/L ratio for various OLED efficiencies.