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**ELECTRON
DEVICES**
meeting

1999

5.5

WASHINGTON, DC
DECEMBER 5-8, 1999

ieed

TECHNICAL DIGEST

High temperature polycrystalline silicon thin film transistor on steel substrates

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Abstract

Polycrystalline silicon thin film transistors were fabricated using both self-aligned and non-self-aligned structures on 0.2 mm steel foil substrates coated with 0.5 μm SiO_2 . The polycrystalline silicon was formed by furnace crystallization of PECVD hydrogenated amorphous silicon films at temperatures from 600 to 950°C. The corresponding annealing times at high temperature can be as short as 20 seconds. No evidence is found for transistor contamination by the steel with drain current on/off ratio of $\geq 10^5$ in all cases. The short crystallization times achievable on steel substrates provide a considerable advantage over glass substrates, which require crystallization times of ≥ 6 hours because of their strain temperatures of $\sim 600^\circ\text{C}$. Our results lay the groundwork for polycrystalline silicon transistor roll-to-roll technology on continuous web.

Introduction

Present active matrix liquid crystal display (AMLCD) backplanes are either hybrids of an amorphous silicon thin film transistor (TFT) matrix on glass and separate silicon IC drivers, or integrated matrix and driver circuits of polycrystalline silicon on one glass plate. The polysilicon is made by crystallization of an amorphous silicon precursor film, as this approach creates better TFT performance than directly deposited polysilicon [1,2]. Recrystallization techniques [3] include furnace annealing [4], rapid thermal annealing by lamp heating [5], and laser crystallization [6,7]. Furnace annealing produces high uniformity over large area, and substrates of glass instead of fused quartz keep cost low. The glass substrates have strain points of $\sim 600^\circ\text{C}$ [8], which limit the thermal budget for polysilicon preparation and processing. At 600°C the crystallization time can be as long as 20 hours. Catalyzed crystallization can reduce this time to ~ 5 hours [9,10,11], which still is much longer than the AMLCD manufacturing requirement of 1 minute per backplane fabrication step [3]. A fast, furnace based process is needed for fabricating polysilicon TFTs over large areas of low cost substrates such as in a roll-to-roll web process. This was our and other recent researchers' [12] motivation for experimenting with steel substrates, which we discovered to support surprisingly high crystallization temperatures. (Recently, steel substrates also have been employed for laser crystallized silicon [13].) By virtue of working with 0.2 mm

thick substrate foils we also investigated the feasibility of continuous web processing.

Raising the crystallization temperature raises the crystal nucleation rate and the crystal growth rate exponentially, so that the crystallization time is reduced dramatically. The rate of nucleation has a higher activation energy than the rate of crystal growth [14,15]. Thus, raising the crystallization temperature above 600°C increases the number of nuclei, reduces their size, and reduces the field effect mobility. However, above a sufficiently high temperature the rate of nucleation begins to drop because of the size of the critical nucleus grows. This is our rationale for exploring two regimes of crystallization temperature. Between 600°C and 800°C the nucleation rate increases faster with rising temperature than the growth rate. At temperatures somewhere above 850°C the nucleation rate is expected to drop, while the growth rate keeps increasing, so that with increasing temperature the grain size and hence the field effect mobility are expected to rise again.

Experiments

A. Substrate preparation

200- μm thick foils of AISI grade 304 stainless steel (Fe/Cr/Ni 72/18/10 wt.%) were cleaned with acetone and methanol. To reduce the roughness of the steel foil surface, a 210-nm thick film of spin-on glass was applied to both sides. Then a 270-nm thick film of SiO_2 was deposited on both sides by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 250°C . The $\sim 0.5\mu\text{m}$ thick insulation layer reduced the roughness from 5nm for bare steel foil to $< 2\text{nm}$. A 160-nm thick precursor film of a-Si:H was deposited by PECVD at a substrate temperature of 150°C .

B. Low temperature (600°C - 750°C) crystallization

After exposing a-Si:H precursor films to a hydrogen discharge for 1 hour to induce nucleation, the films were crystallized at one of four different annealing temperatures: (a) 600°C for 6 hours; (b) 650°C for 1 hour; (c) 700°C for 10 minutes; and (d) 750°C for 2 minutes. These crystallization times are consistent with an activation energy of 2.7eV for crystal growth in the a-Si:H precursor films, after exposure to a hydrogen discharge for pre-seeding [11]. The progress and completion of crystallization was monitored *ex situ* by measuring the ultraviolet reflectance at $\lambda = 276\text{nm}$ [4,5].

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C. High temperature crystallization (950 °C)

The a-Si:H precursor film was pushed into a furnace tube heated to 950°C, in flowing nitrogen gas. After 20 seconds, the film was pulled into the ~500°C zone of the tube. UV reflectance indicated complete crystallization.

D. Polysilicon film conductivity

The electrical conductivities σ of all polysilicon films were measured to check for possible doping by contamination from the metal substrate. They lay between 10^{-6} and 10^{-5} S·cm⁻¹ at room temperature, i.e., not much above the value of $\sim 10^{-7}$ S·cm⁻¹ for intrinsic silicon. The thermal activation energy of σ was 0.53 eV for a sample annealed at 600°C. (The conductivity of polysilicon on glass substrates, crystallized by 6-hour annealing at 600°C after hydrogen pre-seeding, is $\sim 10^{-3}$ S·cm⁻¹ at room temperature.) We also tested the oxide-coated substrate by successfully fabricating bottom-gate amorphous silicon TFTs at 250°C to 300°C (without crystallization) [16,17]. The conductivities of the polysilicon films, and the performance of these amorphous Si test transistors, demonstrate that the silicon films were not contaminated by the steel substrate. Therefore, we proceeded to make TFTs of the polycrystalline layers.

E. Transistor fabrication - 350 °C process (after crystallization) with deposited source/drain

Because we wanted our initial TFTs to measure the quality of the polysilicon films after the recrystallization process, all post-crystallization processing was done at low temperature. Thus we first used a non-self-aligned process with a maximum process temperature of 350°C, instead of the conventional self-aligned process, which requires an anneal at >600°C after ion implantation of the source/drain dopant.

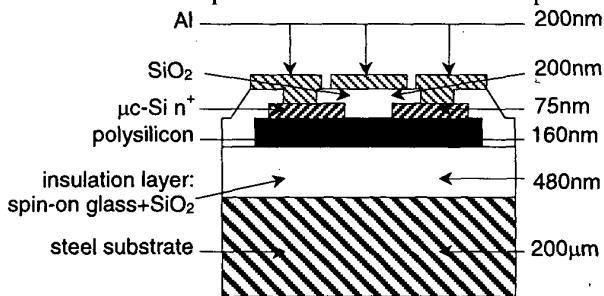


Figure 1. Schematic cross section of polysilicon top gate thin film transistor on steel, with deposited source/drain.

Figure 1 shows the schematic cross section of a top-gate polysilicon TFT made on steel. On top of the crystallized silicon layer, 75-nm thick n⁺ microcrystalline silicon (μ c-Si) was deposited by PECVD at 350°C to serve as the eventual source/drain. Then the original polysilicon layer was patterned into TFT islands by reactive ion etching (RIE), and the above n⁺ μ c-Si was patterned by another RIE step. Next, a 200-nm thick gate oxide was deposited by PECVD at 250°C, followed by a wet etch to open the source/drain contact windows. 200-nm of aluminum was thermally evaporated and

then patterned by wet etch to form the gate and source/drain contacts. The final step in the TFT fabrication was a 15-minute-long anneal at 250°C in a hydrogen (15vol.%) - nitrogen (85vol.%) mixture. This source/drain process is not practical for short-channel TFTs with low parasitic resistance, but is sufficient to evaluate the mobility in long channels. The relatively large parasitic source/drain resistance in our structure does not significantly affect the current and the extracted mobility. The channel is 45 μ m long and 180 μ m wide.

F. Transistor fabrication - 650 °C process (after crystallization) with ion-implanted source/drain

Having achieved state-of-the-art TFT performance with the low-temperature process described above, we now present initial results from a high temperature process using self-aligned, ion implanted source/drains (Fig 2).

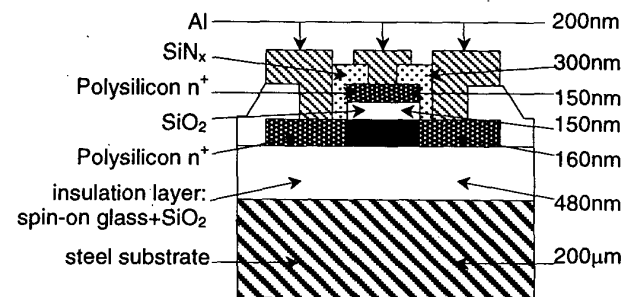


Figure 2. Schematic cross section of a self-aligned polysilicon thin film transistor on steel, with ion-implanted source/drain.

In the current process, the precursor a-Si:H film is crystallized, the active area defined by RIE, a 150nm gate SiO₂ deposited by PECVD at 250°C, 200nm intrinsic a-Si:H deposited by PECVD at 150°C and then is patterned by RIE to form the eventual gate. Then the SiO₂ layer is wet etched to open the source and drain. The source and drain are implanted with phosphorus at 50 keV and a dose of 2×10^{15} cm⁻². The implant damage is annealed out and the gate silicon crystallized was by a 5-hour furnace anneal at 650°C. Then a 300nm SiN_x passivation layer is PECVD deposited at 350°C, and source/drain and gate contact windows are opened by wet etch of the SiN_x. 300 nm Al is thermally evaporated and patterned to form the source/drain and gate electrodes. Finally, the TFTs are annealed in forming gas at 250°C for 15 minutes. The maximum process temperature after crystallization is the 650°C post ion implant anneal.

Results and Discussion

The TFTs were evaluated with a HP 4155A parameter analyzer. All measurements were made with the source and the steel foil grounded. Fig. 3 shows the transfer and output characteristics of TFTs made with the 350°C process of section E. The polysilicon of Fig's. 3(a) and 3(b) was

crystallized at 650°C in 1 hour with hydrogen plasma pre-seeding. The polysilicon of Fig's. 3(c) and 3(d) was crystallized at 950°C in 20 seconds without hydrogen plasma pre-seeding.

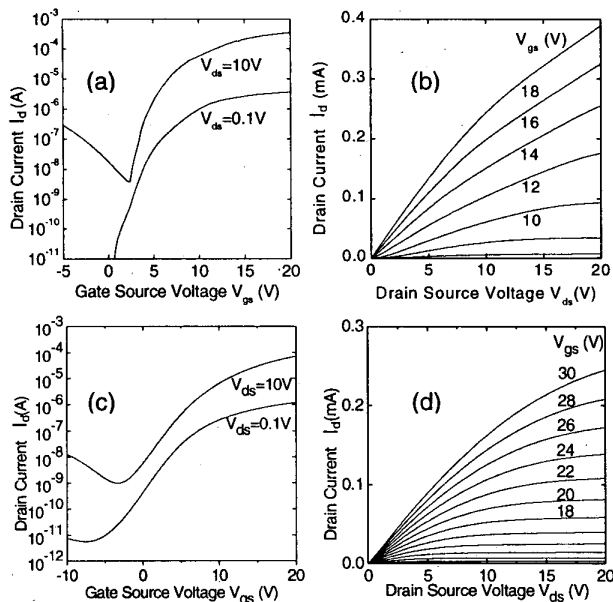


Figure 3. (a) Transfer and (b) output characteristics of a TFT made from polysilicon on steel annealed at 650°C, with deposited source/drain; (c) transfer and (d) output characteristics of a TFT made from polysilicon on steel annealed at 950°C, for 20s with deposited source/drain.

Table I lists the principal characteristics of all TFTs made with the 350°C process (after crystallization) of section E, from films crystallized at five temperatures. The threshold voltage and electron field effect mobility in the linear regime were extracted from the linear plot of I_{ds} vs. V_{gs} at $V_{ds} = 0.1V$, and the electron field effect mobility in the saturated regime was obtained from a plot of $I_{ds}^{1/2}$ vs. V_{gs} at $V_{ds} = V_{gs}$. The highest average mobility of $64 \text{ cm}^2V^{-1}s^{-1}$, observed both in the linear and saturated regimes, was obtained for crystallization at 650°C, and this lies at the top of the range for conventional furnace-annealed material [3]. Typical threshold voltages and subthreshold slope (at 10V V_{ds}) are 7.2V and 0.4V/decade, respectively, for the 650°C TFTs.

Fig's. 4(a) and 4(b) show the transfer and output characteristics of a TFT made with the 650°C self-aligned process of section F, from polysilicon crystallized at 950°C in 20 seconds without hydrogen plasma pre-seeding. This TFT has an on current of 25 mA, an off current of 3.4 nA, an on/off ratio of 10^5 for $V_{ds}=0.1$, a threshold voltage of 14 V, a subthreshold slope of 3.3 V/decade, and electron mobilities of 4.9 (linear) and 5.6 (saturated) $\text{cm}^2V^{-1}s^{-1}$.

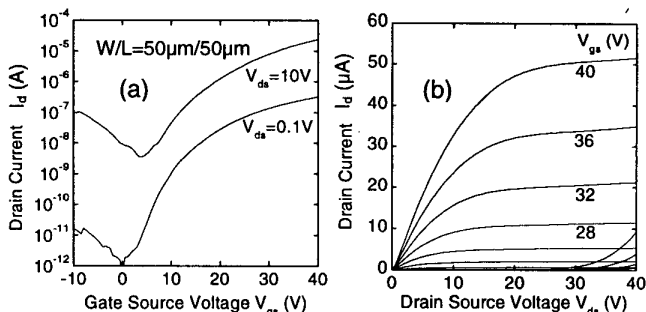


Figure 4. (a) Transfer and (b) output characteristics of a self-aligned TFT made from polysilicon on steel annealed at 950°C for 20s, with ion-implanted source/drain.

Note most significantly that the minimum off currents at $V_{ds} = 10V$ are in the $10^{-9}A$ range, independent of the annealing process, and this value is comparable to the off currents of polysilicon TFTs on glass substrates [18,19]. The low off current is very important, because it suggests that the TFT function is not adversely affected by metal contamination from the substrate. For all five crystallization processes the threshold voltages lie in the range of 4 to 10 V. (Table I). The mobility for the 700°C film, of 13 to 20 $\text{cm}^2V^{-1}s^{-1}$, is comparable to the mobilities of polysilicon TFTs made on quartz glass substrate [20]. The improved performance of the 950°C TFTs over the 750°C TFTs suggests that larger grains indeed are obtained at 950°C. Table I summarizes the characteristics of the TFTs made with the 350°C process, which are shown in part also in Fig. 5(a).

Fig. 5(b) presents the crystallization times in function of temperature, showing the significant decrease in crystallization time afforded by the high temperature process allowed by the steel foil. Note that the differential thermal expansion between the SiO_2 passivation layer (α of fused quartz = $0.6 \times 10^{-6} \text{ K}^{-1}$), the TFT materials ($\alpha \cong 4 \times 10^{-6} \text{ K}^{-1}$), and steel ($\alpha = 18 \times 10^{-6} \text{ K}^{-1}$), does not seem to pose a systematic problem. A very attractive feature of steel foil substrates is their ruggedness and flexibility [17,21]. Therefore our results suggest that steel substrates can furnish rugged high-performance TFT backplanes for emissive and reflective displays. The successful use of steel foil furthermore suggests the feasibility of a roll-to-roll polysilicon TFT technology.

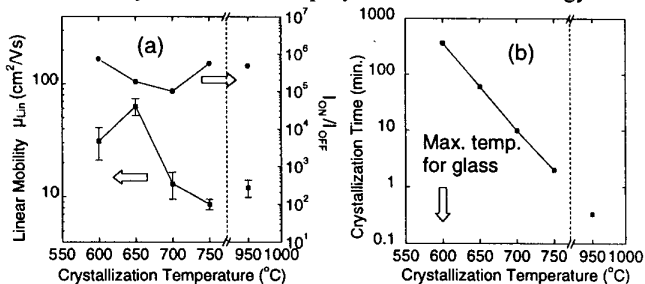


Figure 5. (a) TFT performance (350°C process) vs. crystallization temperature, and (b) Crystallization time vs. crystallization temperature.

5.4.3

Summary

Thin film transistors were fabricated of polycrystalline silicon, made by crystallization at temperatures ranging from 600°C to 950°C on SiO₂ coated steel substrates with crystallization as short as 20s. Due to their tolerance of high process temperatures, steel substrates enable much shorter process times than glass substrates. TFT performance is not adversely affected by contamination from the steel substrate, and the films do not crack during the high temperature process. The technology of polysilicon film on steel foil opens a new route to the high throughput roll-to-roll manufacturing of thin film transistors with uniform characteristics on large-area, low-cost, and rugged substrates.

Acknowledgement

This research is supported by DARPA's High Definition Systems and Molecular Level Printing Programs. Ming Wu thanks the Princeton Plasma Physics Laboratory for a summer stipend.

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Table I. Electrical characteristics of the polycrystalline thin-film transistors with deposited source/drain (350°C process). All electrical measurements are averages from ≥ 10 devices.

Cryst. Temp. (°C)	Cryst. time (minutes)	Hydrogen plasma exposure	Polysilicon conductivity σ^a (S/cm)	UV reflectance ΔR^b (%)	ON current I_{ON}^c (A)	OFF current I_{OFF}^d (nA)	I_{ON}/I_{OFF}	Threshold voltage V^e (V)	Subthreshold slope f^f (V/decade)	Electron mobility (linear) (cm ² /Vs)	Electron mobility (saturated) (cm ² /Vs)
600	360	1 hour	1.1×10^{-5}	6.7	$1.8 \times 10^{-4} \pm 0.6$	2.5 ± 1	-10^5	7.0 ± 1.3	0.9 ± 0.4	31 ± 10	55 ± 11
650	60	1 hour	2.0×10^{-6}	6.2	$3.8 \times 10^{-4} \pm 0.2$	2.1 ± 1.7	-10^5	7.2 ± 1.8	0.4 ± 0.3	63 ± 11	64 ± 11
700	10	1 hour	0.8×10^{-6}	5.5	$5.9 \times 10^{-5} \pm 0.9$	0.59 ± 0.5	-10^5	8.0 ± 3.7	1.8 ± 0.7	13 ± 3.5	20 ± 4
750	2	1 hour	1.4×10^{-6}	6	$3.8 \times 10^{-5} \pm 0.2$	0.69 ± 2.6	-10^5	7.4 ± 1.4	2.7 ± 0.2	8.6 ± 0.9	10.6 ± 1.3
950	0.33	None	2.0×10^{-6}	7.5	$6.2 \times 10^{-5} \pm 0.6$	1.3 ± 0.3	-10^5	7.2 ± 0.8	2.4 ± 0.2	12 ± 2.1	12 ± 1.3

a) at 300K; b) UV reflectance difference from a-Si: H at 276nm, for silicon wafer $\Delta R=7.5\%$; c) at $V_{gs}=20V$, $V_{ds}=10V$; d) at $V_{ds}=10V$; e) at $V_{ds}=0.1V$; f) at $V_{ds}=10V$.

5.4.4