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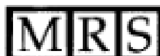

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Polycrystalline $Si_{1-x-y}Ge_xC_y$ for Suppression of Boron Penetration in PMOS Structures

C.L. Chang and J.C. Sturm, Department of Electrical Engineering, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, NJ 08544. clchang@ee.princeton.edu

ABSTRACT

We have fabricated polycrystalline $Si_{1-x-y}Ge_xC_y$ by Rapid Thermal Chemical Vapor Deposition and used it as part of a polycrystalline gate structure for PMOS devices. The results showed that the use of carbon in polycrystalline $Si_{1-x-y}Ge_xC_y$ suppressed boron penetration across the gate oxide. No effects of gate depletion with the use of poly-$Si_{1-x-y}Ge_xC_y$ were observed. Our work suggests that the addition of carbon reduced the chemical potential of boron in $Si_{1-x-y}Ge_xC_y$, which deterred boron from diffusing across the underlying gate oxide.

INTRODUCTION

In a traditional complementary metal-oxide-semiconductor (CMOS) technology, heavily doped n-type (n^+) polycrystalline silicon gates are used for both n- channel (NMOS) and p-channel (PMOS) devices. In order to achieve a high drive current and an optimal logic-gate performance, it is desirable that both n- and p- channel devices have small and opposite threshold voltages (V_T) with comparable magnitudes. The n^+ polycrystalline silicon gate yields a reasonable threshold voltage for n-channel devices, but the threshold voltage of the p-channel devices has a much higher magnitude. As a result, boron is implanted into the device channel to adjust threshold voltage, forming a buried-channel PMOS device.

Even though buried-channel devices generally exhibit a higher carrier mobility than typical surface-channel devices by moving carriers away from SiO_2/Si interface, the advantage is outweighed by other short-channel effects, such as threshold voltage lowering, higher subthreshold currents and higher susceptibility to punchthrough[1]. Furthermore, buried channels are not suitable for low temperature operation due to a dopant freeze-out problem[2]. As a result, as devices are scaled down in size to below 0.35 μm in gate length, "dual-gate" devices are desirable to create both PMOS and NMOS surface-channel devices with better short-channel characteristics.

In dual-gate CMOS devices, n^+ polycrystalline silicon is used as the gate for NMOS devices and p^+ polycrystalline silicon for PMOS devices. A single undoped polycrystalline silicon layer is deposited, which is then doped n^+ or p^+ by the source/drain implantation process of the n-channel and p-channel devices, respectively. For a p^+ polycrystalline silicon gated device, the gate is implanted with boron or boron difluoride (BF_2) at the same time as are source and drain. Unfortunately, boron has been observed to penetrate across the thin gate oxide during post-implant anneal, resulting in a threshold voltage instability[3]. Moreover, even though gate oxides with the presence of fluorine have been shown to increase the resistance to hot-carrier effects, enhanced boron penetration has been reported due to the presence of fluorine in gate oxide[4]. Fluorine increases the boron diffusion constant in oxide[5]and it has been shown that the boron diffusivity increases approximately as the square root of the fluorine dose.

In this paper, we propose using polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a polycrystalline gate to improve the problem of boron penetration. Our work was motivated by the recent interest in using substitutional carbon in single crystalline $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$ to dramatically suppress boron diffusion due to thermal annealing in nitrogen[6], oxidation- enhanced diffusion[7], or transient-enhanced diffusion[8]. Polycrystalline $Si_{1-x}Ge_x$-based gates have been studied due to the

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following advantages. First, it is possible to adjust the work function of polycrystalline $Si_{1-x}Ge_x$ by varying the amount of germanium incorporation to adjust the flatband voltage (or threshold voltage)[9]. Second, the sheet resistance of polycrystalline $Si_{1-x}Ge_x$ is lower than that of the polycrystalline silicon due to a larger grain size which reduces carrier scattering[10]. Here we report that by incorporating carbon into polycrystalline $Si_{1-x}Ge_x$, the problem of boron penetration can be greatly minimized.

EXPERIMENTS

Samples were fabricated by first thermally oxidizing n-type silicon wafers in dry oxygen at 900°C for ~ 15 minutes, resulting in 80-90 Å oxides. Polycrystalline gates were deposited on top of gate oxides by rapid thermal chemical vapor deposition (RTCVD). Polycrystalline silicon was deposited at 700°C using silane, and polycrystalline $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers were deposited at 625°C with silane, germane and methylsilane flow, all with H_2 as a carrier gas at 6 torr. Diborane was used for p-type doping if samples were in-situ doped. Ion-implantation was performed with $5x10^{15}/cm^2$ BF_2^+ doses at 60 keV, resulting in ~ 100nm deep implantation damage. BF_2^+ was used because it has been widely used in industry for gates as well as source/drain shallow implants of MOSFET devices. Fluorine-enhanced boron diffusion will also make the effect of boron penetration significant in this study even with a relatively thick oxide. Samples were annealed in nitrogen after implantation. To study boron penetration across the gate oxide, metal-oxide-semiconductor (MOS) capacitors were fabricated. The capacitor size was 320 μm x 180 μm.

RESULTS

The first set of samples contain three different gate structures. The first sample A(1) is similar to a traditional MOS structure, with a ~ 400nm polycrystalline silicon on a 90Å gate oxide. In the second sample A(2), a ~ 20nm thick polycrystalline $Si_{1-x-y}Ge_xC_y$ was inserted between the gate oxide and polycrystalline silicon while keeping the total gate thickness unchanged. Crystalline $Si_{1-x-y}Ge_xC_y$ grown under identical conditions contains 20% germanium and 0.6% substitutional carbon. The third sample is similar to A(2) except polycrystalline $Si_{1-x-y}Ge_xC_y$ was replaced by polycrystalline $Si_{1-x}Ge_x$ to single out the effect of substitutional carbon. All layers were initially undoped and subsequently doped by BF_2^+ implants.

Figure 1 shows high-frequency (1 MHz) capacitance-voltage (C-V) curve of BF_2^+ implanted samples annealed at 900°C for 40 and 80 minutes. After a 40 minute anneal, there is no pronounced change in the threshold voltage and C-V curves behave normally. As the annealing time was increased to 80 minutes, however, C-V curves shifted by a few volts for samples A(1) and A(3), an indication of boron penetration. A much lower shift is observed in sample A(2), indicating that $Si_{1-x-y}Ge_xC_y$ suppresses the boron penetration. Figure 1(c) shows the threshold voltage as a function of annealing time. It is concluded that polycrystalline $Si_{1-x}Ge_x$ slightly improves the problem of boron penetration while carbon in $Si_{1-x-y}Ge_xC_y$ greatly suppresses boron penetration.

Although the $Si_{1-x-y}Ge_xC_y$ layer suppressed boron penetration, it is crucial that boron still diffuse through the $Si_{1-x-y}Ge_xC_y$ so that the entire gate is heavily doped. This is necessary to avoid gate depletion effects for negative gate bias (inversion) which would reduce the charge in the inversion layer (and the transistor drive current). Quasi-static C-V curve of sample A(2) annealed at 40 minutes, shows the same capacitance in inversion and accumulation, so that we conclude no gate depletion effect occurs with the $Si_{1-x-y}Ge_xC_y$ layer.(see figure 2) A smaller

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reverse-biased capacitance is observed in sample A(1), which could be the result of boron penetration[11] and not gate depletion effects.

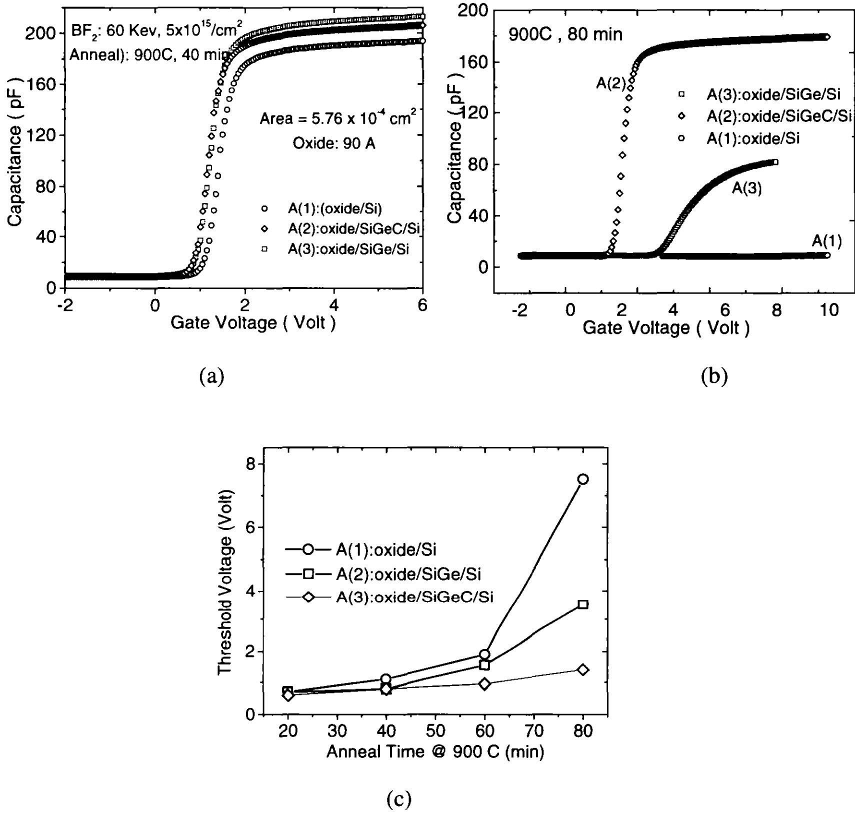

Figure 1: (a) High-frequency C-V curves of implanted samples annealed at 900°C for 40 minutes. (b) C-V curves after 80 minutes of annealing. (c) Threshold voltage as a function of annealing time.

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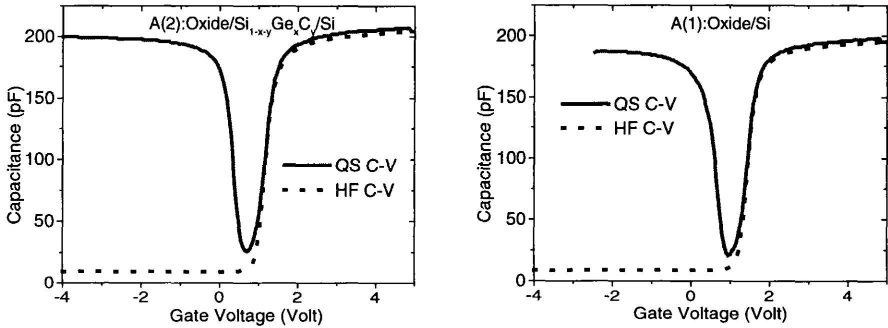

Figure 2: Quasi-Static Capacitance-Voltages curves of sample A(1) and A(2) annealed at 900°C, 40 minutes.

Figure 3 shows the boron concentration profiles analyzed by Secondary Ion Mass Spectroscopy (SIMS) for sample A(1) and A(2) annealed at 900°C, 80 minutes. Boron reached down to top oxide interface for both sample A(1) and A(2), an indication that boron indeed diffused through $Si_{1-x-y}Ge_xC_y$ layer. SIMS also revealed boron penetration in sample A(1). We also observed that fluorine piled up in gate oxides for both sample A(1) and A(2) and there is no evidence of fluorine accumulation in $Si_{1-x-y}Ge_xC_y$. Therefore, we concluded that the effect of carbon on suppressing boron penetration is not due to trapping of fluorine to reduce the boron

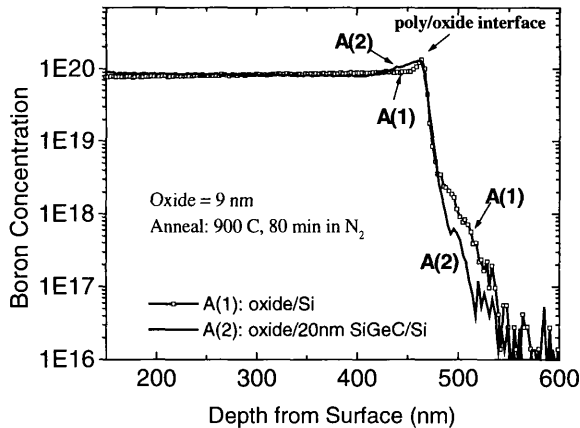

Figure 3: Boron profiles in sample A(1), A(2) by SIMS. Samples were BF_2^+ implanted and annealed at 900°C for 80 minutes.

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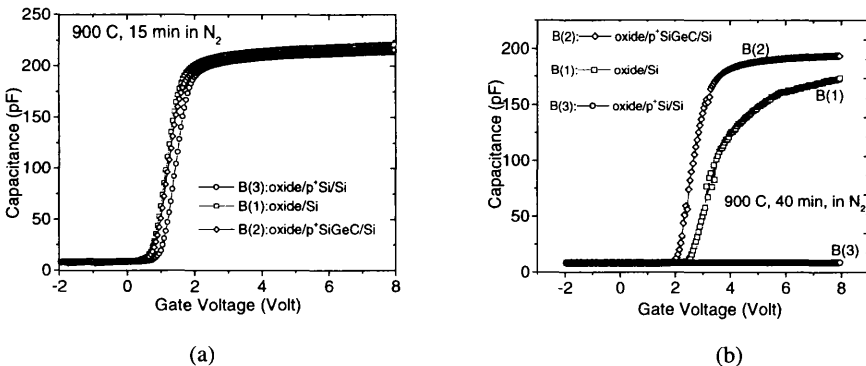
diffusion constant in oxide. We feel that the reduction in boron penetration is due to a lower chemical potential of boron in $Si_{1-x-y}Ge_xC_y$ than in Si, which suppresses boron from diffusing through the underlying oxide. This argument is supported by the observation of a preferential boron segregation in $Si_{1-x-y}Ge_xC_y$ compared to Si, as in figure 3. A higher boron concentration will further reduce gate depletion effect, which shows another advantage of using polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a gate structure. Note that the apparent ability of boron to diffuse through poly-$Si_{1-x-y}Ge_xC_y$ as opposed to single crystalline $Si_{1-x-y}Ge_xC_y$ may be due to grain boundary diffusion in the polycrystalline film.

To test our argument and further eliminate the possibility that poly-$Si_{1-x-y}Ge_xC_y$ suppressed boron penetration through the underlying gate oxide by blocking the incoming boron flux, we designed another set of samples in which $Si_{1-x-y}Ge_xC_y$ is in-situ doped. Sample B(1) is a typical PMOS structure with ~300nm undoped polycrystalline silicon on a ~ 8nm oxide, used as a controlled sample. In B(2), we grew a 50nm p^+ poly-$Si_{1-x-y}Ge_xC_y$ layer between the undoped polycrystalline silicon and the gate oxide while keeping the total gate thickness unchanged. For comparison, we grew sample B(3) similar to sample B(2) except p^+ poly-$Si_{1-x-y}Ge_xC_y$ was replaced by p^+ polycrystalline silicon. SIMS indicated that the boron concentration in the in-situ doped $Si_{1-x-y}Ge_xC_y$ and Si is ~$10^{21}/cm^3$, while the boron concentration is $10^{20}/cm^3$ in the initially undoped polysilicon after doping by implantation of BF_2^+ and annealing.

Figure 4 and 5 show C-V curves and threshold voltage of samples annealed at 900°C for two different annealing times. It is interesting that even with $10^{21}/cm^3$ boron at the p^+ $Si_{1-x-y}Ge_xC_y$ /oxide interface, sample B(2) has a smaller threshold voltage shift than that of sample B(1), which has only $10^{20}/cm^3$ boron in the polycrystalline silicon after implantation and annealing. Also, for boron to penetrate across the gate oxide in sample B(1), it has to first travel through the polysilicon gate (via grain boundaries) and reach the top oxide interface. Both lower doping and a longer distance would seem to warrant less boron penetration in sample B(1), which is opposite from what was observed. This is further evidence that $Si_{1-x-y}Ge_xC_y$ suppresses boron penetration by lowering the chemical potential of boron in the gate.



(a) (b)

Figure 4: (a) High-frequency C-V curves of implanted samples annealed at 900°C for 15 minutes. (b) C-V curves of 40 minutes anneal.

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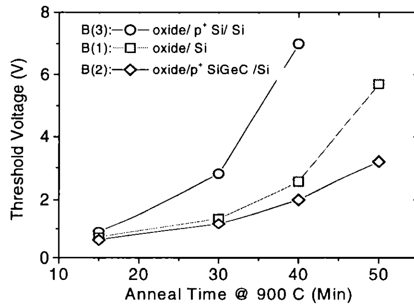

Figure 5: Threshold voltage as a function of annealing time for B(1), B(2) and B(3).

CONCLUSION

In summary, we have used polycrystalline $Si_{1-x-y}Ge_xC_y$ as part of a polycrystalline gate structure to study the effect on boron penetration across gate oxide. The existence of carbon in polycrystalline $Si_{1-x-y}Ge_xC_y$ suppressed boron penetration. We also found a preferred accumulation of boron in $Si_{1-x-y}Ge_xC_y$ which is advantageous in reducing the gate depletion effect. Both observations suggest that carbon reduces the chemical potential of boron.

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