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Suppression of Boron Outdiffusion in SiGe HBTs by Carbon Incorporation

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Abstract

A key problem faced by npn SiGe technology is the outdiffusion of boron from the SiGe base caused by thermal annealing or transient enhanced diffusion. In this paper we investigate the effects of C incorporation in the base on boron diffusion caused by thermal annealing and As emitter implantation. The higher Early voltages of the C transistors compared with that of the no-C transistors indicates that C incorporation in the base dramatically reduces the diffusion of B under postgrowth implantation and annealing procedures.

Introduction

SiGe HBT technology often uses high Ge fractions at the emitter-base interface which allows for high base boron doping levels ($N_A \sim 10^{20}$ cm^{-3}) and consequently low base sheet resistance. Such heavily doped bases have been used to achieve record SiGe f_{max} transistor performance [1]. However, heavily doped bases are susceptible to B outdiffusion from the base which causes conduction band barriers to appear at the base-collector junction [2]. These barriers reduce the transistor's gain, speed, and Early voltage [3,4].

Boron diffusion may be caused by heat treatment or by transient enhanced diffusion from the annealing of implantation damage. Arsenic implantation into the single crystal emitter of SiGe bases with high base doping levels has been shown to cause outdiffusion of B into Si upon annealing [5]. The limitations on SiGe HBT technology posed by the necessity of low thermal budgets and the absence of As implantation for emitter contact formation pose severe constraints for SiGe HBT process integration.

To accommodate the outdiffusion of boron by any one of the above mechanisms, undoped spacer layers of SiGe are usually grown on either side of the doped base [2]. The key technological problem faced is that strained SiGe films have a finite critical thickness before dislocation formation. Hence for a fixed doped base thickness, the thickness of undoped spacers to alleviate outdiffusion problems is limited by critical thickness considerations. The small amounts of B diffusion necessary to cause adverse device effects are less than can be easily detected by SIMS, and are best detected by a drop in I_{co}, or by a dependence of I_{co} on V_{BC} (reduced Early voltage) as the B-C bias pulls down and removes the parasitic barriers which limit I_c.

Effect of C on Uniform Composition Bases with Spacers

The npn Si/SiGeC/Si device epi layers were grown by RTCVD [2] using methlysilane as the carbon source. The base layers were grown on top of a 1 µm phosphorus doped Si buffer and a 2000 Å 5 10^{17}-10^{18} cm^{-3} Si collector. Identical $Si_{0.8-y}Ge_{0.2}C_y$ bases were grown at 625°C with 0.5% C (as measured by X-ray diffraction) and without carbon. As shown in Fig. 1a and 1b, 100, 200, and 400 Å 10^{20} cm^{-3} B-doped $Si_{0.8-y}Ge_{0.2}C_y$ bases were grown with 100 Å undoped $Si_{0.8-y}Ge_{0.2}C_y$ spacers on either side to accommodate any boron diffusion during the emitter growth. Following the base, an insitu phosphorus doped emitter ($\sim 10^{19}$ cm^{-3}) was subsequently grown at 700°C for 73 minutes. SIMS of 400 Å doped SiGe and SiGeC bases are shown in Fig. 2a and 2b (phosphorus and oxygen levels have been removed for clarity). TEM showed no dislocations or SiC precipitates in the base layers.

Our group recently used the temperature dependence of SiGeC HBT collector currents to study the effect of C on the SiGeC bandgap [6]. That work has shown that the addition of C to strained SiGeC layers on Si (100) increases the bandgap only slowly as the strain is reduced, leading to an increased critical thickness for a given bandgap in SiGeC compared to that of SiGe.

Transistor characteristics are a much more sensitive probe than SIMS to study B diffusion. Hence, in this paper we have used two different transistor structures fabricated on different pieces from the same wafer to isolate the effects of boron outdiffusion caused by thermal diffusion used to simulate a higher thermal budget process than that experienced during emitter growth (Fig. 3a) and that of transient enhanced diffusion due to an As emitter implant and anneal (Fig. 3b). The simple, zero temperature budget, mesa process used for the transistors unfortunately results in non-ideal base currents due to the unpassivated surfaces. While the transistors used in this study are not of "manufacturable quality", they are more than adequate for characterizing the motion of boron in the intrinsic base through I_c measurements.

1) Heat treatment

Figure 2a shows SIMS of a device with a 10^{20} cm^{-3} [B] doped base with a Ge fraction of 20%. 100 Å undoped spacers layers were grown on either side of the doped base to accommodate any boron diffusion during emitter growth. As seen at the E-B and B-C interfaces, the boron is totally accommodated within the SiGe. Using a zero thermal budget process, devices were fabricated from wafers according to Fig. 1a with a 100 Å doped base. Devices were also fabricated from 100 Å doped base wafers grown with 50 Å spacers instead of 100 Å. Fig. 4a and 4b show Gummel plots and common emitter characteristics from the 100 Å and 50 Å spacer wafers, respectively. Applying a 1 V reverse bias to the collector of the 50 Å spacer devices increases J_{co} by a

factor of 2.2, but does not affect the J_{co} of the 100 Å spacer devices. This increase in collector current with increasing base-collector reverse bias is reflected in the common-emitter characteristics by the drop in Early voltage from ~50 V for the 100 Å spacer transistors to ~0.5 V for the 50 Å spacer transistors. One may conclude that the B profile is not sufficiently abrupt on a 50 Å scale in the as grown wafers.

Different pieces from the 100 Å doped SiGe and SiGeC wafers with 100 Å spacers were heated to temperatures of 809, 855, or 890°C for 15 minutes in N_2 to simulate the effects of higher temperature processing steps on the as-grown wafers. The pieces were then processed according to Figure 3a. Figures 5a and 5b show Gummel plots for transistors from the wafers annealed at different temperatures for the no C and C wafers, respectively. Figure 5a shows that annealing temperatures greater than ~800°C for 15 minutes leads to lower transistor J_{co} at $V_{BC} = 0$ V for the no carbon transistors. In comparison to the as grown device, J_{co} has dropped by a factor of ~25 during the 855°C, 15 minute anneal. This indicates parasitic B diffusion and barrier formation at the base-collector junction. Figure 5b shows that outdiffusion in SiGeC starts at temperatures higher than ~850°C. These results show that the addition of C suppresses B diffusion.

(2) As emitter implantation and annealing

To simulate the effects of an As emitter implant to contact a lightly doped emitter, devices were fabricated from epi layers which underwent $1.5 \ 10^{15} \ cm^{-2}$ 30 keV and $3 \ 10^{14}$ 15 keV blanket As implants (chosen to follow [7]) with subsequent 15 minute N_2 activation anneals. Anneals were performed at 647 or 742°C. The pieces were then processed according to Figure 3b. Gummel plots and common emitter characteristics for both no C and C wafers annealed at 647°C are shown in Figures 6a and 6b respectively, for 100 Å doped bases. As seen in Fig. 6a, significant barrier formation in devices without C results in degraded transistor characteristics even though 647°C is significantly less than that of the original emitter growth temperature. This is clear evidence of TED of boron. No evidence of reduced I_{co} or Early voltage is seen in the SiGeC case for a 647°C anneal, again showing that C suppresses TED. However, the SiGeC transistors also show degradation in the form of higher I_B, an effect which becomes even more severe in the SiGeC devices after a 742°C anneal. Similar results were found with thicker doped bases.

SIMS of 755°C As implanted and annealed no-C and C wafers with 200Å doped bases (Fig. 7a and 7b) confirms that C incorporation does indeed prevent B diffusion due to TED from the emitter implant.

It has been reported that TED in the intrinsic SiGe base can also result from extrinsic B implantation to form the base contact [8]. We have observed similar effects in devices without C which are suppressed in devices with C.

Doped SiGe/SiGeC/SiGe Base Transistors

In addition to the wafers grown with carbon in both the doped base and in the undoped spacers, wafers were also grown which sandwiched the doped SiGeC layers between doped SiGe, as shown in Fig. 1c. Two wafers were grown, one with a carbon fraction of 0.5% and one with a carbon fraction of 0.9 %. SIMS of the 0.9% C wafer is shown in Fig. 2c.

Devices were fabricated from pieces from these wafers which were subjected to the As implantation and annealing. Figure 6d shows the results from As implantation and annealing at 742°C for 15 minutes for the 0.5% C sample. Whereas the SiGe and SiGeC base HBTs demonstrate lower I_{co} or higher I_B, respectively, the sandwiched bases show no degradation. SIMS from a 755°C annealed sample is shown in Fig. 7c, demonstrating that no outdiffusion has occurred. These results suggest that carbon within doped SiGe reduces TED effects for the entire base, even though it does not exist where all the dopant atoms are. In addition, it seems that for implantation processes, the carbon atom must be separated from the p-n junctions by doped SiGe spacer layers to prevent high I_B as seen in Fig. 6c.

Discussion and Conclusions

Both C in Si [9] and $10^{20} \ cm^{-3}$ O levels in SiGe [7] have previously been shown to reduce B diffusion. The low O (2 $10^{18} \ cm^{-3}$) levels in our SiGe and SiGeC bases are identical, indicating that our results are due to the incorporation of C and not due to O effects.

We have demonstrated that C incorporation in the base of SiGe HBTs dramatically reduces the diffusion of B under postgrowth implantation and annealing procedures. These results lead to improved device characteristics and may not only be important for Si/SiGe(C)/Si HBT devices, but may also be useful for general Si process technology as well.

References

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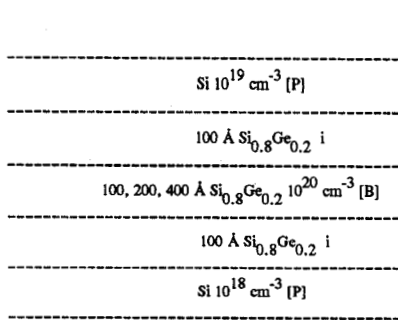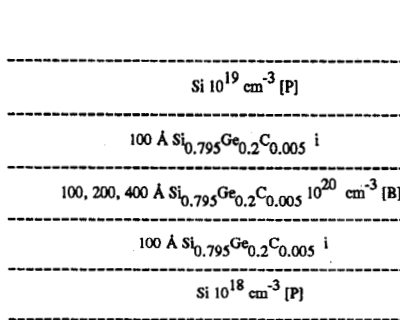[9] P.A. Stolk, et. al., *Appl. Phys. Lett.*, vol. 66, no. 11, pp. 1370-1372, 1995.
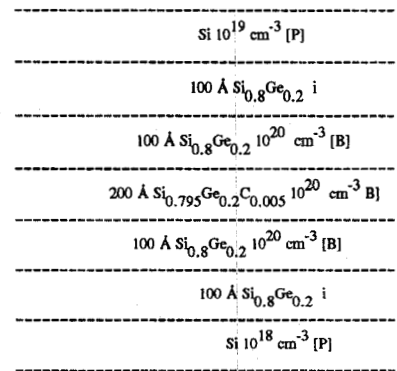
10.2.2

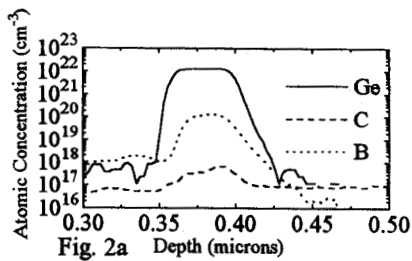Fig. 1a

Fig. 1b

Fig. 1c

Fig. 1 As grown layers used for devices

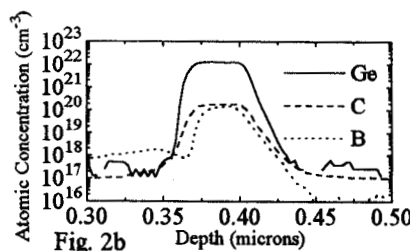Fig. 2a   Depth (microns)
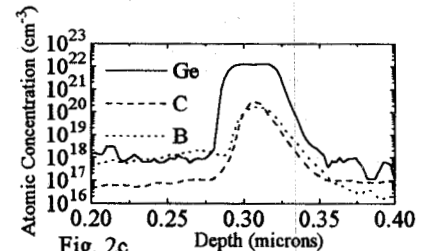
Fig. 2b   Depth (microns)

Fig. 2c   Depth (microns)

Fig 2. SIMS of SiGe, SiGeC, and SiGe/SiGeC/SiGe bases.
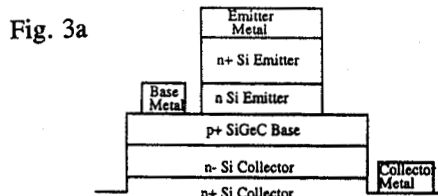

Fig. 3a
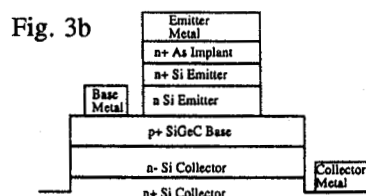
Fig. 3b

Fig. 3   Device cross sections used to isolate the effects of (a) thermal annealing and (b) emitter implants.
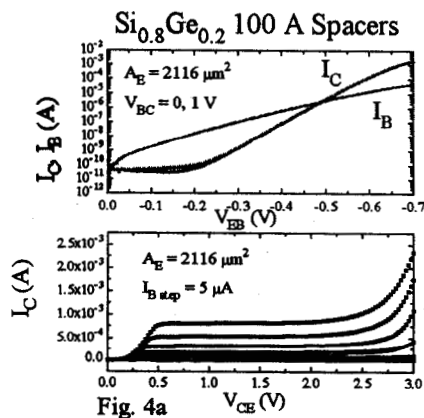

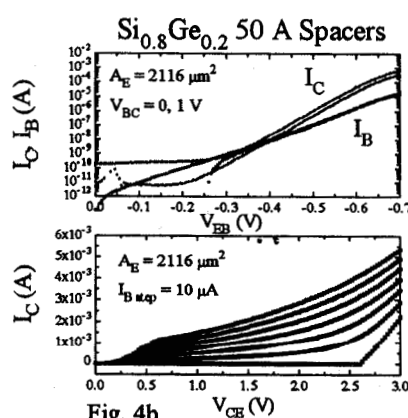Fig. 4a V_{CE} (V)
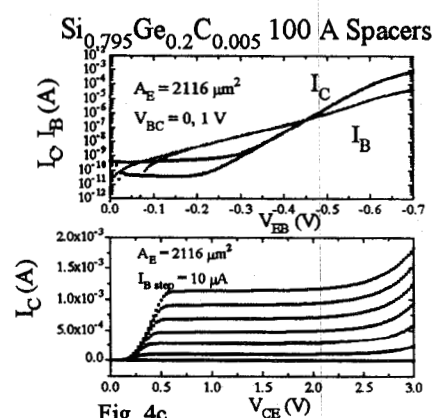
Fig. 4b V_{CE} (V)

Fig. 4c V_{CE} (V)

Fig. 4 As grown transistor curves for 100 A doped bases

10.2.3
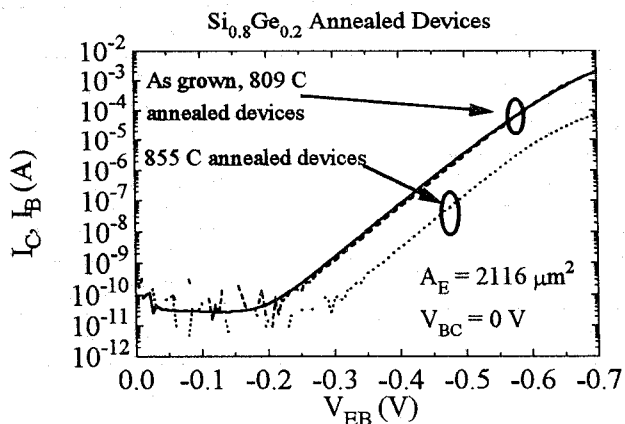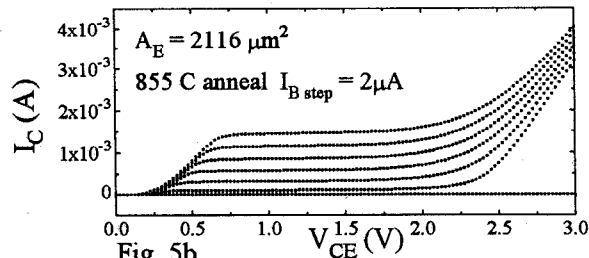
Si$_{0.8}$Ge$_{0.2}$ Annealed Devices

As grown, 809 C annealed devices

855 C annealed devices

$A_E = 2116 \ \mu m^2$

$V_{BC} = 0 \ V$

Si$_{0.795}$Ge$_{0.2}$C$_{0.005}$ Annealed Devices

As grown, 809 C, 855 C annealed devices

890 C annealed devices

$A_E = 2116 \ \mu m^2$

$V_{BC} = 0 \ V$

$A_E = 2116 \ \mu m^2$

855 C anneal $I_{B \ step} = 8 \mu A$

Fig. 5a

$A_E = 2116 \ \mu m^2$
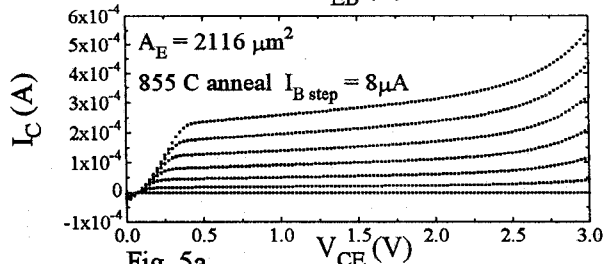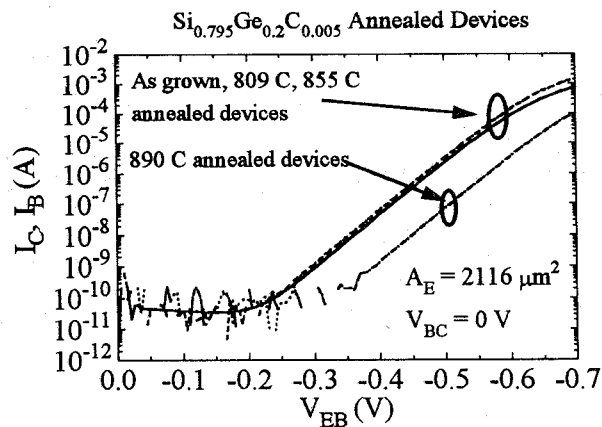
855 C anneal $I_{B \ step} = 2 \mu A$

Fig. 5b

Fig. 5 Transistor characteristics of annealed wafers

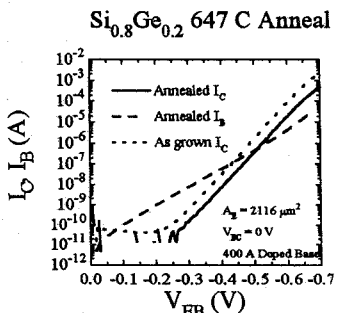## Si$_{0.8}$Ge$_{0.2}$ 647 C Anneal

Annealed I_c
Annealed I_b
As grown I_c

$A_E = 2116 \ \mu m^2$
$V_{BC} = 0 \ V$

400 A Doped Base

$A_E = 2116 \ \mu m^2$
$I_{B \ step} = 10 \ \mu A$

Fig. 6a V_{CE} (V)

Si$_{0.795}$Ge$_{0.2}$C$_{0.005}$ 647 C Anneal

Annealed I_c
Annealed I_b
As grown I_c

$A_E = 2116 \ \mu m^2$
$V_{BC} = 0 \ V$

400 A Doped Base

$A_E = 2116 \ \mu m^2$
$I_{B \ step} = 50 \ \mu A$

Fig. 6b V_{CE} (V)

Si$_{0.795}$Ge$_{0.2}$C$_{0.005}$ 742 C Anneal

Annealed I_c
Annealed I_b
As grown I_c

$A_E = 2116 \ \mu m^2$
$V_{BC} = 0 \ V$

100 A Doped Base

$A_E = 2116 \ \mu m^2$
$I_{B \ step} = 75 \ \mu A$

Fig. 6c V_{CE} (V)

SiGe/SiGeC/SiGe 742 C Anneal

Annealed I_c
Annealed I_b
As grown I_c

$A_E = 2116 \ \mu m^2$
$V_{BC} = 0 \ V$

400 A Doped Base

$A_E = 2116 \ \mu m^2$
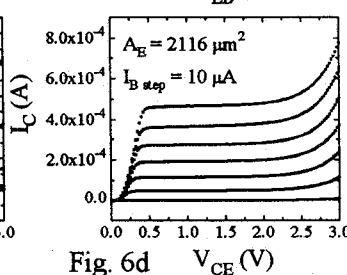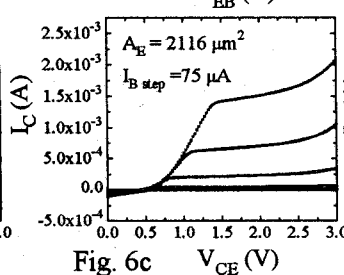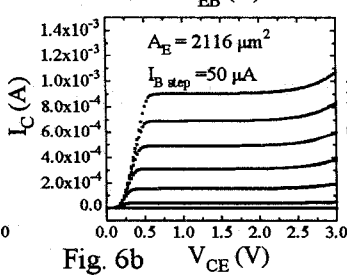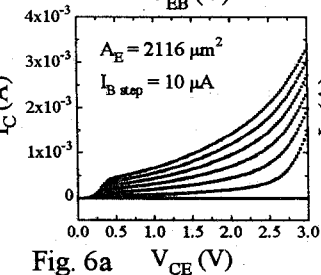$I_{B \ step} = 10 \ \mu A$

Fig. 6d V_{CE} (V)

Fig. 6 Transistor curves for devices with As implanted emitters. As grown I$_C$ is from Fig. 3a transistor structure.

Ge
C
B

Fig. 7a Depth (Angstroms)

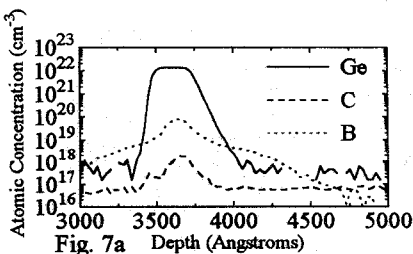Ge
C
B

Fig. 7b Depth (Angstroms)
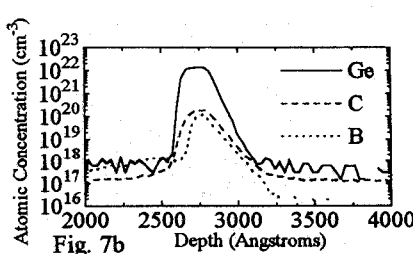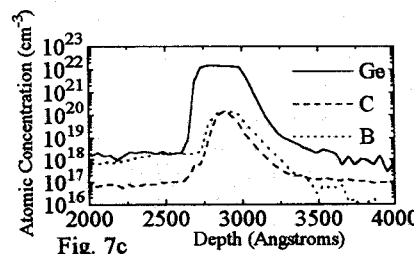
Ge
C
B

Fig. 7c Depth (Angstroms)

Fig 7. SIMS of SiGe, SiGeC, and SiGe/SiGeC/SiGe devices with emitters implanted with As and annealed at 755 C.

10.2.4