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EPITAXIAL GROWTH OF SILICON-BASED HETEROSTRUCTURES BY LOW TEMPERATURE RAPID THERMAL CHEMICAL VAPOR DEPOSITION

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The typical range of growth temperatures necessary to grow $Si_{1-x}Ge_x/Si$ heterostructures is from 450 to 650 °C, which corresponds to the surface reaction limited growth regime for CVD. These low temperatures are necessary for the formation of strained-layer alloys as well as for the formation of epitaxial layers with thicknesses of the order of 10 nm. In the surface reaction limited growth regime, temperature control, interface abruptness and oxygen contamination are key issues which must be addressed.

INTRODUCTION

The drive for improving device performance for high speed integrated circuits is pushing the limits of silicon technology. High speed technology has relied on shrinking lateral device dimensions to minimize the distance electrons must travel within individual devices as well as between devices. Device performance has also been improved by utilizing vertical carrier transport in epitaxially grown semiconductors. Features on the order of ten nanometers are readily achieved in vertical devices by controlling interface characteristics of epitaxially grown layers. Further improvements that are available in vertical devices are gained by heterojunction capabilities. By using the discontinuous band gap between the two semiconductors, new devices can be engineered to improve device performance. Low-temperature epitaxy is required to facilitate the growth of strained layer alloys which are needed for heterojunction formation with silicon. Low temperature epitaxy is also needed to reduce dopant inter-diffusion so that small vertical dimensions can be realized.

Heterojunctions offer improved device performance through the formation of a discontinuous band gap at semiconductor interfaces. Silicon-based devices which exploit a heterojunction for increased speed, such as high mobility field effect transistors [1] and heterojunction bipolar transistors [2], have been demonstrated with strained $Si_{1-x}Ge_x$ (silicon-germanium) on silicon substrates. Unlike III-V heterostructures, the $Si_{1-x}Ge_x/Si$ heterostructure is compatible with silicon processing technology. The merging of silicon VLSI processing and heterojunction technologies has the potential to increase the performance of silicon electronics. The formation of heterostructures in silicon based materials does, however, rely on the growth of strained layer alloys in order to create the heterostructure. The fabrication of such strained layers requires growth temperatures far below standard epitaxial growth temperatures. The typical temperature range for growing strained $Si_{1-x}Ge_x$ on silicon is 450 - 650 °C. The low temperatures needed to for the strained layers will be discussed further below, but it is worth noting that this temperature range corresponds to a surface reaction limited growth regime where silicon and $Si_{1-x}Ge_x$ growth rates depend exponentially on substrate temperature. The reduced temperatures needed for the growth of strained layers is also advantageous for the growth of ultra-thin epitaxial layers with abrupt interfaces. Low temperature chemical vapor deposition has proven to be an effective way of growing high quality epitaxial layers with several advantages over other low-temperature growth techniques such as molecular beam epitaxy. Three items are important for the growth of high performance heterostructures; 1) interface abruptness; 2) temperature measurement; and 3) high purity.

STRAINED LAYER GROWTH

As mentioned above, it is imperative to optimize the growth temperature for each layer of the heterostructure in order to form a high quality interface. Low temperatures (450 - 650 °C) are typical for the growth of metastable strained layers. Unlike III-V materials, silicon lacks a compatible lattice-matched, band gap-mismatched semiconductor with which a heterojunction can be formed, therefore, the silicon material system must rely on strained layer alloys for the formation of defect free heterojunctions. When Ge is added to the silicon lattice during CVD growth, a compressive strain is created in the lattice forcing the $Si_{1-x}Ge_x$ to the in plane silicon lattice constant. The strain which is introduced to the system causes a reduction in the $Si_{1-x}Ge_x$ band gap resulting in the discontinuity needed for the heterostructure [3]. The presence of this strain requires the use of low growth temperatures for the formation of defect free interfaces. A tremendous amount of energy is stored in the compressed bonds, and the energy builds with the growing layer. The bonds will, however, remain strained as long as sufficient energy is not provided to drive the system to relaxation [4] forming defects at the heterointerface. The energy needed to drive the system to relaxation can be provided by growing thick layers of $Si_{1-x}Ge_x$ or by external sources. We will not discuss the growth of thick $Si_{1-x}Ge_x$ layers for relaxed layer growth. By reducing the growth temperature of the strained layer, the excess energy added to the system by external sources is minimized and defect formation avoided.

Low temperatures are also required to suppress three-dimensional growth of the alloy films [5]. Three dimensional growth is characterized by island formation on the wafer surface and leads to non-abrupt interfaces between adjacent epitaxial layers. Two dimensional growth (layer-by-layer) is obtained by reducing the growth temperature [6].

INTERFACE ABRUPTNESS

Interface abruptness is divided into two separate issues. The first is to defeat dopant inter-diffusion between layers. To grow thin layers of alternating doped and undoped materials with abrupt interfaces, one may grow the layers at a high temperature and hence a high growth rate whereby reducing the time a sample is allowed to see high temperatures. A second method is to reduce the growth temperature of the epitaxial layer whereby reducing the dopant diffusion (which depends exponentially on temperature) and increasing the time for which to grow the layers. Given the high activation energy for dopant diffusion (~3.5 eV) compared to growth (~2 eV), the choice of reduced growth temperature becomes apparent. The SUPREM simulation of Figure 1 demonstrates the different profiles obtained when attempting to grow alternating layers of boron doped ($N_A = 10^{18}$ cm^{-3}) material and intrinsic material with layer thicknesses of 10 nm. The 10 nm layers are still defined when grown at 800 °C (0.02 μm/min) where as the layers grown at 1000 °C (0.25 μm/min) are smeared with little distinction between the different layers. A growth temperature of 800 °C is the approximate maximum temperature for growing epitaxial layers with interface abruptness on the order of 1 nm. The reduced growth rate associated with the low temperatures also has the added benefit of allowing precise control over layer thicknesses on the 10 nm scale.

A second issue related to interface abruptness is germanium surface segregation. Since the band gap discontinuity occurs at the $Si_{1-x}Ge_x/Si$ interface, the abruptness of this interface is of extreme importance for heterojunction bipolar transistors. A phenomenon associated with MBE grown $Si_{1-x}Ge_x$ shows that Ge segregates to the growing surface and slowly incorporates into adjacent layers causing a grading of the germanium profile into adjacent layers. Secondary Ion Mass Spectrometry studies show that this grading effect can be as large as 17 nm/dec for MBE grown materials [7]. This grading affects HBT performance in that it pushes the emitter-

base heterojunction into the emitter region whereby it eliminates increased injection efficiency gained by HBT's. This segregation effect is not seen in RTCVD grown $Si_{1-x}Ge_x$ as is shown in Figure 2. The absence of germanium segregation is attributed to a hydrogen passivation of the growing surface during CVD; a property not found in Si-MBE.

TEMPERATURE CONTROL

Temperature control is critical for growth in the surface reaction limited regime where growth rates depend exponentially on temperature. Precise control of temperature is critical for the growth of strained $Si_{1-x}Ge_x$ layers in this temperature range. Many of the properties of silicon are temperature dependent and are measurable during growth. Two of the largest effects are those of band gap narrowing and increased carrier concentration with increased temperature. At room temperature, silicon is transparent to both 1.3 μm and 1.5 μm light [8], but as the temperature of the silicon is increased, the silicon becomes increasingly opaque at these wavelengths due to high free carrier absorption and valence band to conduction band absorption. As benchmarks, the band gap of silicon at 600 °C is approximately 0.93 eV (1.33 μm), at 700 °C ~0.89 eV (1.39 μm) and at 750 °C ~0.87 eV (1.42 μm) with intrinsic carrier concentrations of 2×10^{17}, 5×10^{17} and 8×10^{17} cm^{-3}, respectively. Since the absorption edge of silicon is not abrupt with respect to energy, we can measure the increase in temperature of the wafer due to a gradual decrease in transmission of infrared light. Figure 3 shows the temperature dependence of the absorption coefficient of silicon at 1.3 μm and 1.5 μm in the temperature range of 400 to 800 °C.

The increased phonon population (needed for band to band absorption) [9] and band gap narrowing with increased temperature first push the absorption edge above the 1.3 μm wavelength [9]. The effect is a decrease in 1.3 μm transmission through the wafer with an increase in temperature. A further increase in temperature decreases the 1.5 μm transmission which is due mainly to free carrier absorption [10]. The final result is a temperature probe of 400 to 650 °C with 1.3 μm light and 600 to 800 °C with 1.5 μm light.

The intensity of the light transmitted through the substrate depends exponentially upon the wafer thickness according to:

$$I(T,d) = I_0K(1-R)^2\exp[-\alpha(T)d] \qquad [1]$$

where I(T,d) is the intensity of light transmitted, I_0 is the incident intensity, R is the reflectivity ((1-R) varies by less than 2% over the temperature range of 200 to 700 °C), α(T) is the temperature dependent absorption coefficient and d is the wafer thickness. K is a geometrical factor which includes backside surface scattering and light collection efficiency, which is assumed to be a constant of the system for a given wafer. For applications to RTCVD, the transmitted intensity is normalized by the room temperature transmission signal. This normalization eliminates K and $(1-R)^2$ from Eqn 1. which can be expressed as:

$$t(T,d) = \exp[-\alpha(T)d] \qquad [2]$$

where t(T,d) is the normalized transmission ratio. An absolute temperature scale for temperature normalization was determined with a thermal couple welded to the surface of a 440 μm thick silicon substrate (d_{std}). The normalized transmission data for the 440 μm wafer is shown in Figure 4. The normalized transmission data is easily extended to substrates of arbitrary thickness (d_{sub}), by examining Eqn. 2 and the following relationship:

$$\log[t(T,d_{sub})] = \frac{d_{sub}}{d_{std}} \log[t(T,d_{std})] \qquad [3]$$

where $t(T,d_{sub})$ is the normalized transmission ratio of the test sample at a given temperature and $t(T,d_{std})$ the normalized transmission ratio of the calibration substrate. This relationship makes this measurement technique extremely powerful since it can be used on wafers of arbitrary thickness. Eqn. 3 also illustrates the accuracy of this technique during epitaxial growth. An error in thickness of 5 μm corresponds to a ~1 °C temperature error in the range near 600 °C. Since typical layer thicknesses in $Si_{1-x}Ge_x$ HBT's are on the order of 1 μm for silicon and less than 100 nm for $Si_{1-x}Ge_x$ the result is a very small error in temperature during growth. The normalization technique also eliminates errors associated growth on patterned wafers. The precise control of temperature afforded by this technique insures run to run reproducibility and stable control during long growth periods in the surface reaction limited regime of growth.

OXYGEN CONTAMINATION

Classical limitations of CVD come from part per billion (ppb) contamination of oxygen and water vapor in the gas flows. At temperatures below 850 °C oxygen sticks to the silicon surface. This leads to defects in the epitaxial films due to precipitate formations at the interface, as well as high oxygen concentration in the epitaxial films. In general, the films are of poor crystalline quality as well as poor electrical quality. According to ultra-high vacuum (clean surface) experiments, in order to maintain a clean silicon surface at 750 °C, the background partial pressure of oxygen must remain less than 10^{-8} Torr [11]. This corresponds to a carrier gas purity of better than 1 ppb O_2 if growth is to occur in an ambient pressure of 10 Torr. This restriction is beyond available gas purifiers. The UHV experiments also determine the sticking coefficient (probability) for oxygen on a clean silicon surface to be 0.01. We find that the conditions imposed by the UHV experiments to be too pessimistic to describe growth by CVD. We have determined the sticking coefficient during CVD growth at 6 Torr to be reduced by approximately two orders of magnitude.

We conducted oxygen doping experiments to determine the sticking coefficient of oxygen during CVD by intentionally introducing controlled amounts of oxygen into the reactor environment during growth. The oxygen incorporation efficiency is defined by the ratio of the flux of oxygen incorporated in the growing film and the oxygen partial pressure in the reaction chamber. The efficiency plotted in Figure 5 is temperature independent and demonstrates that oxygen incorporation in this temperature range is kinetically limited. Using this information, it can be determined that to grow silicon films at 750 °C (~50 nm/min) which contain oxygen concentrations of less than 10^{18} cm^{-3}, the gas purity must be less than 100 ppb, a value within the limits of gas purifiers. (The value of 10^{18} cm^{-3} is chosen to correspond to the approximate peak solid solubility of oxygen in silicon. The surface concentration of oxygen for this incorporation level is approximately two order of magnitude lower than that detectable by the UHV clean surface experiments.)

We believe that the reduction in oxygen sticking during CVD growth is due to boundary layer effects as well as a hydrogen passivation of the silicon surface. Figure 6 shows the fraction of open sites on a silicon surface as a function of temperature with a hydrogen overpressure of 6 Torr calculated from simple thermodynamic principles. One sees that the surface is still approximately 90% covered with hydrogen at 750 °C. At higher hydrogen pressures, the surface coverage increases. The boundary (stagnant) layer formed during CVD growth reduces the amount of oxygen which can interact with the substrate surface. This has the effect of reducing the effective sticking coefficient even if the true sticking coefficient (hydrogen passivation) is unchanged. The effective sticking coefficient is reflected in the efficiency plotted in Figure 5. This reduction in the sticking probability for oxygen during CVD growth is fortuitous since it enables one to grow high quality, low-oxygen content films at temperatures below the classical limit. Figure 2 also shows a typical oxygen profile for a $Si_{1-x}Ge_x$ layer grown at 625 °C in a non-UHV environment. The oxygen concentration is at the detection limit of SIMS.

CONCLUSION

To grow high quality $Si_{1-x}Ge_x$ layers by CVD, temperatures in the range of 450 °C to 650 °C are required to provide abrupt $Si/Si_{1-x}Ge_x$ interfaces, and to minimize dopant inter-diffusion between adjacent layers the temperature can be increased to 800 °C. Temperature control is critical in this range due to the exponential dependence of growth rate on temperature. Because of a reduced sticking coefficient for oxygen during CVD growth, growth temperatures below the classical limits can be utilized.

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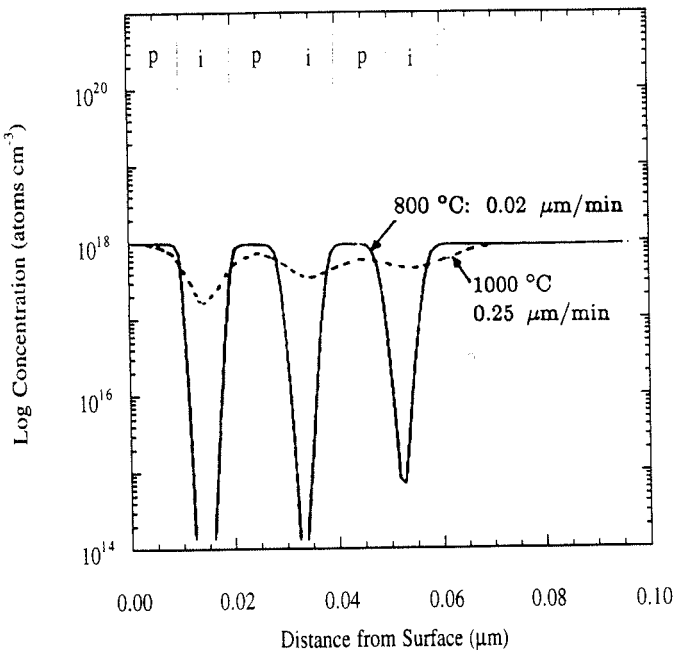

Figure 1. SUPREM simulation of the growth of alternating 10 nm layers of boron doped material and intrinsic material. The dotted line corresponds to 1000 °C growth and the solid line corresponds to 800 °C growth. The layers are still well defined in the 800 °C growth.

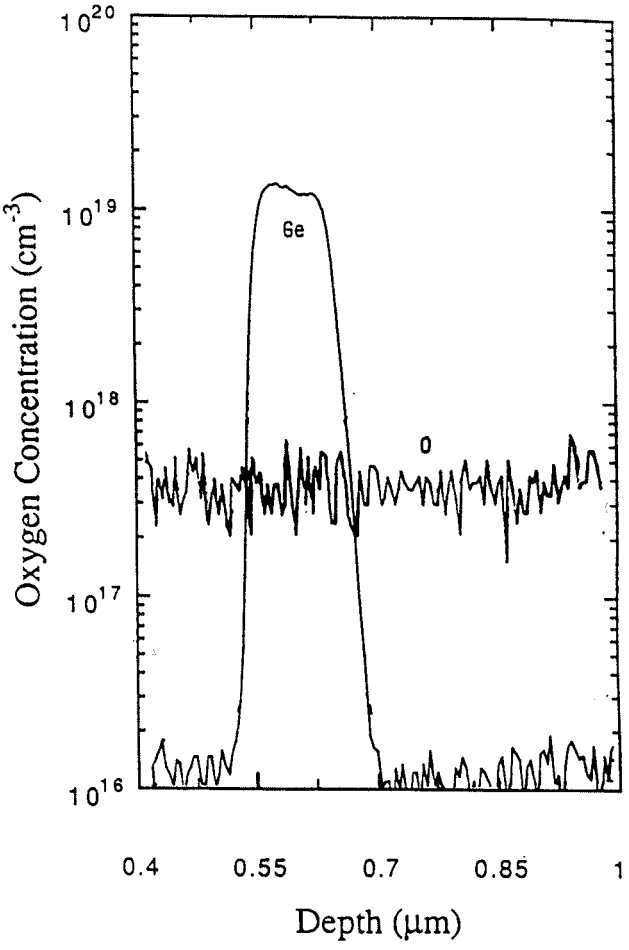

Figure 2. SIMS profile of RTCVD grown $Si_{1-x}Ge_x$. No surface segregation is seen in RTCVD material as seen in MBE grown material hence well defined interfaces can be formed by CVD. The oxygen concentration is limited by the detection limit of SIMS.

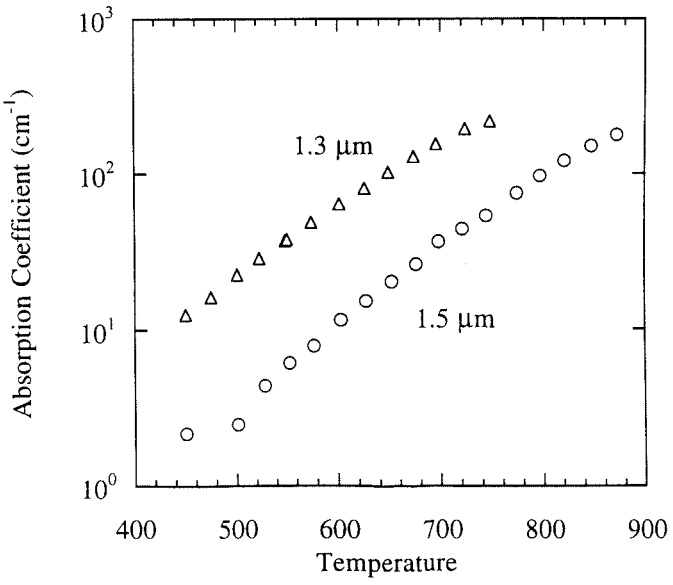

Figure 3. Temperature dependence of the absorption coefficient of silicon at 1.3 μm and 1.5 μm. The gradual increase in absorption with increasing temperature allows for precise control of wafer temperature during growth.

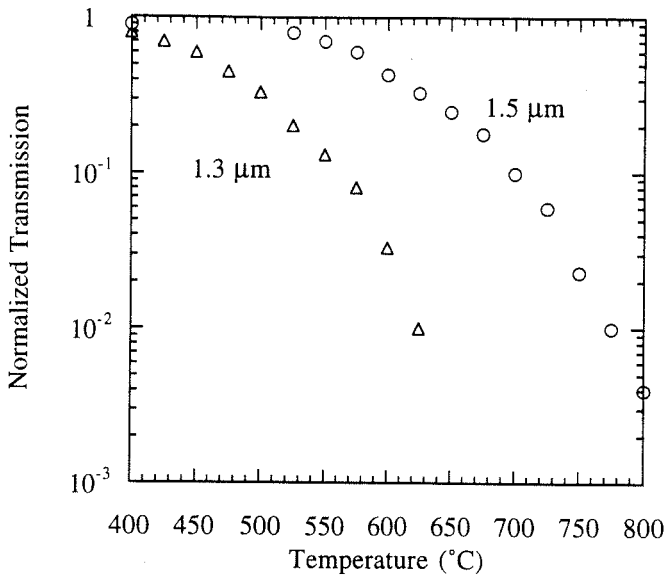

Figure 4. Normalized transmission data for a 440 μm thick silicon wafer in a temperature range from 400 to 800 °C. The 1.3 μm light is attenuated at lower temperature while the 1.5 μm light is attenuated at higher temperatures.

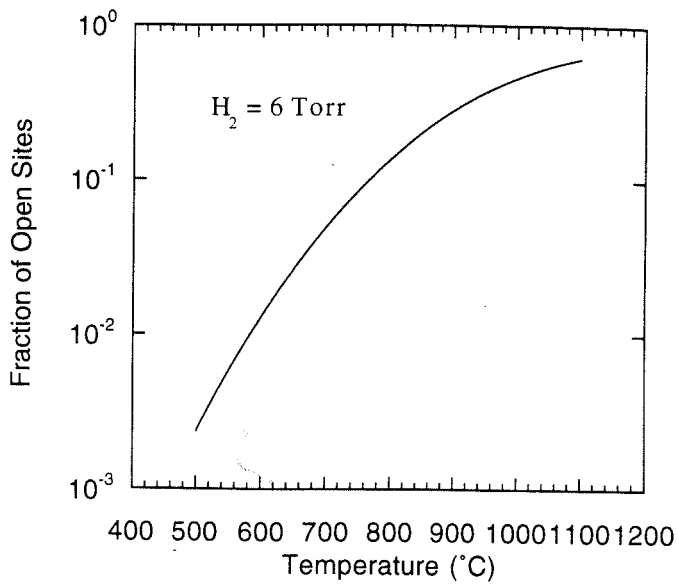

Figure 6. Calculated fraction of open sites on a silicon wafer as a function of temperature with a hydrogen overpressure of 6 Torr. The hydrogen passivation of the silicon surface reduces the number of sites on which oxygen can adsorb.

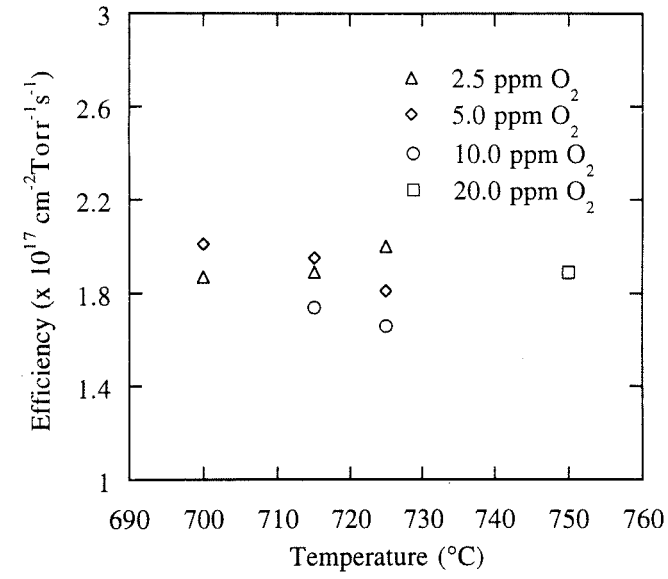

Figure 5. Oxygen incorporation efficiency during CVD growth of silicon films. In this temperature range oxygen incorporation is kinetically limited.