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Structure of oxygen-doped silicon grown by chemical-vapor deposition at low temperature

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The relation between the structural quality of Si:O layers grown by chemical-vapor deposition at low temperatures (700–750 °C) and electrical properties was determined. Transmission electron microscopy (TEM), secondary-ion-mass spectroscopy, and resistivity measurements were used for this study. An oxygen concentration in these layers was in the range of 6×10^{-19}–6×10^{-20} cm^{-3}. TEM studies have shown that amorphous SiO_x precipitates were formed at the lower interface (between the Si buffer and Si:O layer) when silane was used for the layer growth. Slightly smaller precipitates were distributed through the entire layer. In the layers with higher oxygen concentration, high density of stacking faults originated at the same interface and propagated through the entire layer. The Si capping layer grown on top of Si:O was monocrystalline with the density of stacking faults two orders of magnitude lower than in the Si:O layer. For the lower oxygen concentration the stacking faults were not formed and the size of precipitates at the lower interface and in the layer was much smaller. The resistivity of $\sim10^5$ and $\sim10^6$ Ω cm was measured in the layers with lower and higher oxygen content, respectively. Only for the Si:O layers grown in the same range of temperatures (700 °C) using dichlorosilane oxygen induced stacking faults were formed at the upper interface (between Si:O and the capping layer). Some small precipitates were formed at the lower interface but no visible precipitates were present in the Si:O layer. These layers were not semi-insulating. It was concluded that the mechanism to explain semi-insulating properties might be related to the presence of the SiO_x precipitates or structural defects present in these layers.

I. INTRODUCTION

Semi-insulating substrates are desirable for high-speed electronics. It is known that polycrystalline silicon can be made semi-insulating by the addition of large amounts of oxygen (>10%), such as in SIPOS (semi-insulating polycrystalline silicon) films.[1] Similar large amounts of oxygen have also been previously incorporated into crystalline silicon by molecular-beam epitaxy, with a goal of wide band-gap layers for emitters for heterojunction bipolar transistors.[2] Recently, it has been shown[3] that oxygen-doped crystalline silicon films can also be grown by chemical-vapor deposition (CVD) at low temperature, with oxygen levels on the order of 10^{-20} cm^{-3}. In these films it was found that the Fermi level was pinned near midgap and room-temperature resistivities of 10^6 Ω cm were observed. It was also noticed using Fourier transform infrared spectroscopy that the absorption peak in the CVD Si:O layers was shifted to an energy lower than that of the interstitial oxygen and had a larger width than expected for interstitial oxygen. This shift and line broadening is similar to the spectra obtained in oxygen-doped silicon epitaxial films where $SiO_{1.5}$ precipitates were used to explain these changes.[4] Unfortunately, the studies of CVD Si:O layers were not accompanied by structural studies to detect structural defects caused by the high oxygen levels. Therefore, the main purpose of this article is to show how the structural properties of these layers are related to the growth conditions and their electrical properties.

II. EXPERIMENT

In this work oxygen was used as a dopant during low-temperature chemical-vapor deposition of epitaxial silicon. Three different sets of samples with a slightly different growth condition were investigated. All epitaxial layers were grown in a susceptor-free, lamp-heated, chemical-vapor deposition system.[5] The SI:O layers were grown on (100) silicon substrates that were chemically cleaned prior to loading into the reaction chamber. The wafers were cleaned *in situ* at 1000 °C in a 250 Torr hydrogen ambient for 60 s. After the growth of an epitaxial Si buffer layer at 1000 °C using dichlorosilane (DCS), the temperature was lowered to the low growth temperature of 700 °C (or 750 °C) over a period of approximately 1 min without switching of the DCS. After another 1 min at 750 °C, the oxygen was switched on (and simultaneously DCS was switched off and silane switched on in samples with silane growth). All of the gas flows were established into vent lines before switching them into the reactor to minimize switching transients due to slow mass flow controller (MFC) response times ("vent/run" configuration). The vent line for the silicon source gases was at a low pressure like the reactor, but the vent line for the oxygen was at atmospheric pressure. Therefore, an overshoot

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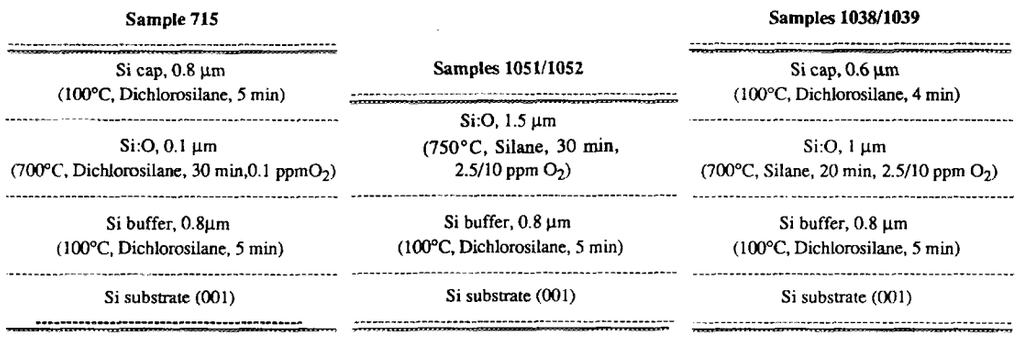

FIG. 1. Cross section of samples used in this study. The oxygen concentration in the hydrogen carrier during growth was 2.5 ppm in samples 1051 and 1038, and 10 ppm in samples 1052 and 1039.

in the oxygen flow probably occurred for several seconds after the oxygen was switched into the reactor, since this would have suddenly increased the pressure differential across the oxygen MFC. The Si:O layers were grown either using the same gas or using silane (SiH_4) as silicon source gas, and oxygen (O_2) was introduced as an oxygen source (0.1–10 pm of the carrier). The oxygen level in the gas for each sample is shown in Fig. 1. For some of the samples capping layers of pure silicon were grown on the top of Si:O layers at 1000 °C to form active areas of devices. For these samples, at the end of the growth of the oxygen-doped layers the oxygen was switched off (and silane switched off and DCS simultaneously on); the low growth temperature was maintained for 1 min; and finally, the temperature was raised (with DCS on) to 1000 °C. The electrical characteristics of metal–oxide–semiconductor field-effect transistors (MOSFETs) built on these structures showed that the oxygen-free silicon forming the active region on top of the Si:O has a mobility similar to that in virgin silicon substrates.[3]

The samples were divided into three different pieces and one part was used for secondary-ion-mass spectroscopy (SIMS) studies in order to determine the oxygen concentration in these layers; the second part was used for electrical characteristics in order to determine resistivity of these layers and Fermi-level pinning; and the third part of these layers was used for transmission electron microscopy studies in order to determine their structural quality.

III. SIMS RESULTS

The oxygen concentration in two of the samples was determined by SIMS. The oxygen level in the Si:O layer (sample 715) grown at 700 °C with DCS (0.1 ppm O_2 in the hydrogen carrier) was on the order of 6×10^{-19} cm^{-3}. For sample 1051, grown at 750 °C with silane (2.5 ppm O_2 in the hydrogen carrier) the oxygen level was 1.4×10^{-20} cm^{-3}. The concentration in sample 1052 (the same as sample 1051 but 10 ppm O_2) was not measured. However, previous work has shown that the oxygen incorporation for samples grown in this range is determined by a simple kinetic mechanism. The oxygen level is proportional to the oxygen concentration in the gas and inversely proportional to the growth rate,[6] as oxygen desorption under these conditions is negligible. Therefore, we estimate an oxygen concentration of 6×10^{-20} cm^{-3} in sample 1052. The oxygen level in the Si:O layers of samples 1038 and 1039 was not measured, but they were grown under identical conditions as those in samples 1051 and 1052, respectively. The relatively high concentration of oxygen in sample 715 for such a small O_2 flow is explained by the very low growth rate of this sample (due to the lower growth temperature and the dichlorosilane source gas) compared to samples 1051 and 1051 (~3 versus ~50 nm/min).

IV. TEM RESULTS

Transmission electron microscopy (TEM) was used to determine the structural perfection of the grown Si:O layers as well as the capping layers. Plan-view and cross-sectioned samples were studied using a 002B Topcon instrument with an acceleration voltage of 200 keV and point-to-point resolution of 0.17 nm. Cross-section samples were prepared from all samples by the conventional method of gluing two samples layer to layer together and cutting a 2 mm thick strip, which was first mechanically polished and then ion milled to obtain electron transparency. The structure of the studied Si:O layers was drastically different. It was found that Si:O layers grown at low temperature are very sensitive to the oxygen concentration introduced during the growth. Very good agreement between the layer thickness estimated by crystal growers and TEM results were obtained for all samples. In sample 715 a 0.15 μm thick Si:O layer followed by an 0.85 μm thick Si cap layer was determined by TEM, instead of 0.1 and 0.8 μm determined by crystal growers. The oxygen concentration of 6×10^{-19} cm^{-3} caused the formation of stacking faults in these samples. TEM study of plan-view samples showed the stacking faults arranged in most cases as squares of the equal size of 1250 nm [Fig. 2(a)]. Their density was determined as 1.3×10^{7} cm^{-2}. Similar defects were observed in bulk silicon during high-temperature oxidation,[7,8] in silicon-on insulator structures (SOI)[9] or in silicon separated by oxygen structure

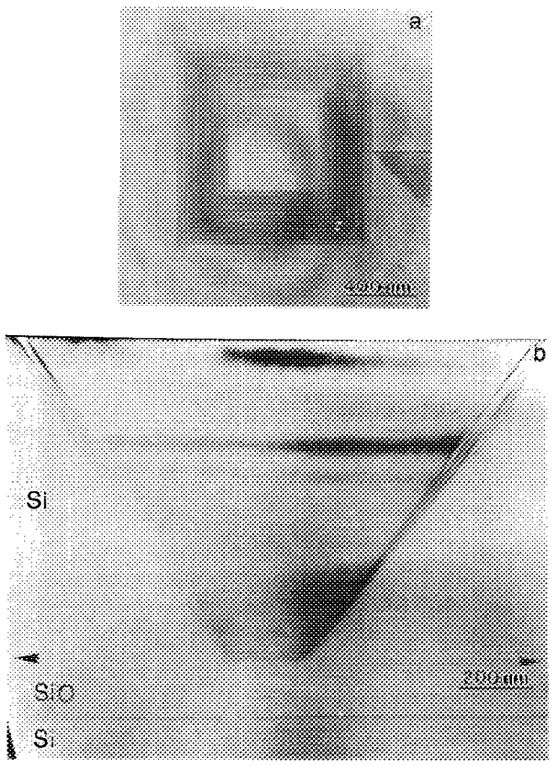

FIG. 2. (a) TEM micrograph of plan view of sample 715 showing formation of extrinsic stacking faults; (b) similar stacking faults shown in cross-section sample in (011) projection. Note their origination at the top of the Si:O layer.

(SIMOX)[10] and are called oxidation induced stacking faults (OISF). These squares are formed due to formation of stacking faults on four different (111) planes. They originate at the upper interface between the Si:O layer and at a cap Si layer grown at 1000 °C [Fig. 2(b)]; propagate on the oblique (111) planes to form a tetrahedron; and intersect the growth surface as squares in the (100) oriented layers. In Si:O layers these OISF were determined as extrinsic type and they most probably originate from small silicon oxide precipitates formed at the upper interface between the Si:O and the capping layer. Accumulation of silicon oxide precipitates was observed in all samples at the lower (Si/Si:O) interface where the growth temperature was lowered. However, in sample 715 this phenomenon was not so clearly observed since the precipitate size was not larger than 1 nm. Some larger defects were occasionally observed within the layer. It is assumed that some precipitates agglomerate at the upper interface when the growth temperature was increased, since all of the stacking faults originate at this interface and, therefore, have the same dimension.

For sample 1051, with a Si:O layer grown at 750 °C using silane with a higher oxygen content of 1.4×10^{-20} cm^{-3}, stacking faults were not formed. Agglomeration of SiO_x precipitates of about 2–3 nm in diameter with a separation between them of about 1 nm were found at the interface between the buffer layer and the Si:O layer [Fig. 3(a)]. Much

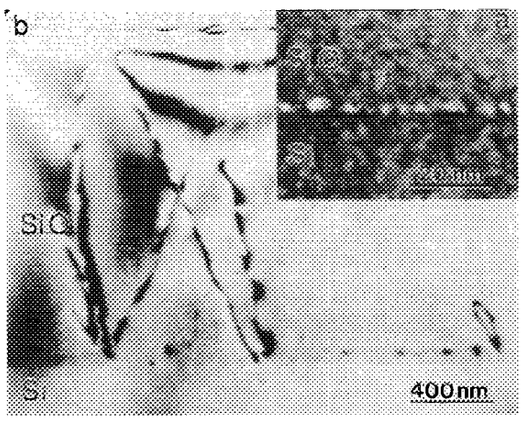

FIG. 3. (a) Accumulation of SiO_x precipitates at the lower interface between the buffer layer and the Si:O layer in sample 1051; (b) formation of hairpin disclocations and the dislocation loops at the same interface.

smaller precipitates uniformly distributed were present in the entire layer. Occasionally, dislocation loops which extended to hairpin dislocations originated at these interface as well [Fig. 3(b)]. These hairpin dislocation extend to the top of the layer and their density was estimated as 5×10^{10} cm^{-2}. The layer thickness measured from TEM micrographs was 1.6 μm, in good agreement with expected thickness estimated from the growth rate (1.5 μm).

Sample 1052 was grown in the same condition as sample 1051, but with 10 ppm instead of 2.5 ppm O_2 during the Si:O growth. As in previous sample, heavy decoration by SiO_x precipitates was observed in this sample. However, in this case, the size of precipitates was roughly two times larger than in sample 1051. A high density of stacking faults ($\sim10^{11}$ cm^{-2}) was formed at the interface with a buffer layer [Fig. 4(a)]. These stacking faults were almost uniformly distributed through the entire layer [Fig. 4(b)]. In the immediate vicinity of stacking faults, some of the precipitates increased their size up to 15 nm in diameter and in the areas between these stacking faults, the size of the precipitates was comparable or slightly smaller than those formed at the interface.

The defect arrangement in samples 1038 and 1039 in the entire Si:O layer is identical to sample 1052. However, the cap Si layers were grown on the top of 1 μm thick Si:O layer in these samples. An interaction between the stacking faults and some annihilation was observed at the interface with the capping layer (Fig. 5). However, some faults propagated through the cap layer. Their density in the capping layer was two orders of magnitude lower than in the Si:O layer. As was expected, precipitates were not present in the capping layer. No accumulation of the precipitate distribution was observed at the interface with the capping layer.

V. ELECTRICAL RESULTS

Resistivity measurements of the Si:O layers on samples 715, 1051, and 1052 were made between aluminum contacts on the top surface (area=6×10^{-3} cm^2) and the substrate. The aluminum contacts were used as a mask to etch mesas to isolate individual devices. The $I-V$ curves were rectifying

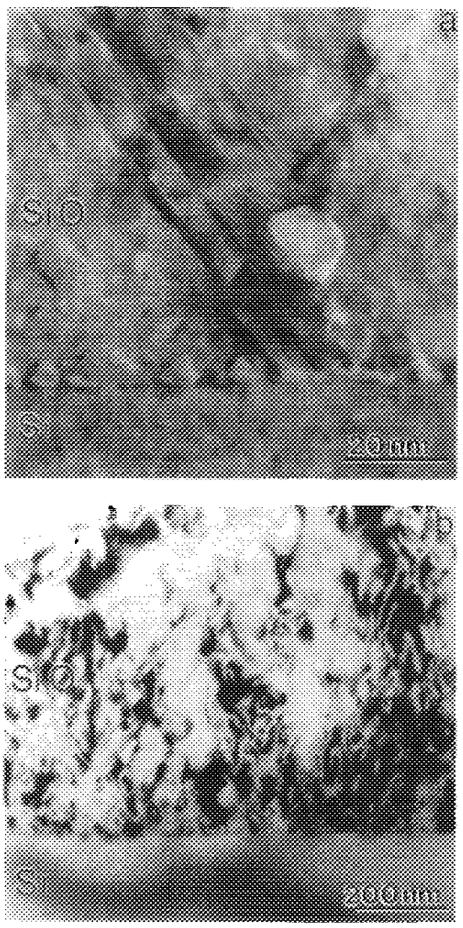

FIG. 4. (a) Accumulation of SiO_x precipitates and origination of stacking faults at the lower interface between the buffer layer and the Si:O layer in sample 1052. Note much larger precipitates in the vicinity of stacking faults and the presence of precipitates in the Si:O layer; (b) low magnification of the same sample showing high density of stacking faults and precipitates in the entire layer.

on samples 1051 and 1052, with a negative bias on the top contacts required for forward bias (Fig. 6). Note the much smaller current levels on sample 1052, indicating a larger resistance in the Si:O layer. Considering that the substrates and buffer layers were doped with boron (p-type), this rectification is consistent with a Schottky barrier model for the devices. The resistivity of the Si:O layers were extracted from the parasitic resistance in the forward bias part of the $I-V$ curves, and it was assumed that the entire thickness of the Si:O layer contributed to the resistance. A resistivity of $\sim 10^5$ and $\sim 10^6$ Ω cm were found on samples 1051 and 1052, respectively. Temperature-dependent measurements on other samples grown under similar conditions shown that the conductivity is thermally activated with an activation energy of 0.6 eV.[3] This suggests that the Fermi level in these samples is pinned near the middle of the silicon band gap, either from the oxygen itself or from structural defects resulting from oxygen. Semi-insulating behavior was not observed in sample 715. This is thought to be due to the fact

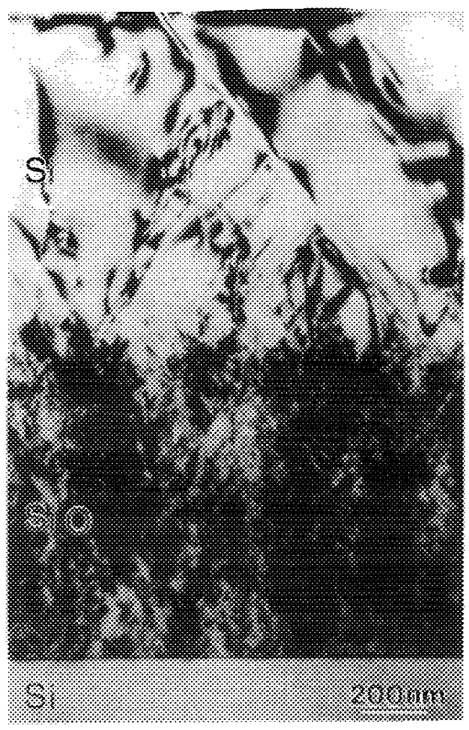

FIG. 5. Defect distribution in sample 1039 with a similar growth condition as in sample 1052. Note that the density of stacking faults in the Si capping layer decreases drastically.

that the Si:O layer was very thin (~ 0.1 μm) and that the Si layers above and below this layer were highly doped (10^{18} cm^{-3}) with boron. During the 1000 °C growth of the top Si layer, high levels of boron would have diffused throughout the Si:O layer and destroyed any semi-insulating properties.

VI. DISCUSSION AND CONCLUSIONS

A clear dependence between the oxygen concentration (as well gas used for the growth) and the structural quality of the Si:O layers was observed. The most striking observation is a heavy decoration of the lower (Si/Si:O) interface by SiO_x

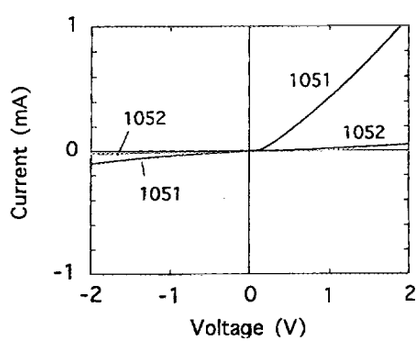

FIG. 6. $I-V$ curves for Schottky barriers of area 0.6×10^{-3} on samples 1051 and 1052.

precipitates when silane was used for the layer growth. This is related to higher oxygen concentration due to an overshoot in the oxygen flow. The entire layers grown with silane had a high density of precipitates. Their size drastically increased with the oxygen concentration in hydrogen carrier increased from 2.5 to 10 ppm during growth. These precipitates were amorphous and electron-energy-loss spectroscopy (EELS) data confirmed the presence of oxygen in these samples. However, even with the help of diffraction patterns obtained on these layers, it was very difficult to confirm if these precipitates are SiO_2 or if their composition is slightly different. In the sample with the highest level of oxygen (sample 1052), a high density of stacking faults originating from the lower interface and propagating through the entire layer was observed, which was not seen in a similar sample grown with lower oxygen content (sample 1051).

For the samples grown using DCS (sample 715), lowering the temperature to the similar range (700 °C) does not lead to such heavy decoration of the lower interface. In this sample formation of stacking faults was observed at the upper interface where the growth temperature was increasing, similar to what was observed in SIMOX samples.[7–9] No visible precipitates were observed in the Si:O layer grown at 700 °C using DCS. One needs to notice that semi-insulating behavior was not observed in this sample.

It is clear that the Si:O layers grown at 750 °C using silane with a high density of SiO_x precipitates have semi-insulating properties. Some similarities between the semi-insulating properties of these novel Si:O layers and the GaAs layers grown at low temperature with As precipitates can be considered. However, SiO_x precipitates are not metallic; therefore, the buried Schottky model might not directly apply in this case. A high density of surface states or fixed charge at the precipitate/Si interface, as is common at poor SiO_2/Si interfaces, could still lead to a pinned Fermi level and semi-insulating properties, however.

Alternatively, it is possible that the high density of SiO_x precipitates (an almost continuous layer up to 5 nm thick) observed at the interface in four studied samples due to an overshoot in the oxygen flow was sufficient to produce the insulating properties of these layers or that a high density of structural defects (precipitates and stacking faults) strongly decreases the carrier mobility due to excess scattering.

Semi-insulating properties were reported as well in GaAs due to void formation after Al implantation.[11] High sheet resistivity of these layers was observed after annealing at 700 °C. The temperature dependence of the sheet resistivity was also measured to determine the effective thermal activation energies of the compensation levels. They were 0.48 and 0.67 eV for the 800 °C anneals and 0.32 and 0.56 eV for the 900 °C anneals. Similarly, deep traps at $E_c-0.55$ eV and $E_c-0.71$ eV that were stable for Si and Se-implanted GaAs have been observed.[12] In the present studies, the effect of amorphous SiO_x precipitates in their properties could be very close to the voids observed in the GaAs, which suggests that the Fermi-level pinning is most probably associated with the presence of these precipitates.

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