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SiGe Single-Hole Transistor Fabricated by AFM Oxidation and Epitaxial Regrowth

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Nanodevices on Si/SiGe heterostructures are of growing interest [1-2]. Si-based quantum dot devices may provide a physical route to achieve quantum computing [3-4]. However, how to fabricate Si-based quantum dots free from interface states is still a great challenge. The high-energy processes of electron-beam lithography and reactive ion etching (RIE), and the presence of SiO_2-passivated surfaces may all lead to damage, defects, and/or interface states, which will degrade the performance of the devices. In this paper, we demonstrate a reproducible single-hole transistor SiGe device fabricated by an approach which allows one to avoid high-energy processing steps and which does not use SiO_2 for passivation. The patterning of the SiGe dots is achieved by AFM oxidation and wet etching, and the epitaxial regrowth of silicon is used for passivation.

Figure 1 shows the nanopatterning process used to pattern 10nm-thick p-type SiGe layers: Anodic oxidation occurs when a negative bias is applied between AFM tip and the sample (Fig. 1a). Dissociated OH^- ions from water vapor react with top Si surface to form SiO_2 [5]. The minimum feature size is < 20 nm [6]. Since the maximum oxidation thickness is less than 3 nm on Si or SiGe, it is difficult to use AFM directly pattern device layers. Therefore, a two wet-etching step has been developed. First, diluted HF is used to remove the SiO_2 (Fig. 1b). Then selective wet etching of SiGe over Si transfers the nano-scale patterns into the relative-thick SiGe layer (Fig. 1c). Due to isotropic wet etching, final lithography resolution is reduced to ~ 50 nm.

Quantum-dot single-hole transistors have been fabricated by above method on Si/SiGe heterojunctions. Figure 2 shows a quantum dot structure after (a) AFM oxidation and (b) selective wet etchings. The pattern was transferred into ~ 10nm-thick p^+-SiGe layer conducting at low temperature. This device has two planar gates (consisting of the same SiGe layer), which can tune Femi-level of the center dot and potential barriers at the two-narrow regions between

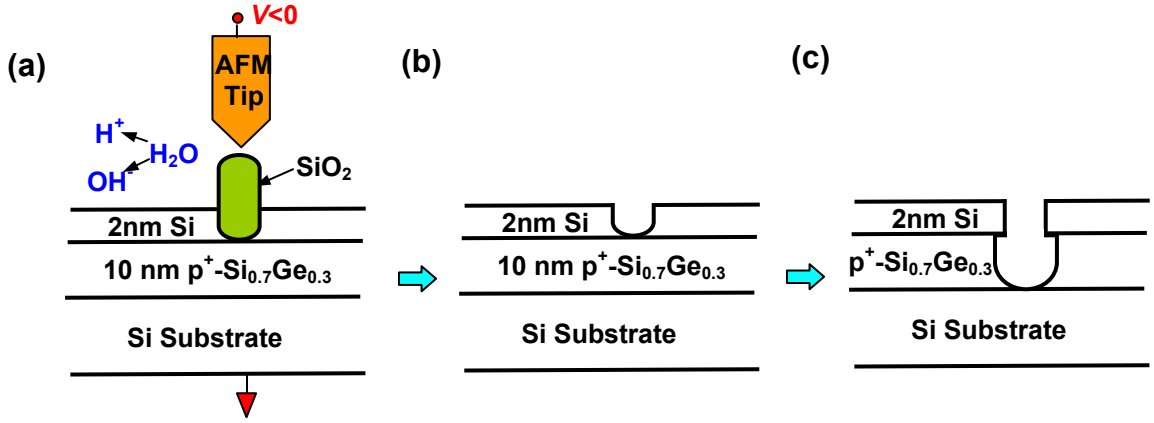

Figure 1. Nanopatterning process of Si/SiGe heterostructures: (a) Si cap AFM oxidation: water dissociated into ions by negative bias on the AFM tip, and reacted with Si to form SiO_2; (b) HF dip to remove SiO_2; and (c) selective wet etching to pattern SiGe layer.

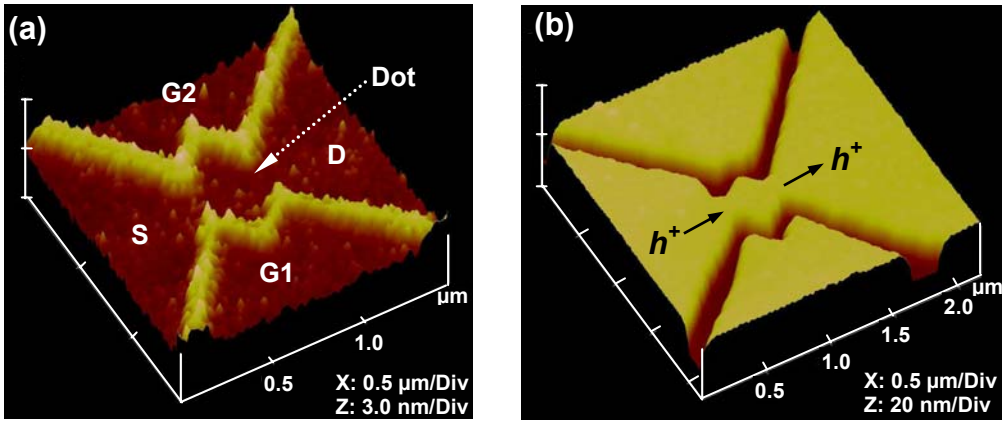

Figure 2. (a) Quantum dot device after AFM oxidation on top thin Si cap; (b) after two-step selective wet etching. S, D, G1, and G2 indicate source, drain, and side gates, respectively.

source/dot and drain/dot. After two-step etching, this device exhibits coulomb blockade oscillations. However, the etched regions of the device are exposed to the air and thus are passivated by the native oxide. Trapping and detrapping in the interface cause the device current/voltage measurement to be unrepeatable and differ on each scan [6].

Rokhinson *et al* [1] demonstrated an ultra-small silicon dot device with MOSFET structure. Although the transport channel is passivated by high-temperature thermal oxide, interface states between Si and amorphous SiO_2 cause the device with one lithographically-defined dot to show double-dot transport characteristics [1]. This is because carriers can also move in and out of the interface states, in addition to in and out of the desired dot. In contrast, the Si/strained SiGe interface in principle can be free of dangling bonds or defects. Thus carriers confined in Si/SiGe heterojunctions might not see any interface states. Therefore we seek to passivate the strained SiGe dot of Fig. 2, previously patterned by AFM oxidation, by silicon epitaxial regrowth. The regrowth was done by RTCVD at 700 °C, preceded by an 800 ºC bake in hydrogen, which is sufficient to provide a clean interface [7]. Photoluminescence spectra indicate the interface between the SiGe and the regrown Si is comparable to that grown without interruption.

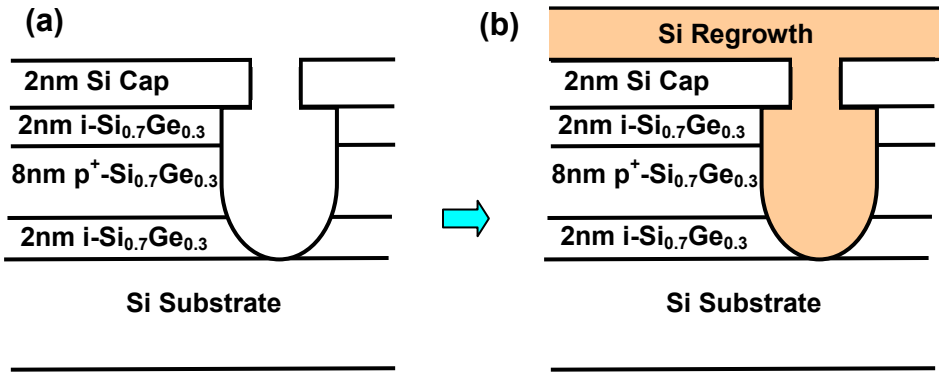

Figure 3. SiGe nanodevices (a) pattered by AFM oxidation and wet etching, and (b) passivated by silicon epitaxial regrowth to eliminate interface states.

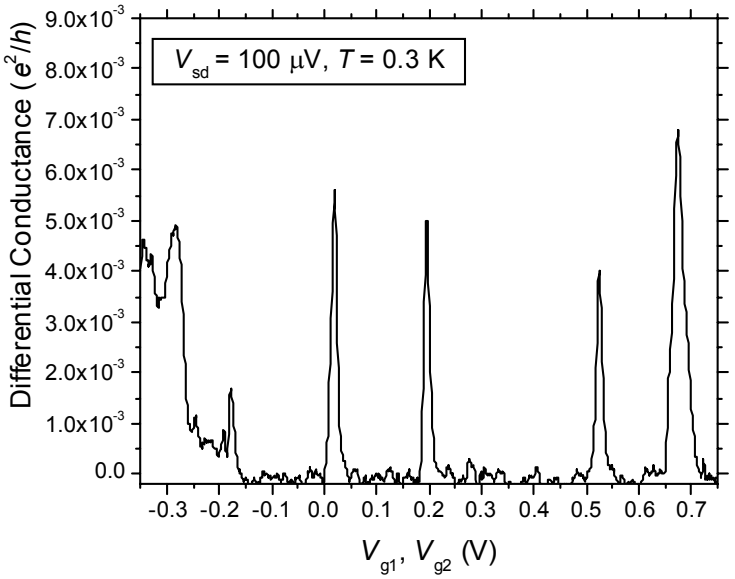

Figure 4. Quantum dot conductance with both gates connected in parallel at source/drain bias of 0.1 mV and temperature of 0.3 K.

A SiGe quantum dot device passivated by silicon regrowth was measured at T = 0.3 K (Figure 4). With both gates connected together, the dot conductance shows very sharp oscillations at source/drain bias voltage of 100 μV, which is believed due to coulomb blockade. A single hole tunnels in/out of the dot only when one energy state of the dot aligns with the Femi-levels of source and drain. Otherwise, tunneling is prohibited due to the high coulomb energy separating energy levels in the dot. In contrast to our previous work, the curves are now very reproducible. Furthermore, the oscillations are very similar at various close bias voltages and temperatures < 1.4 K. This suggests that the passivation of silicon epitaxial regrowth greatly reduces the interface states and their effect on dot operation. Further work is in progress to analyze the exact spacing of the oscillations.

In summary, AFM oxidation plus epitaxial regrowth passivation by RTVCD is an attractive path for the fabrication of Si-based quantum devices free from defects and interface states. Devices fabricated by this approach have been demonstrated for the first time, and single-hole tunneling quantum-effect of the devices is reproducible.

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