

**Si_{1-x-y}Ge_xC_y Alloys: An Enabling Technology for Scaled
High Performance Silicon-Based Heterojunction Devices**

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Abstract

Si/Si_{1-x}Ge_x heterostructures have traditionally faced both fundamental and practical limitations in their applications to advanced device technology. These hurdles have been most significantly been the well known critical thickness limitation for pseudomorphic growth and the less known sensitivity of devices to heterojunction process integration. In this talk, we will review how Si_{1-x-y}Ge_xC_y alloys grown by rapid thermal chemical vapor deposition (RTCVD) are an enabling technology to overcome both these fundamental and practical issues. Examples will be shown for sub-100-nm MOS devices.

Introduction

Since the mid-1980's there has been a strong interest in the fundamental properties and the applications of Si/Si_{1-x}Ge_x heterostructures. Most of the work has been directed towards strained layers (pseudomorphic growth) on Si(100) substrates. This substrate orientation has been chosen since it is the one most widely used in industry, and pseudomorphic growth has been pursued since it allows one to grow layers without misfit dislocations. While RF devices with figures of merit well over 100 GHz have been demonstrated [1,2], over this period of time, the following fundamental and practical limitations of the material system of pseudomorphic Si_{1-x}Ge_x/Si have become clear [3]:

- (i) The limit on the critical thickness imposed by the strain in pseudomorphic epitaxy greatly limits potential applications.
- (ii) Device integration is difficult since dopants must generally stay within a few nm of their as-grown position for successful device operation.
- (iii) There is a negligible conduction band offset for pseudomorphic Si_{1-x}Ge_x on Si(100) substrates, especially for Ge fractions less than 50%.
- (iv) The cost of epitaxy, even using chemical vapor deposition, seriously detracts from the attractiveness of applications.

Over the past few years, it has been found that the addition of a few atomic percent of C to form Si_{1-x-y}Ge_xC_y or Si_{1-y}C_y alloys allows one to overcome all of these disadvantages of the Si_{1-x}Ge_x/Si (100) material system (assuming the carbon is on

substitutional lattice sites). This paper will explicitly address the first, second, and fourth of these advantages. For information about the large conduction offsets in the $\text{Si}_{1-y}\text{C}_y/\text{Si}$ (100) material system, the reader is referred to Ref's. 4 and 5. Although we have previously demonstrated the application of SiGeC layers to advanced bipolar structures [6,7], in this paper we will demonstrate these advantages through application to advanced MOSFET structures.

$\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers can be grown by chemical vapor deposition by the addition of a carbon-containing gas source (e.g. methylsilane) to the usual gas sources used for SiGe layers [8]. All samples reported in this paper were grown by Rapid Thermal Chemical Vapor Deposition using methylsilane, germane, dichlorosilane, and/or silane sources in a hydrogen carrier [9]. Typical growth temperatures were 625 °C. Low growth temperatures are necessary for the carbon to incorporate on substitutional sites, since carbon has a very low equilibrium solid solubility in Si.

Strain Reduction and Critical Thickness

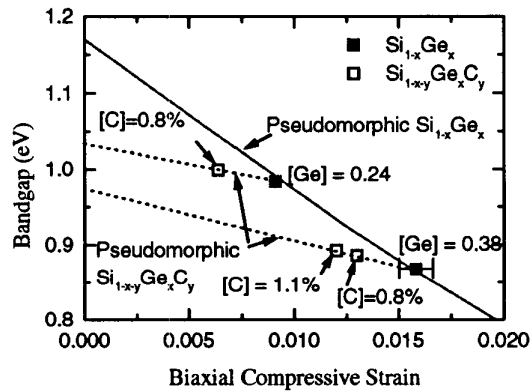


Figure 1. Bandgap vs biaxial compressive strain for pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ and $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers on $\text{Si}(100)$ substrates [12].

The limitations placed on strained $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ (100) heterojunction engineering by the strain in pseudomorphic layer are well known. For example, to achieve a 100 meV bandgap reduction to Si, a Ge fraction of ~ 0.13 is required, with an equilibrium critical thickness of only ~ 25 nm (Fig. 1). In the early growth of $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$, it was established that the small size of the carbon atom leads to a reduction in the tensile strain of pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ layers on $\text{Si}(100)$ substrates as C is added to form $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers [10], with each carbon atom compensating for the strain of 8-10 germanium atoms. Several years later as the quality of the materials improved, the effect of carbon on the bandgap was measured. As carbon is added to $\text{Si}_{1-x}\text{Ge}_x$ layers under compressive strain on $\text{Si}(100)$, the bandgap increases as carbon is added at a rate of ~ 25 meV per percent of carbon [6, 11, 12], so that adding one carbon atom has the same effect on bandgap as

removing three germanium atoms. This relatively slow rate of increase of bandgap as strain is reduced through the addition of carbon leads to lower strain and thus a higher critical thickness for a given bandgap for $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ compared to that for $\text{Si}_{1-x}\text{Ge}_x$ (Fig. 1, Fig. 2) [12,13]. This implies the bandgap for strain-free alloys lattice-matched to silicon is significantly less than that of silicon, which has been confirmed [14]. Adding 1% of C (and slightly increasing the Ge fraction) for our above target of a 100 meV bandgap change with respect to Si, a $\text{Si}_{0.83}\text{Ge}_{0.16}\text{C}_{0.01}$ layer would have a critical thickness of ~70 nm vs the 25 nm without carbon. If the carbon fraction were increased to a level of 0.02, the critical thickness of the $\text{Si}_{0.79}\text{Ge}_{0.19}\text{C}_{0.02}$ layer, also with a bandgap shift from Si of 100 meV, would be nearly one micron [13].

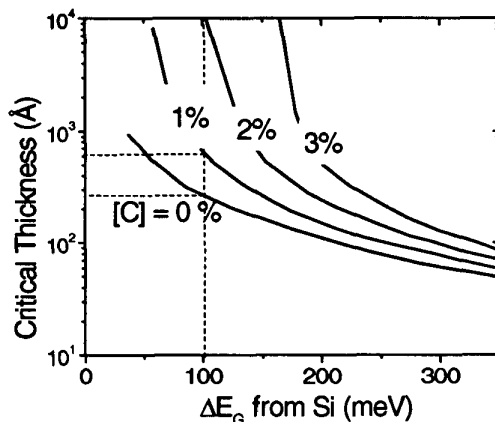


Figure 2. Critical thickness vs bandgap shift from silicon for compressively strained pseudomorphic $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers on Si (100) for 0, 1% and 2% carbon [13].

Dopant Diffusion

For proper operation, many advanced devices depend of the placement of dopant atoms within a few nm with respect to a heterojunction. While structures with such resolution can be routinely grown in silicon-based materials by both MBE and CVD techniques at temperatures less than 700 °C, processing steps such as oxidation, anneals of ion implantation damage, etc., are typically required to integrate devices into existing VLSI processes. These steps can easily lead to dopant diffusion of 10 nm or more, even at temperatures of 750 °C or less, vastly degrading device performance [7, 15, 16]. In many practical examples, this limitation on the thermal budget is far more severe than that for strain relaxation, and hence it is a major stumbling block towards the realization of large-scale circuits with silicon-based heterojunction devices. Over the last few years, it has been found that the diffusion of some dopants, especially boron, can be reduced by an order of magnitude or so (compared to pure Si or $\text{Si}_{1-x}\text{Ge}_x$) by the incorporation of only low levels of substitutional carbon to form $\text{Si}_{1-y}\text{C}_y$ or $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ alloys [7,17].

Even more interesting, it appears that the diffusion coefficient is reduced not only in the $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layer itself, for example, but also in nearby regions of pure Si [7, 18]. This is shown in Fig. 3 using a structure grown by RTCVD with two marker layers of highly-boron-doped silicon layers designed to measure the reduction of oxidation enhanced diffusion of boron (OED) [18]. OED is caused by the injection of interstitial Si atoms, which are necessary for the diffusion of boron. One boron layer is above and one is below a $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ region designed to capture interstitials, which are introduced from the surface during oxidation. While the exact mechanism is not well understood, it appears that substitutional C creates a sink for Si interstitials, which are required for the diffusion of dopant atoms such as boron. By reducing the local interstitial concentration, diffusion coefficients can thus be reduced. Note in Fig. 3 that in the control sample without any SiGeC (Fig 3(a.)) there is a substantial increase in the diffusion coefficient when the samples are annealed in oxygen as opposed to in nitrogen. Modelling the SIMS curves show an increase of the diffusion coefficient by nearly an order of magnitude. In the sample of Fig. 3(b.), a $\text{Si}_{0.8}\text{Ge}_{0.2}\text{C}_{0.005}$ layer was inserted between the boron marker layers. In this sample no OED was observed for the lower boron peak, showing that all of the injected interstitials were effectively captured. Transient-enhanced-diffusion (TED) in silicon is caused by the injection of interstitials resulting from implantation damage, and

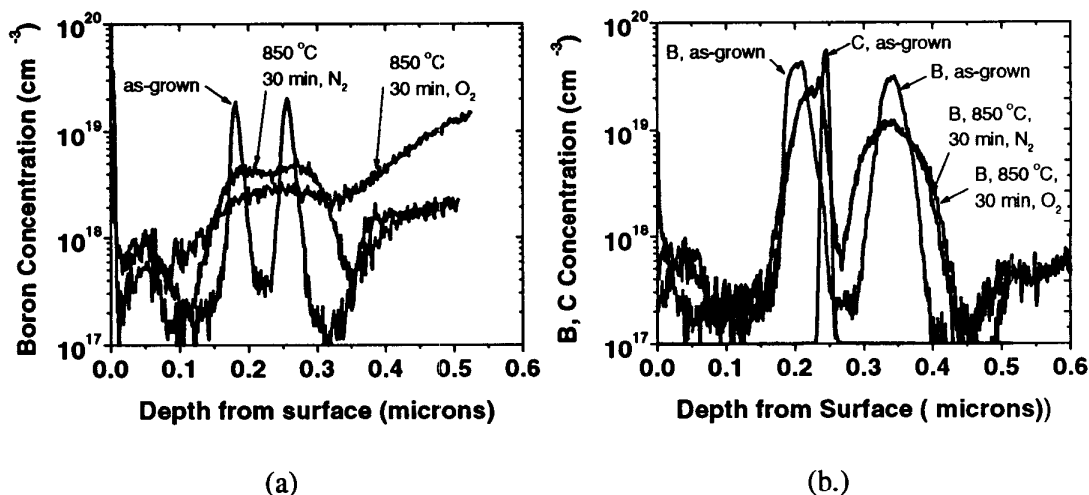


Figure 3. SIMS of boron and carbon levels (C as-grown only) in buried marker layers as-grown and after annealing at 850 °C in either N_2 or O_2 in (a.) control sample with no SiGeC and (b.) sample with SiGeC layer between the two boron layers. Note the elimination of OED in the lower boron-doped layer in sample (b.) [18].

can cause a similarly large anomalous increase in boron diffusion. Because TED relies on an interstitial mechanism, it can similarly be avoided using SiGeC layers to block interstitials [18].

Sub 100-nm Si MOSFET's

One attractive approach for deep-micron Si MOSFET's is a vertical structure, where the thickness of epitaxial layers is used to control the channel length [19]. A vertical wall is formed either by etching or by selective epitaxy, and then the sidewall is oxidized and then coated with polysilicon to form the gate. In such structures, especially p-channel, a severe lower limit on the channel length is the diffusion of the source-drain dopant (e.g. boron) during the sidewall oxidation step to form the gate oxide. For example, Fig. 4 shows the boron SIMS profile of an all-silicon vertical $p^+ - n - p^+$ structure to be used for such vertical FET's, both as-grown and after the growth of 10 nm of gate oxide at 750 °C. While the initial boron profiles are very sharp, suitable for scaling the channel length well below 100 nm, after the short gate oxidation cycle at even the low temperature of 750 °C, the boron has diffused so much that no device with a channel length below 200 nm is feasible. Note that in the literature, no p-channel vertical FET has been reported with a channel length less than 0.2 μm [20] unless a gate oxidation step other than atmospheric pressure thermal oxidation is used [21].

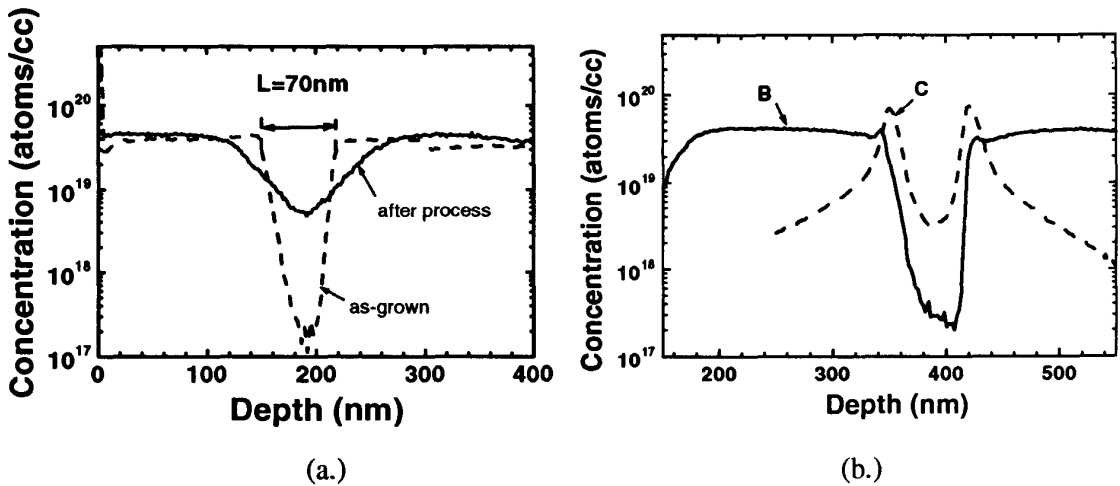


Figure 4. Boron and carbon SIMS profiles of $p^+ - n - p^+$ structures for vertical FET's. In (a.), no SiGeC layers were introduced, and profiles as-grown and after 750 °C gate oxidation are shown. In (b.) SiGeC layers are incorporated into the source drain region to suppress boron diffusion, and only the profile after the same gate oxidation step is shown. Note the improvement in the B profile [22,23]

Simulation showed that most of the diffusion due to the gate oxidation was due to OED effects. Therefore thin SiGeC layers were placed in the source drain region of the FET to suppress the diffusion of the dopant in the source drain [22]. In this case, negligible diffusion of the boron was observed after gate oxidation, so that the devices could be scaled to short channel lengths. I-V curves of FET's with an n-type channel doping of $\sim 2 \times 10^{18} \text{ cm}^{-3}$ are shown in Fig. 5. The channel length is defined as the distance

between the points at which the boron levels (as measured by SIMS) begin to drop from their high values in the source/drain regions. At a channel length of 70 nm the devices are well-behaved and have off currents at a drain voltage of 1 V of ~ 1 pA. Good on/off characteristics are still observed at a channel length of 40 nm, although some signs of punchthrough (due to inadequate phosphorous channel doping) are evident.

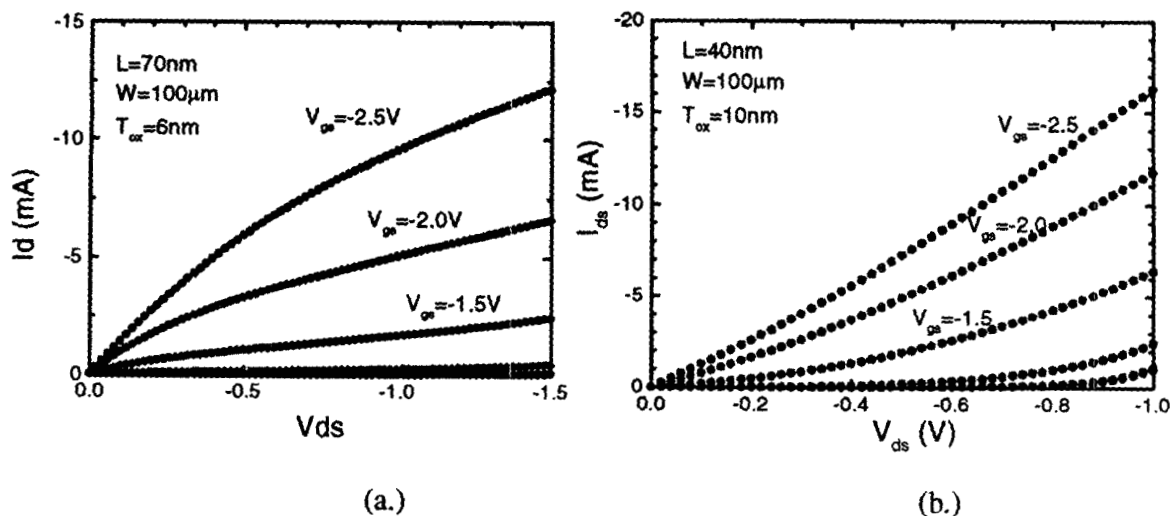


Figure 5. I-V curves of (a.) 70-nm and (b.) 40-nm vertical p-channel MOSFET's with SiGeC layers in source-drains to prevent boron diffusion [22].

Boron Penetration in p^+ Polysilicon Gates

The penetration of boron from p^+ polysilicon gates through the gate oxide into the channel region during the source/drain anneal is a serious scaling problem for short-channel p-channel MOS devices. Such boron-doped gates are desirable for symmetric threshold voltages in CMOS and also for the ease of fabrication of a CMOS process with a single layer of polysilicon for the gates of both p-channel and n-channel devices. When boron penetrates the gate oxide into the channel region, it causes an undesirable positive shift in the threshold voltage of the devices. To suppress this effect, we investigated the use of thin (20 nm) $\text{Si}_{0.8}\text{Ge}_{0.2}\text{C}_{0.005}$ or $\text{Si}_{0.8}\text{Ge}_{0.2}$ polycrystalline layers placed above the gate oxide underneath the usual polycrystalline silicon gate (~ 300 nm) in MOS capacitors with a gate oxide thickness of 9-10 nm. All polycrystalline layers were deposited undoped, and then the top polysilicon surface was implanted with 60 keV BF_2^+ at a dose of 5×10^{15} cm^{-2} , resulting in a boron profile approximately 0.1 μm deep. The samples were then annealed at 900 $^\circ\text{C}$ for various times to drive the boron through the polycrystalline layers. The threshold voltage was then measured by C-V measurements on MOS capacitors (n-type substrates) to evaluate any shifts due to boron penetration through the gate oxide. The details are reported elsewhere [23], but one of the main results is presented in Fig. 6. It shows the threshold voltage as a function of anneal time for an all-Si control structure,

and structures with either a SiGe or SiGeC blocking layer of 20 nm thickness. The superiority of the sample with the SiGeC blocking layer is clear. While boron penetration through the gate oxide is effectively suppressed with the $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ blocking layer, quasi-static C-V measurements indicate that gate depletion did not occur for negative gate biases, indicating a high boron doping in the SiGeC layer, a result supported by SIMS. The seeming contradiction between the high boron concentration in the SiGeC layer adjacent to the gate oxide and ability of the SiGeC to block boron penetration through the gate oxide implies that that boron tends to segregate into the SiGeC layers, which thus suppresses its diffusion into the silicon substrate. The underlying mechanism is under investigation, but the effect of any bandgap offset caused by the carbon is not expected to be important because of the small level of C (< 1%) used in these experiments. Besides the importance of the boron penetration problem, these results are also significant because they demonstrate a potential application of $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers without the need for epitaxial growth.

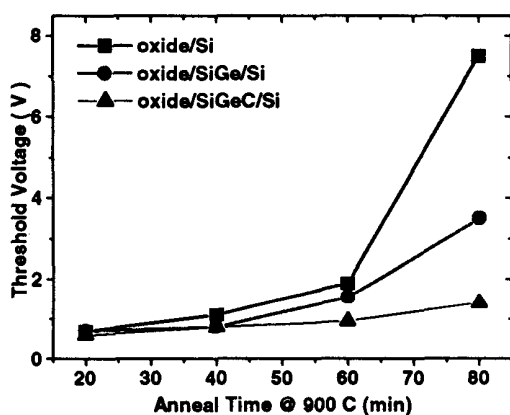


Fig. 6. Threshold voltage vs. anneal time for capacitors with different gate electrode structures: polysilicon gate; SiGe barrier layer + poly-Si gate; SiGeC barrier + poly-Si gate [23].

Summary

In summary, $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers are attractive for overcoming the longstanding critical thickness and dopant diffusion limitations which have severely limited the widespread application of the Si/Si_{1-x}Ge_x material system to date, most notably the critical thickness limitation and the sensitivity of devices to dopant diffusion during process integration. Besides their usual role in heterojunction bipolar transistors, this material system has potential applications to ultra-short channel MOS transistor technology and also to photonic devices.

Acknowledgement

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