1999 EMC At-A-Glance

Wednesday Morning, June 30, 1999

8:30 AM — **EMC PLENARY LECTURE/STUDENT AWARDS**

Room: Corwin Pavalion

Plenary Speaker: Shuji Nakamura, Nichia Chemical Industries, Ltd., R&D Dept., 491, Oka, Kaminaka Anan, Tokushima Japan

Topic: "Present and Future Prospects of InGaN-Based Blue LEDs and LDs"

Break: 9:30 AM - 10:00 AM

Session A. Semiconductor Quantum Dots-Devices

Room: Multicultural Center Theater

10:00 A1, Gain and Emission Characteristics of MOVPE Grown InP/GaInP Quantum Dot Lasers
..... Thomas Riedl

10:20 A2, 4 Watt High Power Quantum Dot Lasers
..... M. Grundmann

10:40 A3, Electroluminescence of Stacked In(Ga)As/GaAs QDs at 1.3 mm-1.4mm
..... Frank Heinrichsdorff

11:00 A4, Collisional Carrier Kinetics and Broadening of Spectral Lines Quantum Dot Structures
..... Alexander V. Uskov

11:20 A5+, Direct Bandgap Materials for Monolithic Optical Interconnects on Silicon
..... Victoria Ann Williams

11:40 A6, Late News

Session B. Materials Integration-Substrate Fabrication and Bonding

Room: State Street

10:00 B1+, Fabrication of Thin Film InGaN LED Membranes by Laser Liftoff
..... William S. Wong

10:20 B2+, GaN LEDs Transferred to Copper Substrates Using Laser Assisted Debonding
..... Philip R Tavernier

10:40 B3+, A Comparison of Wet and Dry Chemistries for Hydrophobic Silicon Wafer Bonding
..... James B. Mattzela

11:00 B4+, Deposition of Borosilicate Glasses by Low Pressure Chemical Vapor Deposition Using Tetraethylorthosilicate and Trimethylborate
..... Darren Michael Hansen

11:20 B5, Ion-cutting of GaSb Wafers
..... Y. Zheng

11:40 B6, Late News

Session C. Characterization, Growth and Properties of Organic Electronic Materials

Room: Santa Barbara Harbor Room

10:00 C1, Dependence of Emission Quantum Yield on Chain Packing in Electroluminescent Polymers
..... Lewis J. Rothberg

10:20 C2+, Near-Field Scanning Optical Microscopy of Conjugated Polymer Films
..... Jessie A. DeAro

10:40 C3, CPAFM: A Tool for Nanoscale Structure and Electronic Properties
..... Tommie Wilson Kelley

11:00 C4+, Growth of Thermally Evaporated Pentacene Films on SiO_2
..... Jonathan Andrew Nichols

11:20 C5, Nanoscale Investigation of the Optical Properties of Tris-8-Hydroxyquinoline Aluminum Films (Alq_3)
..... Grace M. Credo

11:40 C6, Late News

1999 EMC At-A-Glance

Wednesday Afternoon, June 30, 1999

Session G. Epitaxy for Devices

Room: State Street Room

1:30 G1, Tellurium Memory Effects on OMVPE-grown In0.3Ga0.7As0.997N0.003/GaAs Laser Diodes
..... Nein-Yi Li

1:50 G2+, Investigation of p-type GaInNAs for Heterojunction Bipolar Transistor Base Layers
..... Huoping Xin

2:10 G3 +, Growth and Characterization of Long Wavelength (1 micron) GaInAsN Photo-detectors using Gas Source Molecular Beam Epitaxy
..... Sudhir G. Subramanya

2:30 G4, InGaAsN for High Efficiency Solar Cells Grown by Metalorganic Chemical Vapor Deposition
..... Andrew A. Allerman

2:50 G5, Late News

3:10 Break

3:30 G6+, AlGaAs and InGaAs-based Light Emitters on Si via Relaxed Graded GeSi Buffer Layer
..... Michael E Groenert

3:50 G7+, Lattice Matched $Zn_xBe_{1-x}Te$ Films with GaAs and ZnSe for p-Contact Layers of ZnSe-Based II-VI Laser Diodes
..... M. W. Cho

4:10 G8, Selective InAs Contact to GaAs
..... Kumar Shiralagi

4:30 G9+, Development of Multi-functional InGaAs-based Ohmic Contacts for GaAs Devices
..... Mitsumasa Ogura

4:50 G10, Use of Multi-quantum Wells for Photoabsorption Enhancement in Compound Semiconductor Solar Cells
..... Yoshitaka Okada

Session H. Electronic Transport in Organic & Molecular Materials

Room: Santa Barbara Harbor Room

1:30 H1*, What Determines the Resistance of a Molecule?
..... Supriyo Datta

2:10 H2, Simulation of Molecular Devices from First-Principles
..... Massimiliano Di Ventra

2:30 H3+, Electronic Transport Characteristics Through Diisocyanide
..... Jia Chen

2:50 H4, Improved Contacts for Organic Electronic Devices Using Self-Assembled Charge Transfer Materials
..... Jianna Wang

3:10 Break

3:30 H5*, High Mobility Charge Transport in Aromatic Hydrocarbon Single Crystals
..... Jan Hendrik Schön

4:10 H6, High Mobility Polymer Thin Film Transistors Based on Copolymers of Thiophene and 3-Hexylthiophene
..... Jianna Wang

4:30 H7+, Contact Limited Performance of Pentacene Thin Film Transistors
..... David J. Gundlach

4:50 H8, Late News

Session I. Column IV Heterostructures and Devices

Room: Flying A Studios

1:30 I1+, Exploitation of Facet Formations in SiGe/Si Selective Epitaxial Growth for Achieving a Nanometer Template
..... Greg D. U'Ren

1:50 I2+, Selective Si Epitaxial Growth Using Ultrathin Oxide Mask Formed By Resistless Patterning
..... Shawn G. Thomas

2:10 I3, Electrical and Structure Characterization of Single Crystalline SiGe Formed by Ge Deposition and RTP
..... Y. H. Wu

2:30 I4, Surfactant Mediated Epitaxy of Ge/Si Heterostructures for Device Applications
..... Karl R. Hofmann

2:50 I5+, Direct Growth of Ge on Si for Integrated Si Microphotonic Photodetectors
..... Hsin-Chiao Luan

3:10 Break

3:30 I6+, Boron Segregation in Polycrystalline Si(1-x-y)Ge(x)C(y) Alloys
..... Eric Jonathan Stewart

3:50 I7, X-Ray Diffraction and Transmission Electron Microscopy Study of the Development of Texture in Polycrystiallin $Si_{1-x}Ge_x$ Thin Films
..... Wei Qin

4:10 I8, Diamond Epitaxy for Electronic Devices
..... Aleksandar Aleksov

4:30 I9+, Epitaxial Growth of Si/Y2O3/Si: A Potential SOS Structure
..... Michael Edward Hunter

4:50 I10, In Situ Observation of Epitaxial Co Silicidation on Si(001)
..... Kunihiro Sakamoto

Elect. Eng. East, University Park, PA 16802 USA; [2]The Pennsylvania State University, Dept. of Mats. Sci. and Eng., 103 Steidle Bldg., University Park, PA 16802-5005 USA

Because organic electronic materials are often sensitive to the chemicals used in photolithographic processing; devices fabricated by depositing the active organic material onto patterned source/drain contacts (photolithographically defined prior to the organic active layer deposition) are of interest. However, TFTs fabricated using pre-patterned bottom contacts often have reduced performance compared to devices fabricated using top contacts (typically deposited through a shadow mask)[1]. To improve our understanding of bottom contacts we have fabricated TFTs with pre-patterned source/drain contacts of platinum (Pt), palladium (Pd), gold (Au), nickel (Ni), and aluminum (Al) using heavily-doped, thermally-oxidized silicon as the substrate, gate dielectric, and gate electrode. All metals were deposited by ion beam sputtering to give high-quality, thin, smooth films, and contacts were defined photolithographically using a two-layer resist lift-off process. Pentacene, the active layer, was deposited by thermal evaporation. The surface morphology was monitored by atomic force microscopy (AFM) and the structural order was characterized by x-ray diffraction. TFTs fabricated using Pd, Au, or Pt source/drain contacts had the best performance with little difference observed between these relatively stable metals. Devices fabricated using Ni or Al contacts showed strong space charge limited current (SCLC) effects at small source-drain biases and reduced extrinsic mobility, possibly due to the presence of a native oxide for these less stable metals (in previous work we have observed only small work function related contact effects for shadow-masked top contacts). TFTs using Ni or Al as the source contact and Pd as the drain contact had characteristics similar to devices using Ni or Al for both the source and drain contacts. When the source/drain contacts were reversed (Pd as the source contact and Ni or Al as the drain contact), TFT performance was similar to TFTs fabricated using Pd for both the source and drain contacts. This indicates that carrier injection at the source contact can limit device performance and that carrier extraction at the drain contact is less problematic. Correlations between the electrical properties and structural properties revealed by AFM and x-ray diffraction will be discussed. 1. Y-Y. Lin, D. J. Gundlach, and T. N. Jackson, 54th Device Research Conference Digest, p. 80-81, June 1996.

4:50 PM Late News

Session I. Column IV Heterostructures and Devices

Wednesday PM Room: Flying A Studios
June 30, 1999 Location: University Center

Session Chairs: Eugene Fitzgerald, MIT, Cambridge, MA USA; Ya-Hong Xie, UCLA, Dept. of Mats. Sci. & Eng., Los Angeles, CA USA

1:30 PM +

Exploitation of Facet Formations in SiGe/Si Selective Epitaxial Growth for Achieving a Nanometer Template: *Greg D. U'Ren*[1]; Mark S. Goorsky[1]; Kang L. Wang[2]; [1]UCLA, Dept. of Mats. Sci. and Eng., 6532 Boelter Hall, 405 Hilgard Ave., Los Angeles, CA 90095-1595 USA; [2]UCLA, Dept. of Elect. Eng., 405 Hilgard Ave., Los Angeles, CA 90095-1594 USA

Gas-source molecular beam epitaxy was used to investigate facet formations occurring in the selective epitaxial growth of $_{1-x}Ge_x$/Si psuedomorphic heterostructures ($x \leq 0.2$). We carried out experiments on nominally on-axis (100) Si substrates masked with 50 - 60 nm thermally grown SiO_2. Arrays of wires varying in pitch (0.5 - 25 μm) were defined by optical lithography techniques. A sidewall orientation parallel to the <011> directions was used to exploit growth of {hkk}-type facets. Cross-section transmission electron microscopy was employed to monitor the development of both {311}-type and {111}-type facets as function of epi thickness and window size. Phemonologically similar to Si, facet growth in SiGe SEG initiates with the {311}-type, but it differs in that as growth proceeds it continues to dominate over the {111}-type facet by a ratio of 3:1. The {111} facet does nucleate and grow, but as the epi thickness increases it does not completely consume the {3 11} facet as would be expected if surface energy were the sole driving force. The combination of the {111} and {311} facet growth leads to an overall lateral reduction of the (100) mesa top at an estimated rate of 2-3:1[laterals reduction (x,y):epi thickness (z)]. The reduction rate accelerates due to the dominant {311} facet, which has a 1.6 larger projection onto the (100) surface than the {111} facet, more quickly promoting the lateral reduction. In this way, the lateral dimension can be reduced beyond the original lithographic definition, advantageous for fabrication of a nanoscale template, which can be then used for growth of SiGe heterostructures or a Ge island array. Triple axis x-ray diffraction measurements of the selective epi determined that the crystalline perfection is high and is not compromised by the presence of facet growth. For the 0.5 μm lateral features that had undergone the reduction process to fabricate a 15 nm template, a tri-axial stress-state was observed. Parallel to the array of periodic structures, the additional in-plane elastic relaxation as a result of the additional free surfaces was quantified. Experimentally, reciprocal space mapping of both symmetric and asymmetric diffraction geometries was carried out, and the results were compared to simulated contour maps generated using a kinematical approach that determined $\varepsilon_{xx} = (2 \pm 3) \times 10^{-5}$. The driving force for the mechanical response is the inherent misfit strain, in this example $\varepsilon_{zz} = 5.23 \times 10^{-3}$. Perpendicular to the array however, the selective epi is completely commensurate, i.e. $\varepsilon_{yy} \sim 0$. The in-plane asymmetry indicates an overall, but small, orthorhombic lattice distortion in the nanometer template.

1:50 PM +

Selective Si Epitaxial Growth Using Ultrathin Oxide Mask Formed By Resistless Patterning: *Shawn G. Thomas*[1]; Greg D. U'Ren[2]; Mark S. Goorsky[2]; Kang L. Wang[1]; [1]University of California, Los Angeles, Elect. Eng. Dept., 63-109 Eng. IV, Los Angeles, CA 90095-1595; [2]University of California, Los Angeles, Mats. Sci. and Eng. Dept., Los Angeles, CA 90095-1595

Previously, selective epitaxial growth (SEG) of InAs on GaAs has been demonstrated using a 1.5 nm thick oxide mask using the resistless patterning technique described by Shiralagi et al. [Applied Phys. Lett. 71 (20), 1997]. In this paper, we report the results of our efforts at selective Si homo-epitaxial growth using a 1.0 - 2.0 nm thick oxide mask using a similar patterning technique on Si and via gas source molecular beam epitaxy (GSMBE). Resistless patterning was carried out by placing a chrome mask over a hydrogen passivated Si wafer and exposing it to UV light (185 nm) in an ozone cleaner in a room air ambient. Selective growth was performed by GSMBE using disilane as the precursor. Prior to growth, the substrate was heated to a temperature of 615°C for hydrogen desorption. In an effort to maintain the integrity of the masking oxide, the in-situ thermal cleaning process was forgone, initiating Si deposition once the substrate reached a temperature of 615°C and with a (1x1) reconstruction. As growth proceeded, the (1x1) pattern began to assume a surface faceting character. For all experiments, the absence of Debye-Scherrer rings superimposed onto the (1x1) suggests that the SEG was completely selective for the thickest epi. No simultaneous growth of polycrystalline deposits on the masking layer suggests that the SiO_2 was of high quality and free of heterogeneities. The post-growth surface morphology was observed using Normanski interference microscopy and the masked and unmasked regions were clearly delineated. The step height was measured to be 140 - 150 nm, once again indicating a loss in selectivity beyond this thickness. Additionally, x-ray diffraction analysis was performed to gauge the crystalline quality of the SEG film. Based on our experiments, we have demonstrated that it is possible to use an ultra-thin oxide mask to achieve selective Si growth via GSMBE to thickness of 150 nm. Results of this study are compared to observations made in a CVD reactor using dichlorosilane where the presence of chlorine pre-

vents thicker Si growth. Possible applications of this simplified patterning technique and selective growth will be discussed.

2:10 PM
Electrical and Structure Characterization of Single Crystalline SiGe Formed by Ge Deposition and RTP: *Y. H. Wu*[1]; W. J. Chen[2]; Albert Chin[1]; C. Tsai[1]; [1]National Chiao Tung University, Dept. of Electr. Eng., Hsinchu, Taiwan ROC; [2]National Huwei Institute of Technology, Dept. of Mechanical Mats. Eng., Huwei, Taiwan ROC

SiGe alloys have been found to be a very promising material because of its potentially useful electronic and optical properties. In general, the SiGe/Si heterojunction can be grown by UHVCVD, MBE, or even by solid phase epitaxy from Ge ion implantation. However, UHVCVD or MBE require expansive equipment and Ge implantation-formed SiGe does not have a uniform Ge composition. In this work, we have presented a simple method to form single crystalline SiGe by depositing amorphous Ge on Si substrate followed by a rapid thermal annealing. Selective formation of SiGe can be also easily achieved by liftoff. Similar to MBE or UHVCVD epitaxy, the suppression of native oxide is of paramount importance to form epitaxial SiGe rather than the polycrystalline one. To overcome this problem, we have used HF-vapor treatment to passivate the Si surface and suppress the native oxide formation. From x-ray diffraction and TEM analysis, single crystalline SiGe is formed by this method with HF-vapor passivation. A uniform Si0.3Ge0.7 layer of ~50nm is confirmed by SIMS measurement. The crystalline quality is strongly degraded by native oxide that even becomes poly-crystalline structure. Similar quality improvement has been observed by us on ultra-thin oxide with an atomically smooth interface. To further investigate the practicability of this SiGe, we have fabricated PMOS transistor and MOS-capacitor to study its electrical characteristics. As comparing to standard Si-based PMOS, the SiGe PMOSFET showed increased output current Dr. by a factor of two. This current Dr. improvement is due to increased hole mobility. Peak mobility value of 251 cm2/Vs is measured in the SiGe PMOSFET that is about two times higher than Si. In addition to the high mobility, a low source/drain junction-leakage of 2.7x10-8 A/cm2 is measured at -3.3V that is compatible to the standard Si junction. This low junction leakage can be also explained by the similar process to form silicide. Another important advantage of this process is the capability to form high quality SiGe oxide. A very high breakdown electrical field is 15MV/cm is measured that is close to SiO2. The breakdown field is carefully measured and oxide thickness is directly determined by F-N tunneling. The good oxide quality is also demonstrated by the high reliability of charge-to-breakdown of 6 C/cm2. Although exact mechanism of achieving this high quality oxide is still under investigation, it may be related to the high RTP temperature and the strain relaxation in SiGe. In conclusion, high quality SiGe can be formed by a simple, inexpensive and VLSI compatible process.

2:30 PM
Surfactant Mediated Epitaxy of Ge/Si Heterostructures for Device Applications: *Karl R. Hofmann*[1]; Martin Kammler[1]; Dirk Reinking[1]; Michael Horn-von Hoegen[2]; [1]University of Hannover, Inst. f. Halbleitertechnologie, Appelstrasse 11 A, D-30167 Hannover Germany; [2]University of Hannover, Inst. F. Festkoerperphysik, Appelstrasse 2, D-30167 Hannover Germany

The deliberate use of an adsorbed monolayer of a group V element as surfactant, here Sb, during Ge/Si epitaxy inhibits island formation and allows the growth of smooth and continuous epitaxial Ge films on Si. On Si(111) the 4.2 % lattice mismatch between Si and Ge is accommodated by a quasiperiodic array of misfit dislocations which is completely confined to the Si-Ge interface. With this surfactant mediated epitaxy (SME), relaxed Ge-layers of arbitrary thickness larger than 10 nm can directly be grown on Si substrates. Thus high-quality Ge device structures, which are CMOS-compatible, can be placed on Si substrates without the use of thick relaxed graded SiGe buffer layers. We have investigated the structural and electrical properties of such Ge-layers grown into oxide windows on wafers pre-structured with a conventional LOCOS process and on bare Si substrates. The layers were analyzed by AFM, TEM, XRD, high-resolution LEED, SEM, and lateral Hall mobility and vertical Ge/Si diode transport measurements. The excellent crystal quality of these Ge films is revealed by X-ray diffraction which shows extremely sharp diffraction peaks with the Ge bulk lattice constant. Furthermore, very high electron Hall mobilities of 3200 cm^2/Vs at room-temperature are routinely obtained (12000 cm^2/Vs at 77K) for 1000 nm thick Ge films on Si(111). These mobility values correspond to high-quality bulk Ge mobility values with low Sb background n-type doping as reflected by Hall electron densities of about $1*10^{16}cm^{-3}$. This low background doping concentration of the surfactant Sb is three orders of magnitude below the Sb solid solubility in Ge. We have recently fabricated the first devices - Ge p-channel MOSFETs - on a Si substrate using SME. We will report results on the SME growth of strained SiGe MODFET structures on thin relaxed SiGe alloy layers on Si substrates demonstrating the potential of this growth technique for a variety of interesting device applications.

2:50 PM +
Direct Growth of Ge on Si for Integrated Si Microphotonic Photodetectors: *Hsin-Chiao Luan*[1]; A. M. Agarwal[1]; Kzumi Wada[1]; E. A. Fitzgerald[1]; L. C. Kimerling[1]; [1]Massachusetts Institute of Technology, Dept. of Mats. Sci. and Eng., 13-4130, 77 Mass Ave, Cambridge, MA 02139 USA

The successful development of integrated Si microphotonic circuits requires the integration of efficient photodetectors operating at 1.3um or 1.54um with Si CMOS devices and polySi waveguides. Ge with its high absorption coefficient at these two wavelengths is a candidate material for such an application. However, the 4% lattice mismatch between Ge and Si results in island formation when Ge is grown directly on Si. SiGe graded buffer technology can provide high quality Ge films on Si with threading dislocation densities as low as 2x10^6cm^-2. This technology, however, requires a 10um thick graded buffer for grading from Si to pure Ge. Si CMOS devices are relatively planar and occupy only the region close to the top surface of Si wafers. For simple process integration of Ge photodetectors with Si CMOS devices it is desirable to grow a thin high quality Ge film directly on Si. In this work we report the development of a process for the growth of Ge films with low threading dislocation densities on Si. We have investigated the quality of Ge, grown on Si, by a two-step UHV-CVD process followed by cyclic thermal annealing. Thin Ge films were first grown on Si at 300ºC. Growth at low temperatures reduced the diffusion of Ge atoms and prevented island formation. After 60nm of Ge was grown, the furnace temperature was raised to 600ºC and 1um of Ge was deposited. The threading dislocation density in the as-grown Ge (measured with plan-view TEM) was 9.5±0.2x10^8cm^-2. Cyclic thermal annealing reduced the threading dislocation density to 2.2± 0.3x10^7cm^-2. The effect of thermal annealing temperature, annealing time, and the number of thermal cycles on threading dislocation density was studied. We propose a simple model for dislocation motion and reactions due to differential thermal stress to account for the reduction of threading dislocations. To determine the applicability of Ge films grown on Si using two-step technique, we have studied the effect of threading dislocations on the GHz operation of Ge photodetectors. Using a model that correlates the junction leakage current and threading dislocation density we reported earlier, we compared the leakage current noise and photoelectron noise. The optical power required to obtain a bit-error-rate of 10^-9 was calculated as a function of detector speed and total leakage current. We find that the noise due to carrier-generation at threading dislocations (10^7cm^-2) is not fatal to GHz operation of Ge photodetectors. Based on our model, direct growth of Ge on Si is a viable process for the integration of high speed Ge photodetectors in Si CMOS technology.

3:10 PM Break

3:30 PM +
Boron Segregation in Polycrystalline Si(1-x-y)Ge(x)C(y) Alloys: *Eric Jonathan Stewart*[1]; Malcolm S. Carroll[1]; Chia-Lin Chang[1]; James C. Sturm[1]; [1]Princeton University, Dept. of Elect. Eng., Center for Photonics and Optoelectronic Mats., J303 Eng. Quad, Olden St., Princeton, NJ 08544 USA

Polycrystalline $Si_{1-x-y}Ge_xC_y$ gates have been previously shown to greatly reduce the penetration of boron through thin gate oxides in PMOS structures[1]. PMOS capacitors made with a layer of poly $Si_{1-x-y}Ge_xC_y$ in the heavily boron doped (~$10^{21}/cm^3$) gate electrode had greater

resistance to boron penetration through the gate oxide than those with all polycrystalline Si or polycrystalline $Si_{1-x}Ge_x$ gate electrodes. Boron readily diffused out of the poly Si and poly $Si_{1-x}Ge_x$ gates and through the gate oxide during high temperature anneals (900℃). In the structures with poly $Si_{1-x-y}Ge_xC_y$ gates, however, boron accumulated in the $Si_{1-x-y}Ge_xC_y$ layer, significantly reducing diffusion through the gate oxide. This effect appears to be due to boron preferentially remaining in poly $Si_{1-x-y}Ge_xC_y$ layers, possibly because it has a lower chemical potential in $Si_{1-x-y}Ge_xC_y$ than in Si or $Si_{1-x}Ge_x$, not due to the lower diffusion coefficient of boron in crystalline SiGeC as has recently been reported[2]. In this abstract we report, to the best of our knowledge, the first independent evidence of boron segregation into both polycrystalline and crystalline $Si_{1-x-y}Ge_xC_y$ from Si. Layers of poly $Si_{1-x}Ge_x$ and poly $Si_{1-x-y}Ge_xC_y$ were grown on a wet chemically oxidized p-type substrate by Rapid Thermal Chemical Vapor Deposition(RTCVD). Each SiGe(C) layer was isolated by polycrystalline silicon spacer layers on both sides. The poly $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers were grown at 625℃ and x~0.2; the poly Si spacer layers were grown at 700℃. All layers were doped in-situ with boron at ~$1x10^{20}/cm^3$. Silane, germane, diborane, and methylsilane were used as source gases in a hydrogen carrier gas at 6 torr. Oxygen levels in all layers were much less than boron or carbon levels. These structures were then annealed at 800℃ for 18 hours in nitrogen. Concentration vs. depth profiles of all relevant materials in the structure were obtained by Secondary Ion Mass Spectroscopy (SIMS). Boron clearly segregated from the silicon into the $Si_{1-x-y}Ge_xC_y$ layers during the anneal. In the poly $Si_{1-x}Ge_x$ layers, boron outdiffused into the adjacent poly Si layers, causing concentration profiles to flatten out. In the poly $Si_{1-x-y}Ge_xC_y$ layers with significant carbon content(>0.1%), boron concentrations actually increased after annealing, with boron levels decreasing in the adjacent poly Si layers. In the $Si_{1-x-y}Ge_xC_y$ layer with ~1% carbon, the boron levels after annealing were approximately four times higher than in the adjacent silicon layers. Any tendency of boron to segregate to polycrystalline $Si_{1-x}Ge_x$ layers without carbon was an order of magnitude weaker, consistent with observations in crystalline $Si_{1-x}Ge_x$/Si samples[3]. We have also observed large segregation of boron to $Si_{1-x-y}Ge_xC_y$ in crystalline $Si_{1-x-y}Ge_xC_y$/Si samples. Initial electrical data suggests that the boron is still electrically active after segregation to $Si_{1-x-y}Ge_xC_y$, and does not segregate to electrically inactive defect sites. This is fortuitous for device applications such as polycrystalline gates. Existing models for boron segregation in the $Si_{1-x}Ge_x$/Si system are based on lattice strain and valence band offset arguments[4]. From both of these arguments, less boron diffusion to $Si_{1-x-y}Ge_xC_y$ than $Si_{1-x}Ge_x$ would be expected. A new model to explain our data will be presented. References 1. C. L. Chang and J.C. Sturm, "Polycrystalline $Si_{1-x-y}Ge_xC_y$ for suppression of boron penetration in PMOS structures," Materials Research Society Symposium Proceeding, 525, (1998). 2. M. S. Carroll, L. D. Lanzerotti, and J.C. Sturm, "Quantitative Measurement of Reduction of Boron Diffusion by Substitutional Carbon Incorporation," Materials Research Society Symposium Proceeding, 527, (1998). 3. S. M. Hu, D. C. Ahlgren, P. A. Ronsheim, and J. O. Chu, "Experimental Study of Diffusion and Segregation in a Si-(GexSi1-x) Heterostructure," Physical Review Letters, 67:(11) 1450-1453, (1991). 4. S. M. Hu, "Diffusion and Segregation in Inhomogenous Media and the GexSi1-x Heterostructure," Physical Review Letters, 63:(22) 2492-2495, (1989).

3:50 PM

X-Ray Diffraction and Transmission Electron Microscopy Study of the Development of Texture in Polycrystalline $Si_{1-x}Ge_x$ Thin Films: *Wei Qin*[1]; D. G. Ast[2]; T. I. Kamins[3]; [1]Institute of Microelectronics, 11 Sci. Park Rd., Singapore Sci. Park II, Singapore 117685 ROS; [2]Cornell University, Mats. Sci. & Eng. Dept., Ithaca, NY 14853 USA; [3]Hewlett-Packard Laboratories, Palo Alto, CA 94303-0867 USA

Intrinsic, 300 nm thick $Si_{1-x}Ge_x$ films with x=0.02, 0.13, and 0.31 respectively, and a control polysilicon film, x=0 were deposited by CVD at a pressure of 100 Torr, on a 60 nm polysilicon seed layer at temperatures between 600 and 800℃, depending on Ge fraction. SiH_2Cl_2 was used for polysilicon deposition and SiH_2Cl_2 mixed with GeH_4 for SiGe. Polysilicon seed layer was grown by CVD on SiO_2 using SiH_4 at 650℃. X-ray diffraction and transmission electron diffraction (TED) study on planar samples showed that polysilicon control film and SiGe films had {110} texture. X-ray diffraction of a 'seed layer only' sample indicated that grains in seed layer were randomly oriented. The development of texture was studied by taking TED patterns of cross-section samples, employing conditions such that electron beam illuminated top layer only, or using a larger beam size, both seed layer and top layer. Comparison of relative diffraction intensity of arcs contributed by the {110} texture to total diffracted intensity was used to obtain information on the texture in seed layer. Consistent with x-ray diffraction result, {110} texture appears weak or absent in the seed layer, indicating that texture in the seed layer remained unchanged. To determine the width of distribution of otientation around fiber axis, a, we measured the spread of {110} arc on TED patterns for samples containing diffrerent Ge fractions. This analysis showed very similar value for a in all Ge containing films, about 25°. The a in polysilicon control film is about 31°. Analysis of the x-ray diffraction intensity showed that about 46 to 54% of grains in films were {110} oriented, the fraction oriented increased with increasing Ge fraction, indicating that the addition of Ge facilitates the development of {110} texture. Other orientations present, listed in decreasing sequence according to their texture intensity, were {311}, {111}, {100}, and {331}. TED of wedge-shaped planar specimens showed that {110} was dominant texture during entire growth process in all films, and that the degree of this texture increased during growth. The grain size in the top layer was found to range from 45 nm to 81 nm by TEM, depending on Ge fraction. Microtwins with common {110}orientation were found in all films. Cross-section TEM images showed that all films possessed a columnar structure, and that numerous V-shape grains formed near that op of the film. The above results indicate that the orientation of the polycrystalline seed layer does not play a critical role in determining the texture that develops in subsequently deposited SiGe films, when the seed layer has no preferred texture, and that the {110} texture, once initiated, rapidly increases during subsequent film growth.

4:10 PM

Diamond Epitaxy for Electronic Devices: *Aleksandar Aleksov*[1]; Mike Kunze[1]; Andrei Vescan[1]; Wolfgang Ebert[1]; Erhard Kohn[1]; Andreas Bergmaier[2]; Guenther Dollinger[2]; [1]University of Ulm, Dept. of Electron Devices and Circuits, Albert-Einstein-Allee 45, Ulm D-89081 Germany; [2]Technische Universitaet Muenchen, Dept. E12, Beschleunigerlabor der LMU/TUM, Muenchen Germany

Diamond is commonly considered a quite unusual and difficult semiconductor material. Nevertheless many electronic devices have been realized so that the extraordinary potential of this ultra wide bandgap semiconductor can be well assessed. In this presentation we would like to discuss the epitaxial procedures for the most advanced structures, namely d-doped channel, lossy dielectric FETs and pnp BJTs. The epitaxial growth of high crystal quality diamond was performed by MWPCVD using an approximate 1.5%-CH4 in H2 mixture at 30Torr and 600°C-800°C. The growth rates range from 5nm/min to 14nm/min. The only technically relevant dopants in diamond are boron and nitrogen (phosphorus is being considered as a shallow donor, but has not yet been implemented in complex device structures). A method of doping diamond during epitaxial growth by using a boron rod as a solid doping source was developed. With this doping method it is possible to fabricate steep doping profiles (delta spikes), homogeneous and degenerately doped (NA>1020cm-3) diamond films, needed for the fabrication of diamond FETs and BJTs. The activation energy of boron is EA=0.38eV. At NA»1020cm-3 the EA disappears due to miniband formation and overlap with the valence band. The maximum controllable sheet charge density in FET channels pSmax is presently limited to 2×1013cm-2. This leads to d-doped channels with channel widths <3nm for full activation. Epitaxially grown d-doped films were analyzed by elastic recoil detection giving a FWHM of 4nm with peak NA>2.5×1020cm-3. Nitrogen is a very deep donor with ED=1.7eV. Nevertheless it is possible to fabricate abrupt boron/nitrogen pn-junctions that operate even at R.T. This pn-junctions were then applied in BJTs and as control diodes in FETs. Abrupt junctions were fabricated by using growth interrupts, which are not detrimental in the case of diamond. Deep donor and acceptor levels are common in many wide band gap semiconductor materials, with the extreme case of diamond. Problems concerning diamond are similar but an order of magnitude higher than in other wide gap materials like SiC and III-Nitrides. Nevertheless device operation, both FET and BJT has been demonstrated. Diamond d-channel FETs with a lossy dielectric boron/nitrogen control junction