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Electrical characteristics of double-base $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors

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Recent advances in low-temperature epitaxial growth of strained, single-crystalline silicon–germanium random alloys ($Si_{1-x}Ge_x$) have introduced band gap engineering into the design of silicon-based devices. Here we describe a novel device, the double-base heterojunction bipolar transistor, which increases the functionality of a "normal" $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor by having two base contacts which can independently control the collector current. It can be used in a single-transistor NAND gate at temperatures up to 140 K, as an amplifier with digital ON/OFF control, or to increase the Early voltage (output resistance). In this article, the fabrication procedure of the device is outlined in detail, followed by complete electrical evaluation and modeling.

I. INTRODUCTION

$Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors (HBTs) have shown the ability to vastly improve the characteristics of silicon homojunction bipolar transistors, but they perform the same circuit function. Recently, a novel double-base $Si/Si_{1-x}Ge_x/Si$ HBT has been demonstrated which increases the functionality of a simple transistor, and thus could lead to novel circuit applications besides improvement in device speed. For example, using this device a single-transistor two-input NAND gate circuit has been demonstrated.[1,2]

In this article, the principle of operation of the device will be quickly reviewed, followed by detailed discussion of the fabrication procedure, electrical performance and applications, and electrical evaluation of the band diagram parameters.

II. PRINCIPLE OF OPERATION OF DOUBLE-BASE HBT (DBHBT)

The key idea of a HBT is to lower the potential barrier seen by the carriers responsible for the output current (electrons in *npn* devices) compared with the one seen by the carriers constituting the input current (holes in *npn* devices), thereby increasing the ratio of output to input current, the common-emitter current gain $\beta = I_C/I_B$ of the HBT, compared with a homojunction transistor. In a $Si/Si_{1-x}Ge_x/Si$ HBT, this is achieved by replacing the *p*-Si base of a homojunction transistor by a narrow-band gap strained $p\text{-}Si_{1-x}Ge_x$ layer to give a $n\text{-}Si/p\text{-}Si_{1-x}Ge_x/n\text{-}Si$ sequence.[3–5] These devices have recently been fabricated with near-ideal electrical characteristics.[6–8]

In the DBHBT, which is based on an $n\text{-}Si/p\text{-}Si_{1-x}Ge_x/i\text{-}Si/p\text{-}Si_{1-x}Ge_x/n\text{-}Si$ layer sequence, an *i*-silicon layer is inserted in the middle of the $p\text{-}Si_{1-x}Ge_x$ base (see Fig. 1). The resulting two $p\text{-}Si_{1-x}Ge_x$ layers are independently contacted to form two base inputs. Since the band lineup at the $Si/Si_{1-x}Ge_x$ heterojunction is such that $\Delta E_C \ll \Delta E_V$, and the Si layer is fully depleted, the conduction band in the base is approximately constant, if both $Si_{1-x}Ge_x$ layers are at the same potential, like that in a flat base $Si/Si_{1-x}Ge_x/Si$ HBT. The intrinsic silicon layer in the base, however, causes a barrier for holes of height $E_V(\text{Si}) - E_V(\text{SiGe})$ in the valence band between the two $p\text{-}Si_{1-x}Ge_x$ layers at the emitter and the collector side of the base. This valence band potential barrier can isolate the two $Si_{1-x}Ge_x$ layers in the base from each other, since it blocks holes for a sufficiently large barrier. If separate contacts are made to these two $Si_{1-x}Ge_x$ layers, they will be electrically independent of each other. The resulting device, which we call double-base heterojunction bipolar transistor (DBHBT), has four terminals; emitter, base 1, base 2, and collector.

The modes of operation of this DBHBT are illustrated in Fig. 2. The basic principle is that the shape of the barrier seen by electrons in the conduction band is determined by the voltages applied to both of the base contacts, as opposed to a single base in a normal bipolar transistor. We assume that the base 2–collector junction is always reverse biased resulting in negligible electron injection into the base from the collector side. If both bases are shorted to the emitter, no electrons are injected into the base from the emitter, resulting in no collector current [Fig. 2(a)]. If only one of the bases is forward biased with respect to the emitter, the base which is not forward biased still presents a barrier for electrons in the conduction band, and no collector current flows [Figs. 2(b) and 2(c)]. Only if *both* bases are forward biased with respect to the emitter vanishes the barrier for electron flow in the conduction band, resulting in collector current [Fig. 2(d)]. In series with a load resistor, this device can therefore be used in a single-transistor NAND gate which increases the functionality of the DBHBT compared to a $Si/Si_{1-x}Ge_x/Si$ HBT.[2]

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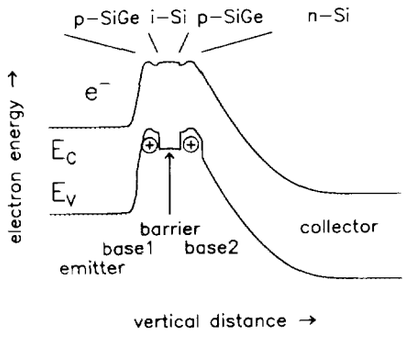


FIG. 1. Calculated band diagram of DBHBT, obtained by inserting an intrinsic silicon layer into the p-$Si_{1-x}Ge_x$ base of a flat-base HBT. Note that the conduction band in the base is still approximately flat because $\Delta E_C \ll \Delta E_V$ at the $Si/Si_{1-x}Ge_x$ heterojunction.

III. GROWTH OF EPITAXIAL LAYERS AND DEVICE PROCESSING

The layer sequence was grown by rapid thermal chemical vapor deposition (RTCVD).[9] First, the collector layers were grown at 1000 °C without intentional doping on an n^+ buffer layer. Then the temperature was lowered to grow the base layers, first, the second p-doped $Si_{1-x}Ge_x$ base with intrinsic $Si_{1-x}Ge_x$ spacers on both sides (625 °C), then the nominally 200 Å thick intrinsic Si barrier (700 °C), and finally, the first p-$Si_{1-x}Ge_x$ base, again with i-$Si_{1-x}Ge_x$ spacers (625 °C). The approximate base doping was 5×10^{18} cm^{-3}. The i-$Si_{1-x}Ge_x$ spacers were inserted to prevent the base dopant from diffusing into the i-Si barrier. In the four wafers grown, the germanium concentration in the two bases and the i-$Si_{1-x}Ge_x$ spacer

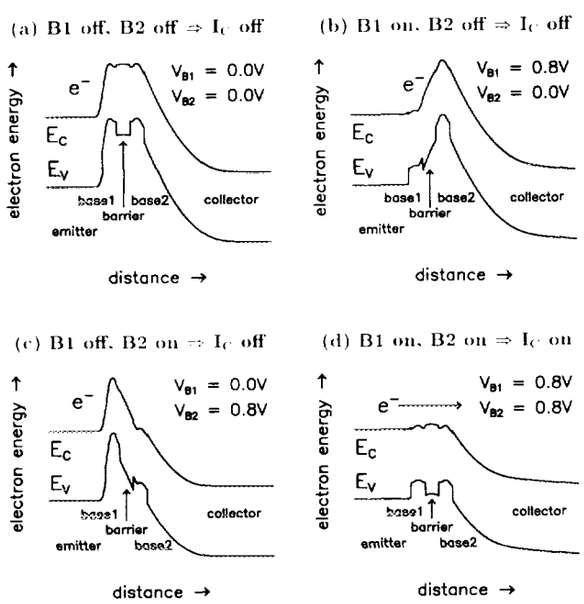


FIG. 2. Band diagrams showing modes of operation of DBHBT. Only if *both* base inputs are forward biased with respect to the emitter are electrons injected into the p-base region.

TABLE I. Device structures for DBHBTs grown by RTCVD.

Device	1075	1076	1077	1078
Nominal Ge concentration (%)	20	30	30	38
Nominal p-$Si_{1-x}Ge_x$ thickness (Å)	160	30	60	40
Nominal i-$Si_{1-x}Ge_x$ thickness (Å)	50	60	45	30
Barrier thickness W_{Si} from C-V (Å)	299	427	288	310
E_A from T-dependent I_C (meV)	158	215	215	239
E_V(Si)–Φ_p(SiG) from T-dependent $I_{B1,B2}$ (meV)	178	215	275	255

thicknesses were varied as shown in Table I. The emitter was grown at 700 °C using silane because of the higher growth rate compared to $SiCl_2H_2$ to minimize the thermal budget experienced by the base layers, and it was doped *in situ* with phosphorus, instead of using ion implantation, so that no implant anneal was required. The low thermal budget was crucial to prevent boron diffusion into the i-silicon barrier which would have resulted in insufficient isolation between the two bases due to band bending in the base. Table I shows that the $Si_{1-x}Ge_x$ layers were thicker than the equilibrium critical thickness. On wafers No. 1076 and No. 1078 misfit dislocations could be observed by phase contrast (Nomarski) microscopy, because they caused increased chemical etching during device processing.

From these layers, devices were then fabricated in a triple-mesa process with low thermal budget similar to the one employed by Narozny *et al.*[10] (see Fig. 3). First, low-temperature silicon dioxide (p-SiO_2) was deposited by plasma deposition and patterned with the emitter mesa mask. Then the silicon emitter was etched in a room-temperature solution of 150 g KOH, 6 g $K_2Cr_2O_7$, 150 ml n-propanol, and 600 ml de-ionized water. This solution etches silicon at ~75 Å/min, while the etch rate for strained $Si_{1-x}Ge_x$ is much smaller. The p-SiO_2 mask was then removed in 1:6 HF:NH_4F (buffered oxide etch), followed by base 1-mesa photolithography. The $Si_{1-x}Ge_x$ base layer was next etched in a solution of 200 ml HNO_3, 100 ml H_2O, and 25 ml 1:100 HF:H_2O which etches the $Si_{1-x}Ge_x$ alloy with a high selectivity compared to silicon at an etch rate of ~200 Å/min.[11] Next, new oxide was deposited and patterned with the base 1-mesa mask, and the base 2 $Si_{1-x}Ge_x$ etched as described for base 1. Finally, the base 2 mesa was plasma etched down to the n^+-buffer layer. The oxide was then removed, and new oxide deposited over the whole structure, followed by contact hole etch and metallization (5000 Å Ti: 5000 Å Al; 400 °C anneal in forming gas for 20 min). Even a thin ($\approx$100 Å) layer of Ti acts as a diffusion barrier for Al to prevent spiking. The relatively high Ti layer thickness was chosen to obtain step coverage of the metallization at the base 2 mesa.

The device on wafer No. 1077, whose electrical characteristics are presented in Sec. IV had an emitter area of $\sim70\times70$ μm^2 and a base-1 area of $\sim215\times215$ μm^2. The smallest working devices had an emitter area of 30×30 μm^2.

IV. ELECTRICAL MEASUREMENTS ON DBHBTs

The devices were then evaluated with temperature-dependent current–voltage and capacitance–voltage measurements. Working devices were obtained on all four wafers. We now present measurements taken on wafer No. 1077. Corresponding measurements on the other wafers yielded similar results.

With both bases externally shorted together, the devices worked like $Si/Si_{1-x}Ge_x/Si$ HBTs for temperatures from 85 to 373 K, with a common-emitter current gain of ~ 100 [see Figs. 4(a) and 4(b)]. The base currents were nonideal with ideality factors of $n \approx 1.3$ at room temperature, because the base–emitter junctions were mesa isolated, resulting in recombination current from the periphery of the devices due to surface states. This has also been observed by other groups using a similar process for fabricating conventional $Si/Si_{1-x}Ge_x/Si$ HBTs.[12] The collector currents were ideal in the temperature range measured with slopes of 60 mV/decade at 293 K, as shown in Fig. 4(a).

The key point for the operation of the DBHBT is the $p\text{-}Si_{1-x}Ge_x/i\text{-}Si/p\text{-}Si_{1-x}Ge_x$ barrier in the valence band. Figure 5 shows its room and low temperature current–voltage characteristics. If a bias is applied between the two $p\text{-}Si_{1-x}Ge_x$ layers, holes are injected by thermionic emission over the valence band discontinuity at the $Si/Si_{1-x}Ge_x$ heterojunction, estimated to be 222 meV for 30% Ge.[13] The magnitude of this current precluded independent base operation of the DBHBT at room temperature. At 77 K, however, thermionic emission was sufficiently suppressed to provide isolation between the two base layers, and the two bases were independent with leakage currents below 5 μA for relative base voltages of less than 0.5 V in a device with a base mesa area of $184 \times 184\ \mu m^2$. From 77 to ~ 140 K, the leakage currents were only weakly dependent on temperature, as will be discussed later.

Since the voltages applied at *both* bases shaped the conduction band the collector current consisting of electrons injected from the emitter could be controlled independently with either base contact at 77 K as shown in the three-dimensional (3D) Gummel plot of Fig. 6, where the collector current I_C is plotted versus base input voltages V_{B1} and V_{B2}, with grounded emitter and a constant collector voltage of $V_C = 1$ V. Only if *both* bases were forward biased with respect to the emitter was the collector current turned on. It increased with an inverse slope of less than 17 mV/decade, close to the ideal value of 15.3 mV/decade at 77 K. This confirmed the basic operating principle of the device. Since both inputs must be forward biased with respect to the emitter for I_C to flow, the device can be used to perform a single-transistor NAND function.[2]

The electrical versatility of the device is further shown in Fig. 7. Since both bases must be forward biased for

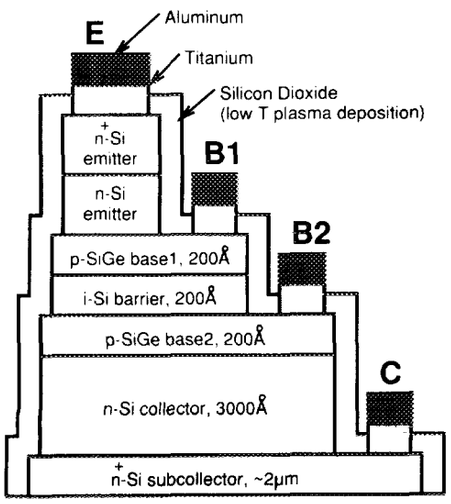


FIG. 3. Triple mesa device structure of DBHBT.

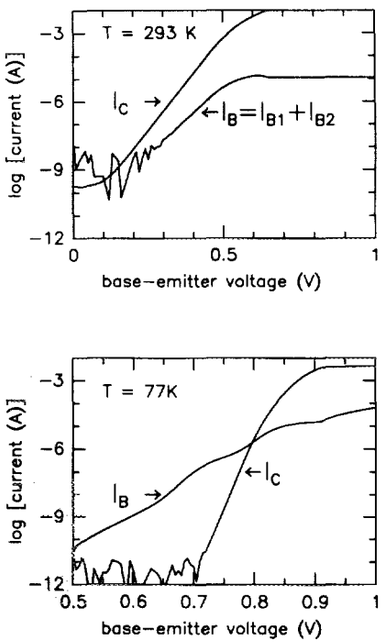


FIG. 4. Gummel plot of DBHBT No. 1077 at (a) room temperature and (b) 77 K with both bases externally shorted together and a base-collector reverse bias of 1 V.

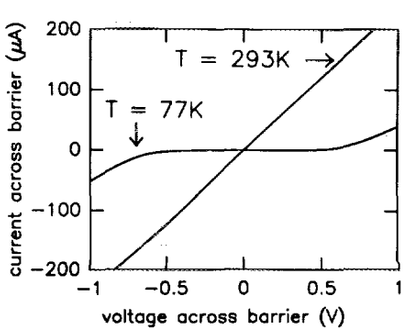


FIG. 5. Current–voltage characteristics of the $p\text{-}Si_{1-x}Ge_x/i\text{-}Si/p\text{-}Si_{1-x}Ge_x$ barrier of device No. 1077 at room temperature and at 77 K.

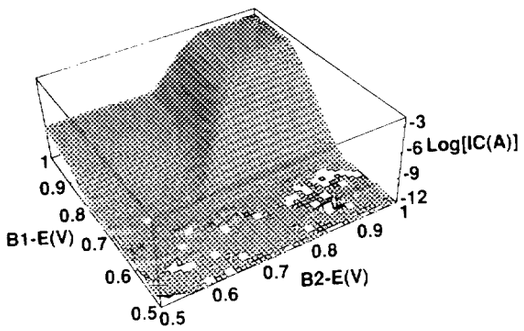
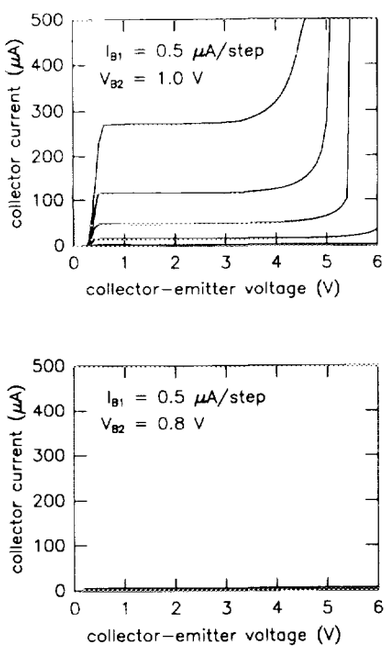


FIG. 6. Measured collector current of DBHBT No. 1077 at 77 K as a function of V_{B2} and V_{B1}.

collector current to flow, the base next to the emitter can be used in normal common-emitter operation, while the second base can be used as digital input to turn the device on and off. This is illustrated in Fig. 7 showing common-emitter characteristics where base 1 was used as a normal base input for current amplification, and the voltage on base 2 was used as a digital input to control the current gain of the device. At 77 K, the current gain seen by base 1 was ~ 100 for $V_{B2}=1$ V [Fig. 7(a)], but zero for $V_{B2}=0.8$ V [Fig. 7(b)].

A further benefit of this mode of operation is the very high output resistance (absence of collector voltage modulation of collector current). If the bases were tied together, an Early voltage of ~ 50 V resulted. If the second base input was held at 1 V forward bias with respect to the



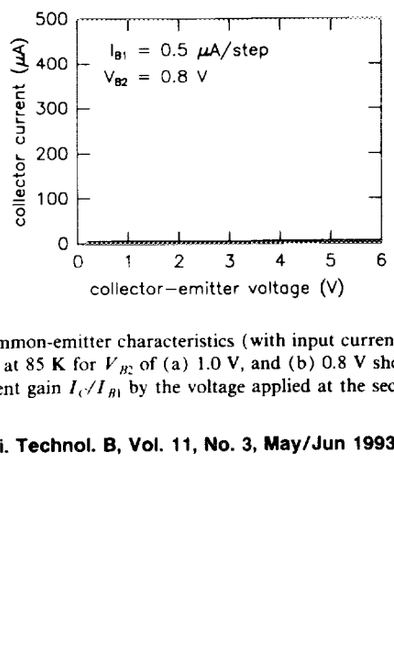


FIG. 7. Common-emitter characteristics (with input current into base 1) of DBHBT at 85 K for V_{B2} of (a) 1.0 V, and (b) 0.8 V showing control of the current gain I_C/I_{B1} by the voltage applied at the second base.

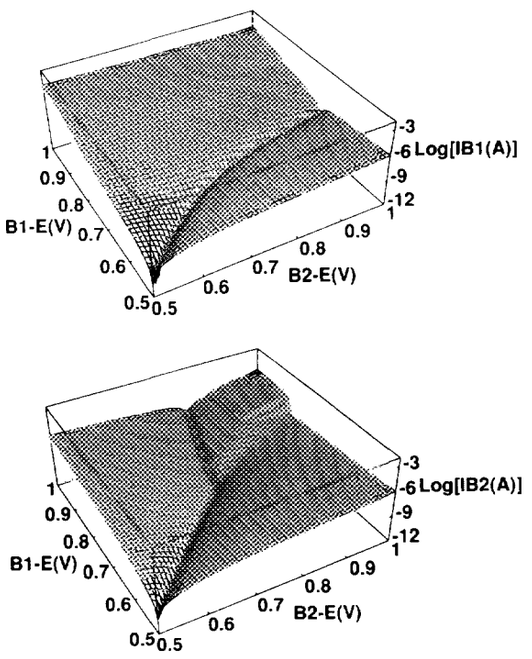


FIG. 8. Measured magnitude of the current into (a) base 1 and (b) base 2 vs input voltages of device No. 1077 at 77 K.

emitter, however, as shown in Fig. 7(a), the second base shielded the critical conduction band barrier controlled by I_{B1} from the collector voltage, and hence a higher Early voltage of ~ 500 V was obtained.

The base currents at low temperature were also independently measured versus V_{B1} and V_{B2} with grounded emitter and $V_C=1$ V [Figs. 8(a) and 8(b)]. Figure 9 shows a schematic diagram of possible base current sources which is useful for understanding these data. There can be three components of I_{B1}; due to holes injected into the emitter (or the base–emitter space charge region), whose number will depend only on $[V_{B1}-V_E]$ [path (a) in Fig. 9], and due to holes moving over the barrier to or from base 2, whose number will depend on $[V_{B1}-V_{B2}]$ [path (b) in Fig. 9]. The current into base 1 was not symmetric with respect to the difference of the base inputs. It depended strongly on the voltage applied at base 1 suggesting

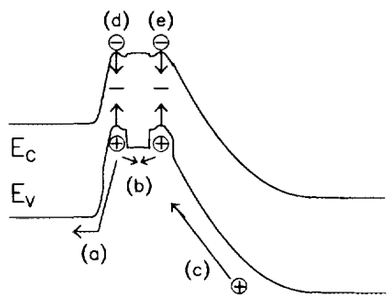


FIG. 9. Schematic band diagram showing the source of the two base currents I_{B1} and I_{B2}.

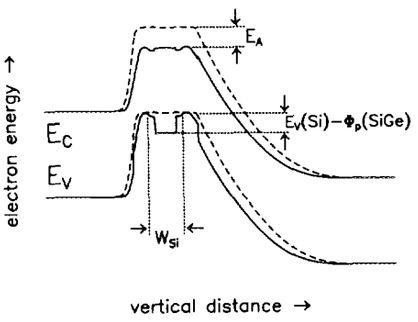


FIG. 10. Band diagram of DBHBT (solid lines) and Si homojunction transistor (dashed lines) showing the parameters determined from electrical measurements: barrier thickness W_{Si}; effective band gap reduction E_A; and barrier height for holes, $E_V(Si)-\Phi_p(SiGe)$.

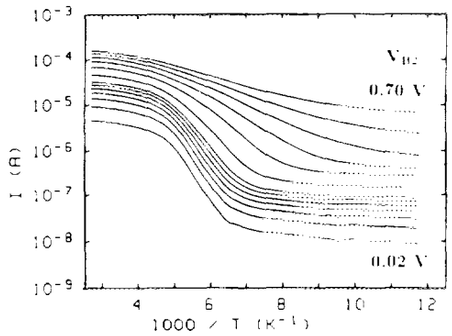


FIG. 11. Current across *i*-silicon barrier plotted logarithmically vs inverse temperature for various values of $V_{B2}-V_{B1}$ (0.02, 0.04, ..., 0.14, 0.2, 0.3, ..., 0.7 V).

that it was due to holes injected from base 1 into the base–emitter depletion region, or into the neutral emitter for large V_{B1}. Neutral base recombination [path (d) in Fig. 9] could also contribute to this current. For low base 1-emitter voltages, the current reversed its direction, and it was dominated by holes leaking through the valence band barrier into the base-2 layer [path (b) in Fig. 9].

The current into base 2 consists of holes traveling over the barrier to or from base 1 [path (b) in Fig. 9], of holes recombining with injected electrons in the neutral base 2 [path (e) in Fig. 9], and of holes generated by avalanche multiplication or thermal generation in the reverse-biased base–collector junction [path (c) in Fig. 9]. The current into base 2 was symmetric with respect to the difference of the base input voltages, i.e., the voltage across the valence band barrier between base 1 and base 2, for values of V_{B1} and V_{B2} below the turn-on voltage of ~ 0.8 V. This shows that I_{B2} was dominated by holes leaking through this barrier. Above turn on, however, there was a nonideal component of base 2 current, probably due to neutral base recombination in base 2 [path (e) in Fig. 9], caused by defects in the $Si_{1-x}Ge_x$ layers which exceeded the equilibrium critical thickness.

V. ELECTRICAL EVALUATION OF BAND DIAGRAM PARAMETERS

Some parameters of the band diagram of Fig. 1 could be determined from electrical measurements. They are listed in Table I, and schematically shown in Fig. 10. The thickness of the isolating barrier W_{Si} was measured with a capacitance–voltage measurement at 85 K, a frequency of 10 kHz, and no applied dc bias, where the leakage current through the barrier was suppressed. Base 1 was shorted to the emitter and base 2 to the collector. If the applied ac signal caused a positive voltage at base 2, the *i*-$Si_{1-x}Ge_x$ spacer between base 1 and the Si barrier was in depletion, and the *i*-$Si_{1-x}Ge_x$ spacer between base 2 and the Si barrier was in accumulation. The two bases therefore acted as the plates of a capacitor with the Si barrier and the depleted *i*-$Si_{1-x}Ge_x$ spacer being the dielectric, and from the measured value of the capacitance between the two bases, the thickness of the isolating barrier was determined. The measured values of ~ 300 Å were consistent with the growth rates assumed for the Si and $Si_{1-x}Ge_x$ layers. In wafer No. 1076, thicker *i*-$Si_{1-x}Ge_x$ spacer layers were inserted on both sides of the *p*-$Si_{1-x}Ge_x$ bases. This was reflected in a thicker barrier (427 Å).

The effective band gap reduction in the base (E_A) between the DBHBT doped about 5×10^{18} cm^{-3} and a Si homojunction device doped 10^{19} cm^{-3} was determined from a temperature-dependent collector current measurement, with both bases externally shorted together. Assuming the absence of parasitic barriers from excessive base dopant outdiffusion either into *n*-silicon emitter and collector or the *i*-silicon barrier, the band gap difference between the *p*-$Si_{1-x}Ge_x$ layers and the silicon control device (approximately equal to the valence band discontinuity ΔE_V) could be determined. The activation energies E_A of the Arrhenius plots, listed in Table I, were close to the expected values of ΔE_V and ΔE_G for the Ge concentrations used, except for device No. 1078, where the smaller than expected E_A may have been due to excessive strain relaxation. This is evidence that dopant diffusion or segregation into the Si barrier did not occur in our devices.

The current–voltage characteristics of the *p*-$Si_{1-x}Ge_x$/*i*-Si/*p*-$Si_{1-x}Ge_x$ barrier were also measured as a function of temperature for various values of the voltage V_{B2} across the barrier. Figure 11 shows an Arrhenius plot (current plotted logarithmically versus inverse temperature) for positive values of $V_{B2}-V_{B1}$. A measurement taken at negative values of $V_{B2}-V_{B1}$ yielded similar results. For this measurement, base 1 was externally shorted to the emitter, and base 2 was externally shorted to the collector. For temperatures below ~ 140 K, the leakage current through the barrier was a weak function of temperature, indicating that in this temperature range thermionic emission was suppressed. In the temperature range between ~ 140 and 200 K, thermionic emission of holes over the valence band barrier caused a strong increase in current corresponding to the Richardson law of thermionic emission,[14]

$$I_{B1,B2}=A_{B1}\frac{4\pi qm^*k_B^2}{h^3}T^2\,e^{\{-|E_V(\mathrm{Si})-\Phi_p(\mathrm{SiGe})|/k_BT\}},$$

where A_{B1} is the area of the base-1 mesa, and A^* the effective Richardson constant. From these measurements the activation energy could be extracted which corresponds to the energy difference between the valence band in the Si barrier and the hole quasi-Fermi level Φ_p in the $Si_{1-x}Ge_x$ degenerately doped bases. The measured activation energy decreased with applied bias across the barrier, indicating that holes tunneled through the triangular part of the barrier (Fowler–Nordheim tunneling). The maximum values of $E_V(\mathrm{Si})-\Phi_p(\mathrm{SiGe})$ which were obtained at small biases of $\leqslant 0.02$ V across the barrier and averaged over positive and negative values of $V_{B2}-V_{B1}$ are shown in Table I. They are less accurate than the values of the effective band gap reduction described above, because the exponential increase in $I_{B1,B2}$ was limited for temperatures above ~ 200 K by the parasitic resistance between the base-2 contact and the region of the base-2 layer vertically below base 1, and we estimate the error bars to be ~ 30 meV. Within this accuracy, the experimentally obtained hole barrier heights agreed with the expected values. Note that although devices No. 1076 and No. 1077 had the same Ge concentration, the device with bigger *i*-$Si_{1-x}Ge_x$ spacers had a smaller $E_V-\Phi_p$ because of the barrier height for the holes in the *p*-$Si_{1-x}Ge_x$ layer. This indicates that the thermal budget of the process was sufficiently low to prevent dopant diffusion into the *i*-$Si_{1-x}Ge_x$ spacer.

VI. CONCLUSIONS

A novel four-terminal DBHBT with two base inputs has been developed which increases the functionality of HBTs. The extra terminal can be used to turn the device on or off, to avoid collector voltage modulation of the output current, or to create a single transistor NAND gate. With $\approx 30\%$ Ge in the *p*-bases, the device can be operated with near-ideal base isolation up to 140 K. Attempts to raise the maximum operating temperature with a higher base Ge concentration resulting in bigger band offsets were limited by strain relaxation of the $Si_{1-x}Ge_x$ layers.

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