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INTEGRATED AMORPHOUS AND POLYCRYSTALLINE SILICON TFTs WITH A SINGLE SILICON LAYER

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ABSTRACT

Selective exposure of an a-Si:H film to a room temperature hydrogen plasma using a patterned SiN_x capping layer and a subsequent anneal at 600°C, resulted in polycrystalline and amorphous silicon regions in a single silicon layer on the same glass substrate. Top-gate non-self-aligned TFTs were fabricated in both the amorphous and polycrystalline regions with all shared processing steps and no laser processing using a re-hydrogenation step. The TFTs had good characteristics, with field-effect mobilities upto 1.2 cm²/Vs and 15 cm²/Vs for the a-Si:H and the poly-Si TFTs, respectively, and ON/OFF ratios >10⁵ in either case.

INTRODUCTION

For large-area electronics, there has been considerable interest to integrate both polycrystalline and a-Si:H TFTs. This can be done by selective laser crystallization of a-Si:H [1], or using two layers of silicon, one polycrystalline and second amorphous [2], to integrate the a-Si:H and the poly-Si TFTs on the same substrate. In active-matrix flat panel displays, a-Si:H TFTs provide low leakage in the OFF state and poly-Si TFTs high drive currents. Integration of a-Si:H and poly-Si TFTs is traditionally difficult for three reasons. First, the conventional a-Si:H TFT fabrication process is a low temperature process (<300°C) [3], while the poly-Si TFT fabrication requires a 600°C anneal starting from a-Si:H if laser processing is not used. Second, one would like to deposit only a single Si layer instead of two (a-Si:H and poly-Si) to save cost, and third, the structure and fabrication sequence of a-Si:H TFTs and poly-Si TFTs are traditionally very different (e.g. bottom gate vs. top gate process), so that few process steps can be shared.

In this paper we demonstrate a method for integrating such transistors together starting with a single Si layer without laser processing. The work is based on the selective crystallization of amorphous silicon to polysilicon by locally seeding the crystallization with a masked RF hydrogen plasma at room temperature, followed by subsequent crystallization anneal at 600 °C [4]. All of the fabrication steps between the two transistors are combined to simplify the process. Using a critical re-hydrogenation step after the 600 °C annealing, top-gate a-Si:H TFTs with a field-effect mobility as high as 1.2 cm²/Vs and an ON/OFF ratio of 10⁶, and polysilicon TFTs with a field-effect mobility of 15 cm²/Vs and an ON/OFF ratio of 10⁵ can be achieved.

SELECTIVE CRYSTALLIZATION

Hydrogenated amorphous silicon (a-Si:H) films 150 nm thick, were deposited by PECVD using pure silane, on 1737 glass substrates at a substrate temperature of 150 °C, at RF power of ~0.02 W/cm². The usual process [3] for growth of a-Si:H for TFT fabrication is the same but the substrate temperature is 250°C. The substrate temperature was lowered to 150°C in this case because, due to the higher hydrogen content of the a-Si:H of 15 at.%, the lower growth temperature ensures a longer incubation time during crystallization anneal [5,6]. The subsequent

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exposure to atomic hydrogen was done in a parallel plate Reactive Ion Etcher (RIE) at room temperature. The RF power was 200 W, RF frequency was 13.56 MHz, the chamber pressure was 50 mtorr, the exposure time was 60 min, and the RIE electrode area was 250 cm². The samples were then annealed in a furnace at 600 °C in N₂. UV reflectance measurement [7] was done on all samples to monitor the crystallization process.

Exposing a-Si:H to room temperature plasma before the 600° C anneal greatly reduced the time taken to crystallize the amorphous film from the ~20 h required for an untreated film [4]. A hydrogen plasma has the largest effect, with the crystallization time reduced by a factor of five, and argon plasma had the smallest effect (Fig. 1). Exposure of an a-Si:H film to the hydrogen plasma leads to hydrogen abstraction from the surface of the film resulting in Si dangling bonds [5]. This facilitates the formation of silicon crystal nuclei, which act as seeds during subsequent annealing. This hydrogen-plasma-induced crystallite formation is limited to the top 30-40 nm of the surface [5]. The evidence of crystallite formation is indirect, because Raman spectrum analysis of the films was inconclusive. Most likely the crystallite size and number is too small to be detected by Raman spectroscopy.

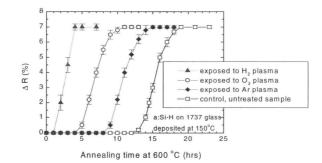


Figure 1. Change in UV reflectance at 276 nm as a function of annealing time for samples exposed to H_2 , O_2 or Ar plasmas. Untreated films shown for comparison [4].

The principle of area-selective crystallization is to protect selected areas of the a-Si:H precursor film from the plasma exposure by masking [4,5,7,8]. A 120 nm thick SiN_x mask film was deposited by PECVD using SiH₄, H₂ and NH₃, at substrate temperature of 200 °C and RF power of ~ 20 W [9], on a 150 nm thick a-Si:H precursor layer deposited at 150°C on 1737 glass substrate. The SiN_x was patterned by etching in dilute hydrofluoric acid (HF) and the sample was exposed to the hydrogen plasma. Then the samples were annealed at 600°C in a N₂ ambient, with the SiN_x capping the a-Si regions to minimize the out diffusion of hydrogen during the anneal.

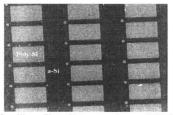


Figure 2. Optical micrograph of a silicon film with patterned areas ($100x200 \ \mu m^2$) of polycrystalline silicon (light) surrounded by amorphous film (dark) [4].

After ~4 hrs of anneal the portion of the a-Si:H film that had been exposed to the hydrogen plasma was completely crystallized (confirmed by UV reflectance measurement) while the unexposed regions were still amorphous. The SiN_x capping layer was then removed by etching in dilute HF. Both amorphous and polycrystalline silicon were obtained in a single silicon layer as can be seen in Fig. 2.

HYDROGEN EFFUSION AND NEED FOR RE-HYDROGENATION

A critical issue for the fabrication of a-Si:H devices in such a process is the loss of hydrogen from the amorphous regions during the 600 °C anneal. The SiN_x layer is a good diffusion barrier, but not sufficient to prevent out-diffusion of hydrogen in the film. To measure hydrogen content, 250 nm a-Si:H deposited on SiO₂/Si substrates (Si to allow infra-red measurement and thin SiO₂ to prevent crystallization during the anneal) were used. The atomic hydrogen content in the films was deduced from integrated absorption near 630 cm⁻¹, which is due to the Si-H and Si-H₂ wagging modes [10], with a conversion factor of 4.2×10^{-4} cm. The atomic hydrogen content in the as-grown a-Si:H was ~15 at.% and after annealing it reduced to about ~0.3 at.%. The defect state density, which results in mid-gap states, increased due to the hydrogen out-diffusion resulting in increase in sub-gap absorption as measured by photo-thermal deflection spectroscopy (Fig. 3). A similar loss of hydrogen is evident in Si-H stretching mode IR absorption at ~2000 cm⁻¹ (Fig. 4). The a-Si:H top-gate transistors made with this film had electron mobilities of only 0.01 cm²/Vs with an ON/OFF ratio of only ~10⁴.

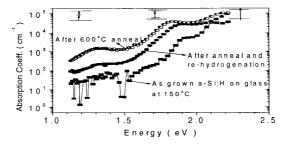


Figure 3. Photothermal deflection spectra of the optical absorption coefficient of a-Si:H films in the as-deposited, annealed with SiN_x cap layer at 600 °C, and re-hydrogenated states. The inset shows the relevant transitions at different energies in a band diagram.

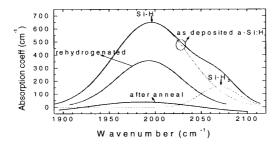


Figure 4. Infrared absorption specturm of the a-Si:H films around 2000 cm⁻¹ (Si-H stretch vibration). The spectrum of the as-grown film is decomposed into the Si-H and Si-H₂ components. The total H contents of the as-deposited film is ~15 at.%, of the annealed film (with SiN_x cap) ~0.3 at.%, and of the re-hydrogenated film ~4.4 at.%.

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Re-hydrogenation is necessary to reduce the defect state density in both the amorphous and polycrystalline regions of the film. This was done after stripping the patterned SiN_x cap layer with dilute HF. The hydrogen plasma conditions were chosen such that hydrogen abstraction and etching are minimal and hydrogen insertion is the dominant mechanism. This is realized by performing the re-hydrogenation in a plasma deposition system with lower sheath bias voltage, at an elevated substrate temperature of 350°C, a low RF power of ~0.2 W/cm² and at a high pressure of 1 Torr, so that the hydrogen ion energies are small (<30 eV) when compared to the hydrogen ion energy (~500 eV as estimated by the DC self bias) during the crystallization seeding process. The re-hydrogenation increased the hydrogen content of the film to ~4.4% as measured by the IR absorption at 630 cm⁻¹ for an exposure time of 75 min. The increase in hydrogen content resulted in the passivation of the Si dangling bonds and therefore led to a decrease in sub-gap absorption as can be seen in figure 3.

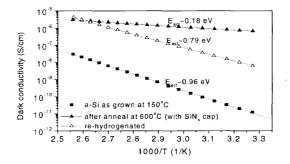


Figure 5. Dark conductivity measurement of the a-Si:H samples. A high activation energy reflects conduction above the mobility edge of low-defect density a-Si:H. Low activation energies reflect activated hopping through a high density of defect states.

Re-hydrogenation, in addition to increasing the hydrogen content of the a-Si:H improves the stability and the electrical characteristics of the film, as the hydrogen predominantly bonds in the form of Si-H in contrast to the as-grown a-Si:H film deposited at 150° C (Fig. 5) which had a considerable Si-H₂ content. The Tauc optical gaps calculated from the optical transmission spectra above the band-gap show that the optical band-gap of the film drops to 1.6 eV from 1.8 eV during annealing and that re-hydrogenation raises the band-gap value to 1.7 eV. Dark conductivity measurement shows that the conductivity of the a-Si:H film increases after the anneal and that the films have low activation energies indicating conduction through defect states. Re-hydrogenation brings the activation energy of the film closer to $E_g/2$ indicating a reduced defect density. But conductivity values are still not as small as that of the as-grown a-Si:H, which may explain the slightly higher leakage currents of the transistors (Fig. 8). Overall the data show that the capped a-Si:H film remains amorphous after the anneal and that the rehydrogenation results in a device quality a-Si:H film.

TFT FABRICATION AND RESULTS

After the re-hydrogenation step, ~50 nm of n⁺ microcrystalline (μ c-Si:H) silicon was deposited by PECVD using SiH₄, H₂ and PH₃, at pressure of 900 mTorr, RF power of ~0.3 W/cm², and a substrate temperature of 340°C. Device islands were then defined by dry etching in

a SF₆/CCl₂F₂ plasma and future channel regions were defined by dry etching just the n⁺ μ c-Si:H layer in a separate etching step using a CCl₂F₂/O₂ plasma.

The gate dielectric, ~180 nm of SiO₂, was then deposited by PECVD at a substrate temperature of about 250 °C using SiH₄ and N₂O at a RF power density of ~0.1 W/cm². Etching in dilute HF opened contact holes to the source and drain regions. Aluminum was then evaporated and patterned to form the gate, and source and drain contacts (Fig. 6). The samples were then annealed at 200°C in forming gas to reduce contact resistance. The same process was simultaneously applied in both polycrystalline and amorphous silicon regions. Note this is not a self-aligned process; the source/drain contacts process are similar to those in a standard bottom gate staggered a-Si:H TFT fabrication.

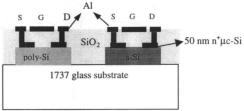


Figure 6. Cross-section of top gate integrated a-Si:H and poly-Si TFTs on glass substrate.

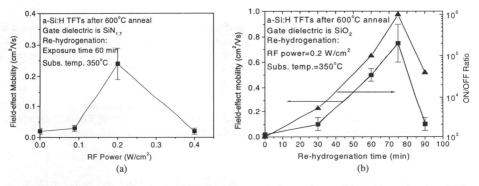


Figure 7. Field-effect mobility of the a-Si:H TFTs for different re-hydrogenation conditions, (a) as a function of RF power, and (b) as a function of exposure time.

Using a slightly different process, polysilicon TFTs with field-effect mobility as high as 75 cm²/Vs and ON/OFF ratio of ~10⁷ with a maximum process temperature of 600 °C were achieved [11]. The properties of the a-Si:H TFTs were critically dependent on the rehydrogenation conditions (Fig. 7). The best a-Si:H TFT performance was achieved for crystallization anneal of 625 °C and re-hydrogenation time of 75 min at RF power density of 0.2 W/cm², resulting in a field-effect mobility of ~1.2 cm²/Vs and ON/OFF >10⁶ (Fig. 8(a)) [6].

For the optimized case with both a-Si:H and polysilicon TFTs integrated together, the field-effect mobilities were ~0.7 and ~15 cm²/Vs for the a-Si:H and poly-Si TFTs respectively. The leakage current was ~10 fA/ μ m at V_{DS} = 10 V for the a-Si:H in the OFF state. The ON current of the poly-Si TFT was \geq 0.5 μ A/ μ m, with ON/OFF ratios of both types of devices \geq 10⁵ (Fig. 8(b)). This is the first demonstration of the integration of a-Si:H and poly-Si TFTs on the

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same substrate in a single layer without laser processing. These results compare favorably with other work on integrated a-Si and poly-Si TFTs using laser processing which resulted in a-Si TFTs with field-effect mobility of ~0.9 cm²/Vs and poly-Si TFTs with field-effect mobility of ~20 cm²/Vs [1]. These are also the best results for a-Si:H top gate TFTs after a 600 °C anneal step.

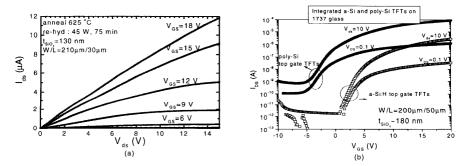


Figure 8. TFT characteristics of (a) the best a-Si:H top-gate TFT fabricated after 600 $^{\circ}$ C anneal with linear field-effect mobility of ~1.2cm²/Vs, and (b) optimized integrated a-Si:H and poly-Si TFTs on the same glass substrate.

CONCLUSION

We have successfully integrated high performance a-Si:H and poly-Si TFTs in a single Si layer on the same glass substrate, using a hydrogen-plasma selective crystallization technique. The TFTs share all processing steps and no laser processing is involved. Re-hydrogenation is critical after the crystallization anneal at 600 °C to obtain a device quality a-Si:H film.

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