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Teaching Systems Performance Limitations Through an Integrated Circuit Fabrication Laboratory

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ABSTRACT

Because the physical implementation and hence performance limitation of many aspects of Electrical Engineering rely on the integrated circuit, all Princeton EE majors take a course to understand the fabrication and operation of ICs. In the lab portion of the course all students fabricate their own IC chip. The goal of the course is not to understand in depth the detail of the physical processes behind transistor operation or chip fabrication, but rather to show how basic analog, digital, and opto-electronic functions may be integrated onto a chip. The students test the circuits using needle probes and a microscope so they can see the circuit while measuring its limitations. Through lab and lecture the connections between the physical parameters, such as line width on a chip and system parameters such as power delay product (digital) or gain bandwidth product (analog) are developed.

INTRODUCTION

Recently at Princeton, the Electrical Engineering (EE) curriculum has been revised to accommodate the needs of a student interested in engineering in the modern world of sophisticated systems technology. The new students do not have the background in tinkering with systems by taking them apart and fixing them, because with the cover off, a modern system (such as a TV or radio) reveals just an inaccessible layer of complex boards and integrated circuits (ICs). The curriculum revisions included changing an upper-level elective IC fabrication laboratory course to a required sophomore level course. More details concerning the reasoning behind this change are presented in the motivations section of this paper. The new requirements needed to make this change are discussed in the implementation section, and finally a new set of experiments which were designed to show how systems are integrated on an IC and to measure the performance limitation of these simple systems are described in the final section of this paper.

MOTIVATION

The new introductory curriculum at Princeton focuses on solving problems across the entire EE field, and away from narrowly focused specialty courses centered around various tools and methods. This is accomplished through four required sophomore level courses which are: An Introduction to EE Systems and Signals, Electric Circuits, Digital Logic, and Integrated Circuits: Practice and Principles. The four courses span the scope of electrical engineering and are not designed to be an introduction of various tracks for people keen on majoring in that track. Rather, they are designed as a broad overview, more to instill what the basic concepts and goals are in the area for the non-specialist. In the area of integrated circuits, an IC fabrication laboratory course was chosen because ICs are at the heart of all modern systems, not only computer systems, but other

systems such as appliances, automobiles, and scientific equipment, etc. as well, and though students can easily gain experience using integrated circuits, the details about how the IC is made remains a mystery to all EEs not specializing in that field.

The course itself will not focus on the physical and chemical principles behind the fabrication and operation of integrated circuits, but rather will concentrate on the integration of transistors to create system functions. In modern IC systems, literally millions of transistors are interconnected on one chip to create sophisticated equipment such as computers. This concept is very difficult to present in lecture, because with no prior knowledge, the fabrication steps required to make an IC seem like magic. It is easy to describe in lecture the current flow into the pin of the familiar IC package, or the voltage across that pin and the ground terminal, or the fact that it is part of an address bus or data bus, but it is very difficult to describe how a million interconnected transistors got inside that little plastic package in the first place. Therefore, each student will make their own chip in the lab. This takes the mystery out of the fabrication process and allows the students to see how integrated systems are created on a chip.

The systems that the students create will be at the level of small scale integration (less than 100 transistors). Although these systems are extremely small as compared to modern integrated systems, they are still very useful to highlight a system limitation. In the field of analog electronics, integrated amplifiers will be tested to show gain-bandwidth limits. For opto-electronics, the signal to noise ratio limit will be addressed, and in the field of digital electronics, the power-delay product limit will be presented.

IMPLEMENTATION

The new IC fabrication lab is modified from a previous upper-level elective course which focused on the physics and chemistry of transistor fabrication and operation. While this course did take the mystery out of IC design for the students involved, the lab concentrated on sophisticated measurements which delve into the intricacies of semiconductor device physics. This detailed knowledge is important to a student specializing in semiconductor engineering, but is not required knowledge for all electrical engineering students.

To create a systems level approach from the old lab, the only requirement is to change the mask design. A fabrication process requires masks to form a specific pattern in thin films as they are sequentially applied to a chip. A particular mask design can produce a discrete transistor, while an integrated circuit is just a group of transistors interconnected to perform a function. The fabrication steps that were used to create discrete transistors are exactly the same as those required to make an integrated circuit. At Princeton, the process used is a four level, 25μm, PMOS process, which is outlined in the left-hand column of Table 1. Once the new mask set is designed, the fabrication portion of the lab is taught exactly as it was for upper-level course. Note, the new mask only has to be designed once and can be re-used for each new lab session.

The measurements portion of the lab also has to be modified to correspond to the circuits created by the new mask set. This will be done by combining the three measurements sessions of the old lab to the three sessions at the end of the semester, as shown in Table 1. During each of the last three sessions, the students will choose to perform one of the five new experiments. In this way, students will be exposed to the three systems level experiments that interest them most. Also,

measurements performed in the old lab on the physics of semiconductor devices will be combined together into one of the new experiments, so a student interested in semiconductor engineering can still benefit from this portion of the lab.

Table 1. A list comparing the ten lab sessions for the old lab in the first column and the new lab in the second column.

Lab Week	Old Lab Sessions	New Lab Sessions
1	Lab tour; Safety discussion; Determining charge carrier type; Determining resistivity.	Lab tour; Safety discussion; Determining charge carrier type; Determining resistivity.
2	Solvent clean; Acid clean; Wet oxidation.	Solvent clean; Acid clean; Wet oxidation.
3	Photolithography Level 1; Oxide etch; Strip resist; Solvent clean; Acid clean; Spin on dopant glass.	Photolithography Level 1; Oxide etch; Strip resist; Solvent clean; Acid clean; Spin on dopant glass.
4	Diffuse; Crack dopant glass; Etch dopant glass; Cleave wafer; Solder diode portion to glass slide.	Diffuse; Crack dopant glass; Etch dopant glass; Demonstrate diode electrical characteristics.
5	Measure diode electrical characteristics.	Photolithography Level 2; Oxide etch; Strip resist; Solvent clean; Acid clean; Dry oxide.
6	Photolithography Level 2; Oxide etch; Strip resist; Solvent clean; Acid clean; Dry oxide.	Photolithography Level 3; Oxide etch; Strip resist; Photolithography Level 4.
7	Photolithography Level 3; Oxide etch; Strip resist; Photolithography Level 4.	Evaporate aluminum; Lift-off; Sinter & Anneal; Solder to glass slide.
8	Evaporate aluminum; Lift-off; Sinter & Anneal; Solder to glass slide.	Experiment 1 - required; Choice of Experiments 2-5.
9	Measure MOS capacitor electrical characteristics.	Choice of Experiments 2-5.
10	Measure MOSFET electrical characteristics.	Choice of Experiments 2-5.

To allow the students to perform their own experiments, the lab will be upgraded from three stations to six stations. New electronic equipment has been purchased to accommodate the new experiments. To save costs each station does not need to be equipped to perform every experiment. Also note, that to expand the lab (such as creating new experiments), only requires upgrading the mask set to accommodate new systems, and will most likely be pursued in the future.

EXPERIMENTS

The five experiments are each designed to be completed in one lab session. Below is a list of each experiment and a general description on how it pertains to teaching systems performance limitations. A drawing showing the important feature of the mask design is shown in Figure 1. This figure can referenced to enhance the description of the experiments.

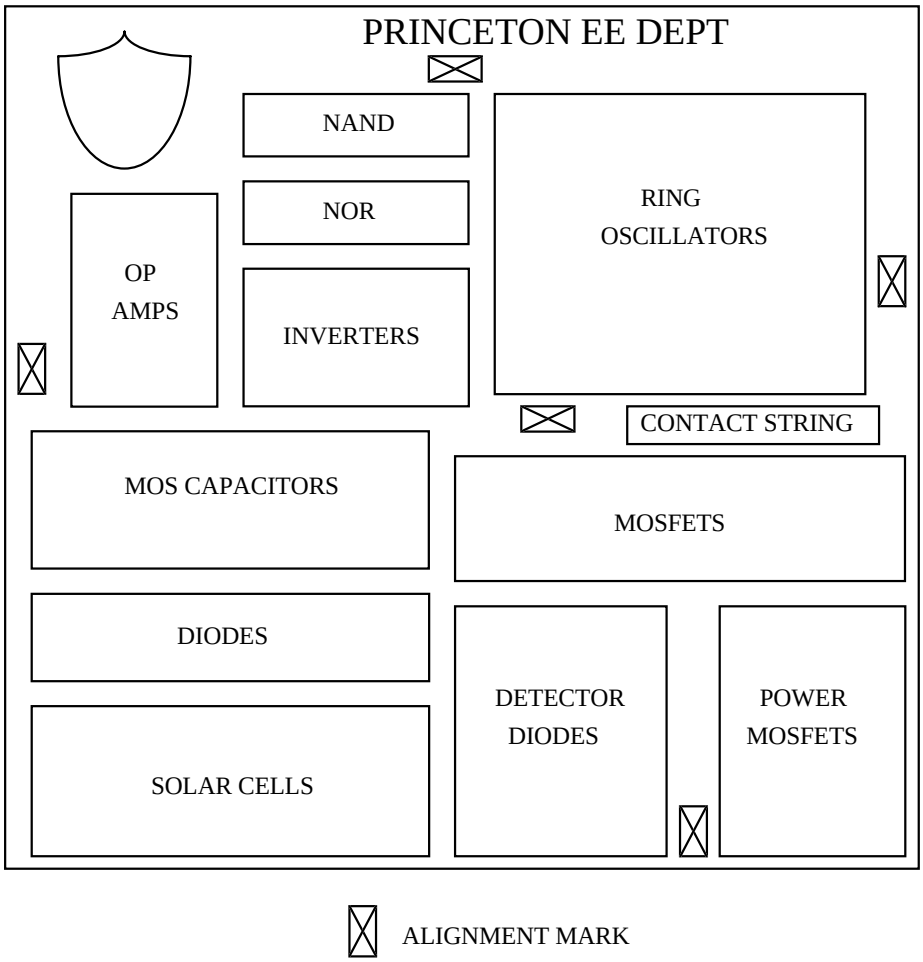

Figure 1. Integrated circuit "road map" showing the important features on the new mask design.

Experiment 1 : MOSFET Characterization

Because all integrated systems are based on the operation of the MOSFET, all students are required to perform an experiment which highlights the operating principle of the transistor. A curve tracer is used to display the current-voltage characteristics of a device. From the display, data is taken to calculate the threshold voltage, the transconductance, and the carrier mobility of the MOSFET. The results can be used for calculations in subsequent labs.

Experiment 2 : Semiconductor Device Physics

This experiment will remain as a choice for those students who wish to pursue semiconductor engineering. The detailed measurements of diode current-voltage and capacitance-voltage characteristics will be measured. Also, the MOS capacitor capacitance-voltage

characteristics and the MOSFET current-voltage characteristics will be measured for various size devices. The analysis will deal with many of the famous semiconductor device physics equations and will yield results about the properties of the semiconductor material and device fabrication process.

Experiment 3 : Digital Gate Performance

The inverter circuit, the simplest logic gate available in IC design, will be studied. The voltage in-voltage out transfer function will be plotted for inverters containing transistors of various dimensions, showing how the optimum choice is made. Then ring oscillators, a series of an odd number of inverters connected in a circular chain, each made with increasingly smaller line-widths will be tested. The power-delay product will be measured showing improved system performance for smaller devices. This will provide insight into the drive for miniaturization. Finally, NAND and NOR gates will be included for a quick test of logic truth-tables.

Experiment 4 : Opto-electronics

The diffused diodes in the PMOS process can be used as solar cells. The old lab schedule included testing of the solar cell using a HeNe laser. This experiment, in which the solar cell efficiency is determined, will be included in the opto-electronics experiment. In the second part of this experiment, the diode will be used as an optical detector. Four different sized diodes will be connected with an external amplifier, such that the gain-area product of each detector is the same. The detector will be driven by an amplitude modulated light beam using an audio sound source such as a frequency generator or radio. When the beam is directed over the diode with a fiber optic cable, the amplifier will drive a speaker. It will be shown that the smallest diode provides the highest bandwidth, but suffers from the worst signal to noise ratio.

Experiment 5 : Analog amplifier

In this experiment, a single transistor amplifier is created using an external biasing circuit. It is determined how to properly bias the transistor for audio amplification applications. Again, transistors of various line-widths are used. The gain-bandwidth product for each is measured, showing the improved performance for smaller geometries. Next, a completely integrated analog amp is tested and it shown how the entire external biasing circuit (a box of several inches in dimension) can be completely integrated onto a chip in a size no larger than your fingernail.

Future Experiments

Future improvements in the lab will consist of creating new experiments. An obvious extension is to include memory systems. Memory systems such as RS or JK flip-flops, or static or dynamic read only memory will be pursued.

CONCLUSION

An upper-level elective course has been changed to a sophomore level required course as part of a new curriculum in the undergraduate EE program at Princeton University. The course, which was a lab course for students specializing in semiconductor materials and devices, has been modified to be presented to the entire EE community. The new experiments are designed to teach the performance limitations of small integrated systems. This is done by allowing the students to fabricate their own IC chip which includes circuits representing a variety of applications.