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Industry/University Teaming for Display Research

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ABSTRACT

In an effort to raise the efficiency and speedup the rate of technology transfer from its university funded research programs, DARPA has been encouraging the formation of industry/university teams to accelerate the development of backplane thin-film electronics for AMLCD displays. The effort among its university researchers has been carried forward through voluntary participation in a series of workshops cosponsored by DARPA and the Electric Power Research Institute. Evidence of the effectiveness of the teaming arrangement is shown by the many collaborations entered by the display industry participants.

Keywords: industry/university teams, display research, a-Si:H TFTs, polysilicon TFTs

1. INTRODUCTION

A number of U.S. corporations are manufacturing active matrix liquid crystal displays (AMLCDs) using a-Si or polysilicon thin-film transistors (TFTs). For this industry, the large-area deposition and processing of thin-film semiconductor circuits represents an enabling technology. The Defense Advanced Research Projects Agency (DARPA) as part of its High Definition Systems program has been sponsoring research in both industry and university laboratories to advance the U.S. capabilities in that enabling technology. In order to increase the returns from their sponsorship of that research, DARPA has sought a paradigm shift in how university research is applied. One approach to this paradigm shift has been to apply the customer-focused team approach, developed by the Electric Power Research Institute (EPRI) and used successfully by the National Renewable Energy Laboratory.[1,2] This customer-focused team approach includes the following steps. Research problems are identified and defined by a polling of industrial researchers. Teams are then formed among university and industry researchers to determine the root causes of the problem and adopt a program plan to solve it. The next organizational step is the most time consuming: Customer-related and -accepted metrics (measurable goals) that define research progress must be established by the teams. During the entire period of research, continued interest of, and participation by, industry must be maintained if the results are to be transferred to industry. In this paper we report on the activities and progress of the teaming efforts that have been undertaken in the DARPA sponsored backplane electronics university research programs.

2. PROBLEM DEFINITION

The customer-focused team approach began with a series of twice yearly workshops in November, 1993 that brought together researchers from the display industry, including manufacturers and suppliers, university researchers, researchers from the national labs, and program managers from DARPA and the military services. The purpose of the workshops has been and continues to be to address TFT manufacturing and materials issues needing resolution for the U.S.

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AMLCD industry to achieve world class competitiveness. In addressing these issues the workshop sought to: 1) stimulate communication among industry and university researchers and avoid inefficient duplication of effort; 2) increase the rate of progress in thin-film TFT research necessary for higher performance/lower cost display products; and 3) promote technology transfer among universities and the display industry.

Figure 1 shows the results of the TFT technology analysis derived in the initial workshops with input coming mainly from the industrial participants. The fishbone diagram defines those areas of research that require attention for industry to attain its goal of low-cost high-performance active matrix displays. The diagram contains both the key issues, e.g. device design, semiconductors, interfaces, etc., and the root causes that must be addressed. Further discussion among the workshop participants led to a ranking of the top five root causes listed below in Table 1. These were judged to be the areas were the most leverage could be gained by U.S. industry from university research.

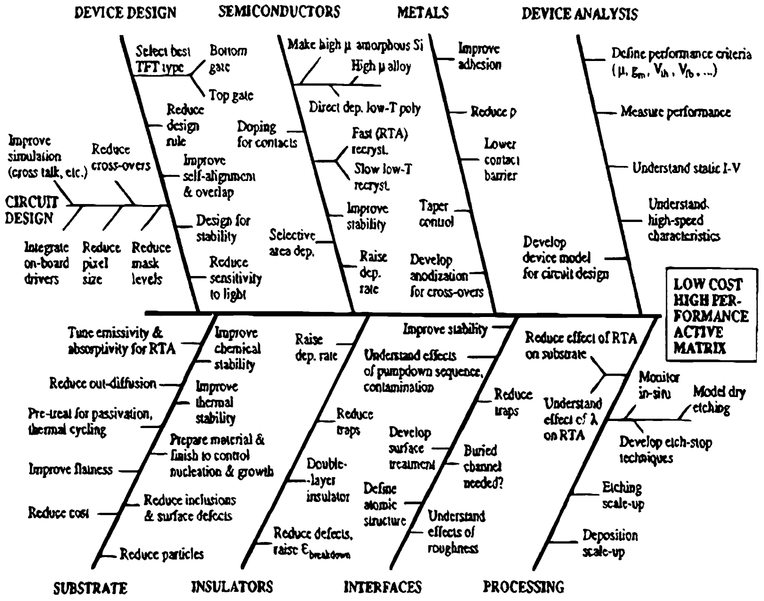

Figure 1. TFT Technology Analysis

RANK	ROOT CAUSE
1	Need higher performance TFTs with manufacturable process
2	Circuit design not fully developed for functionality, test and repair
3	Need simulation for TFT design including quasi-static and transient behavior
4	Process window too narrow
5	Manufacturing costs too high (Equipment ownership, material, etc.)

Table 1: The top five root causes for lack of progress in AMLCDs

3. PROBLEM ANALYSIS, PROGRAM PLAN AND PROGRESS MEASUREMENT

The technology analysis developed with input from industry led to the organization of five university-industry team areas in which the appropriate university research and university/industry collaborations could be placed. The five team areas are listed in Table 2. All of the DARPA funded research already could be categorized within one or more of these teams. However, the exercise of determining the key issues and defining the teams brought new perspective and direction to almost all of the university programs. Also, it brought to the university researchers attention who the customer for their research product is and a greater understanding of the industrial customer's priorities and requirements.

TEAM RESEARCH AREAS
Team 1: High Performance a-Si:H TFTs
Team 2: High Performance Polysilicon TFTs
Team 3: a-Si:H Process and Manufacturing
Team 4: Polysilicon Process and Manufacturing
Team 5: TFT Simulation

Table 2: Research Teams

A final, but key organizational step to implementing the team approach was to establish customer-related and -accepted metrics (measurable goals) that define research progress. This was accomplished by identifying the key issues that must be addressed for successful implementation of the technology. When the key issues have been agreed to, then values can be chosen that provide the state-of-the-art value for the parameter associated with the key issue. After the state-of-the-art values have been agreed to, then near and long-term goals for improvement in those values can be established. As is the case in much of the initial effort in setting up the teams, industry's input provides numbers for the required improvements. The results of this effort are shown in Tables 3-7. The program plan represented in Tables 3-7 has been supplemented recently by a document prepared by a workshop subcommittee titled "Industry Suggestions for University Research Critical to Display Manufacturing." This document is an update, and an extension to flat-panel display research. The purpose of this document is to identify university research that is needed by U.S. display manufacturers, and to identify topics suitable for university-industry research collaboration. Research areas that specifically called for are TFT stress work which would significantly extend AMLCD function. Specific improvements needed in a-Si:H technology are: 1) improved TFT mobility and transconductance, 2) improved manufacturability and low cost manufacturing, 3) improved uniformity of large area plasma processing, and 4) processing improvements for low resistivity metallurgy (Al, Cu). Priority areas for polysilicon research include: 1)large area processing, specifically crystallization (laser, RTA), hydrogenation, doping process, dopant activation and low temperature gate dielectrics; and 2) design for low power consumption drive circuitry (row and column drivers in polysilicon CMOS).

The data in Figures 2-5 continues to be updated at successive workshops. Many of our near-term goals have already been met since the industry/university teaming began. For example, in the area of a-Si:H TFT performance metrics, mobilities of greater than 1cm^2/V-s have been achieved. Substrate temperatures during the deposition of the semiconductor and insulator layers have been reduced as low as 130°C with PECVD and with reactive sputtering. In the area of polysilicon process and manufacturing metrics, Penn State has demonstrated defect passivation using high density plasma sources that meets the near-term goal of 60 plates/hr. The group at Lawrence Livermore National Laboratories has demonstrated exceptional TFT properties for laser crystallized polysilicon at substrate temperatures that also do not exceed 130°C. In order to increase the value of the information being generated and enhance the technology transfer rate the teams have developed measurement protocols for a-Si:H and polysilicon TFTS, and have established stress protocols for the determination of stability issues. Finally, in order to make it easier for universities to experiment and for industry to interpret their data, a TFT mask set has been designed and fabricated through the cooperation of OIS, Intevac, and Penn State. The five-level mask set is available to any interested party through the National Nanofabrication Facility at Cornell University.

4. RESULTS PROPAGATION

The teaming effort has succeeded in several ways. First, it has brought industry and university researchers into much closer communication through the series of twice yearly workshops. Here they meet to discuss the key issues and the progress of their research and initiate collaborations. The timely exchange of information has also helped avoid inefficient duplication of effort. Also in a context of industrial advising, the different university groups continually share information amongst themselves and thus immediately benefit from the others experience. This has the effect of maintaining competitiveness while at the same time accelerating the progress of all the groups involved. Because of the continued and active support of the display industry, technology is transferred at a much greater rate from the universities to industry. In addition, because the teams receive continued input from industry, the relevance of the technology created by the universities is very high.

The minutes of each of the workshops (there have been eight thus far) are made available to the participants and others who express interest. Further, participation in these workshops is not limited to universities that have contracts in the DARPA High Definition Systems Program but is open to any group that can contribute and wishes to do so. Results are also made available to the larger display industry community through the participation of organizations such as the USDC in the workshops activities.

5. FUTURE PLANS

Future plans call for the further strengthening the workshop format as a forum for hosting and encouraging industry/university collaboration. Future workshop topics will include organizing collaborations on FPDs, beyond the present focus on TFT backplanes of industry and the possibility of forming a distributed foundry for display research.

ACKNOWLEDGMENTS

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University Industry Collaborations	Key Issues	State-of-the-art Value	Near-term Goal (bottom gate, 1024 x 1280 x 3, 10" to 20" diag, ~1000 rows	Long-term Goal (Self-aligned, 21" diag, ≥5000 rows)
AT&T-Princeton TEL-Penn State IBM-U of Illinois	I_{ON}	$\mu_n = 0.7$ cm^2/V-s $V_{TH} = 1\text{-}2$ V	$\mu_n \geq 1$	
	Capacitance, C	C_{CG} $C_{OVERLAP}$ 200 pf/μm ΔC	→ 0	→self-aligned
	Scan line Resistance Processability		¼ Ω/□	
	Stability	V_{TH} μ I_{SD}		Define measurement
IBM-Penn State	S/D resistance	w/o μ loss	< channel R	< channel R
	I_{OFF} S/D Leakage	10^{-15} A/μm $V_{SD} = 10$ V	don't increase	don't increase
	Photocurrent			

Table 3: A-Si TFT Performance Metrics

University Industry Collaborations	Key Issues	State-of-the-art Value	Near-term Goal (bottom gate, 1024 x 1280 x 3, off for direct view, 2" to 4" diag, T≤600°C, low thermal budget)	Long-term Goal (4000 lines at 1200 lpi (x3), T≤600°C, low thermal budget)
IBM-NCSU OIS-Penn State Xerox-Stanford	I_{OFF} Pixel and Periphery I_{OFF} distribution	$I_{OFF} = 10^{-13}/\mu m$ @ $V_{SD}=10V$ $V_G = 20V$	Maintain while reducing channel length	Maintain while reducing channel length
	S/D Properties Pixel and Periphery	Contact resistance less than channel resistance		Single gate with no LDD and symmetric structure
	I_{ON} Pixel and Periphery	μ_n=50-100 cm^2/V-s	Maintain μ_n, reduce I_{OFF} and decrease channel length	Maintain μ_n, reduce I_{OFF} and decrease channel length
	Stability Pixel and Periphery		Need to define measurement and stress	
	Scan Line Resistance Pixel and Periphery		¼ Ω/□	
	V_{TH} Pixel and Periphery	V_{TH}=1-3 V	Remains the same	Remains the same
	Periphery TFTs PMOS μ_p and V_{TH}	μ_P=20-50 cm^2/V-s V_{TH}=-10 V	μ_p and V_{TH} same as NMOS	μ_p and V_{TH} same as NMOS

Table 4: Projection/Direct View Polysilicon TFT Performance Metrics

University Industry Collaborations	Key Issues	State-of-the-art Value	Near-term Goal	Long-term Goal
U of Alabama-Princeton	Throughput: process steps		In general reduce mask count	
Intevac-U of Illinois	Throughput: deposition rate	1500-2000 Å/min		Understanding high-density plasma and it effect on process (generic issue)
	Metallization: interaction with ITO Process time			Adhesion (Cu), taper, undercut, etchability
	Particle control ($\geq 0.5\ \mu m$)		$0.3/cm^2$ size?	
	ESD → V_{TH}	≤ 500 V	Define measurement	
	Selectivity: Etch, Deposition			
	Glass cleaning Monitoring cleanliness		Generic issues	
	Photolithographic tools		Generic issues	

Table 5: A-Si Manufacturing Metrics

University Industry Collaborations	Key Issues	State-of-the-art Value	Near-term Goal	Long-term Goal
Xerox-Penn State	Defect Passivation		60 Plates/hr	Get rid of need for passivation- particularly hydrogen
Xerox-XMR-LLNL-Arizona State Intevac RTP-Lehigh Intevac RTP-Stanford Intevac RTP-Penn State	Poly recrystallization a-Si crystallization		Large area, reproducibility (uniformity) Large area, reproducibility (uniformity) Throughput ≤5% change in all properties of On-state glass compatible	
	Large area S/D doping			
Xerox-Penn State	Yield and Repair		Reduce plasma damage	
	ESD		$\Delta I_{OFF} \leq 10\%$	

Table 6: Polysilicon Process and Manufacturing Metrics

University Industry Collaborations	Key Issues	State-of-the-art Value	Near-term Goal	Long-term Goal
Xerox-U of Virginia Xerox-Princeton Xerox-Sandia-Cornell	Device simulation Amorphous Polysilicon	Quasi-static		
OIS-Penn State	Quasi-static Transient	semi ver.-a AMPS (1D-2D) semi ver.-a AMPS (1D-2D)		Transient-amorphous and poly
Xerox-Arizona State	Sensitivity analysis		Link between process and model	

Table 7: TFT Simulation Metrics