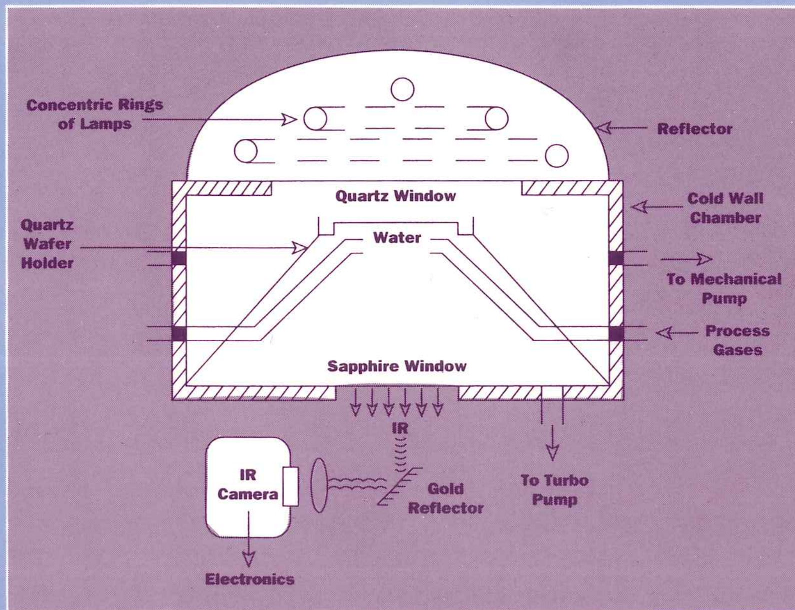
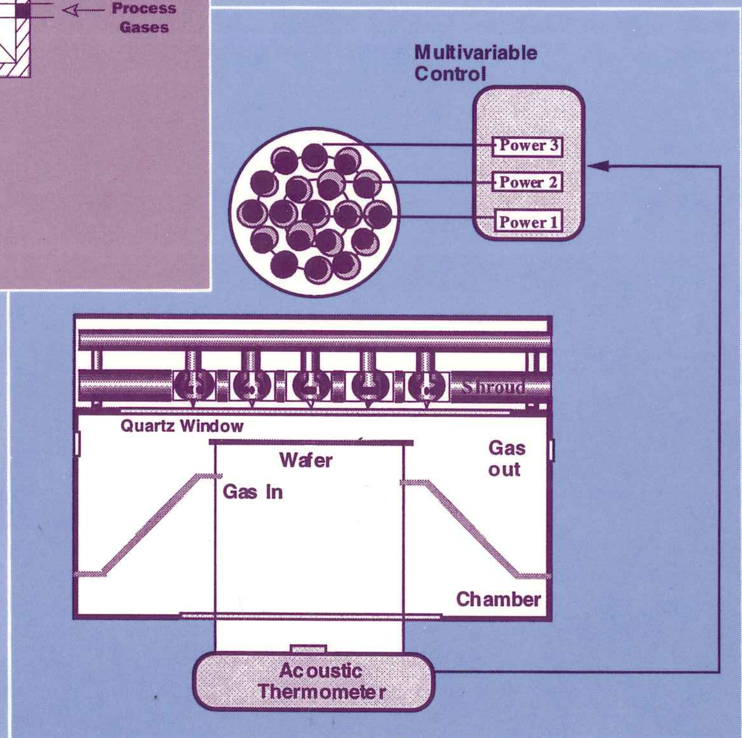
TRANSIENT THERMAL PROCESSING TECHNIQUES IN ELECTRONIC MATERIALS





Edited by

N. M Ravindra
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Rapid Thermal Chemical Vapor Deposition of Silicon-Based Heterostructures

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Abstract

Rapid Thermal Chemical Vapor Deposition (RTCVD) has been one of the leading techniques used for the epitaxial growth of silicon-based heterostructures. This paper examines three critical aspects of low-temperature epitaxial growth which relate to the growth of high quality heterostructures. The first is the fortuitous role of hydrogen in passivating the growth surface during low-temperature CVD. This hydrogen layer suppresses the adsorption of oxygen and water vapor, leading to high purity layers, and suppresses surface segregation, leading to sharper interfaces. The paper then examines the low-energy photoluminescence often seen in $Si_{1-x}Ge_x$ grown by Molecular Beam Epitaxy. By recreating this deep luminescence in samples grown by CVD, we show that the source of this deep luminescence is radiation damage, which may occur during the MBE growth process but which is inherently absent in the CVD process. Finally, we show how $Si_{1-x-y}Ge_xC_y$ substantially relaxes the critical thickness limits inherent in $Si_{1-x}Ge_x$/Si heterostructures.

Introduction

In the last several years there has been an increasing interest in Column-IV heterostructures for high performance electronic and opto-electronic devices. The main reason for this interest has been the possibility of integrating these devices with VLSI, and hence nearly all of the work has been performed on Si (100) substrates. Most of the research in the field has been performed using either Molecular Beam Epitaxy (MBE) or various forms of Chemical Vapor Deposition (CVD) to grow the heterostructures. In the CVD field, one can choose from growth pressures ranging from that in Ultra-High Vacuum (UHV) CVD (about 1 mtorr) [1] up to atmospheric pressure [2], nearly 6 orders of magnitude higher. Most of the materials work to date has been focused on the $Si_{1-x}Ge_x$ material system, but the limits of that material system by now have been fairly well explored.

In this paper, the Rapid Thermal Chemical Vapor Deposition (RTCVD) growth technique will first be reviewed. The beneficial effects of hydrogen for low-temperature CVD will then be examined. Next, both the MBE and CVD growth techniques will be contrasted from a fundamental point of view, and it will be shown that CVD is inherently better suited for the growth of high-quality material in many cases. Finally, the role of carbon in extending the limits of the $Si_{1-x}Ge_x$ material system through $Si_{1-x-y}Ge_xC_y$ alloys will be shown.

Overview of Rapid Thermal Chemical Vapor Deposition

All work at Princeton to date was performed in a load-locked RTCVD reactor shown schematically in Fig. 1. The reactor consists of a 175-mm quartz tube in which a 100-mm silicon wafer is suspended on quartz pins and heated by an external bank of tungsten halogen lamps. The wafers are introduced to the reactor through a load lock. A typical deposition pressure is 6 torr, and source gases are typically dichlorosilane, silane, germane, methylsilane (for carbon), diborane, and phosphine, all in a hydrogen carrier [3]. Both the reactor and load-lock are exhausted by common rotary vane pumps, and both the reactor and load-lock are pumped down to a pressure of ~100 mtorr when loading wafers. For high-quality growth at low temperature, in our experience it is far more important that the reactor be leak-tight and gases be clean rather than pumping the load-lock and growth chamber to low base-pressures with every sample. A turbo-molecular pump is attached to the growth chamber, but is not routinely used. When used, the base pressure of the reactor is in the range of 1 x 10^{-8} torr.

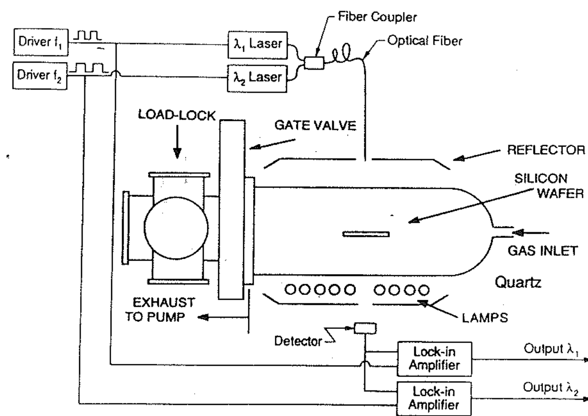

Fig. 1. Schematic cross section of RTCVD reactor used in this work with temperature measurement by infrared transmission.

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The desire for 2-D growth in $Si/Si_{1-x}Ge_x$ structures (as opposed to 3-D growth) [4] and abrupt interfaces generally limits the growth temperatures to under 700 °C. Because of the relatively fast increase of dopant diffusion coefficients at high temperature, a thermal budget of only a few seconds at 1000 °C is already too long to achieve the interface abruptness desired for heterojunction devices [3]. Because of the lower growth rates at low temperatures (1 - 10 nm/min), the growth times of typical layers (10 nm) are on the scale of 100 s or more. Therefore minimizing the thermal exposure of the wafer on the scale of seconds is not required. One can therefore establish the wafer temperature before the reactive gas flows are turned on, and hence turn the growth reaction on and off as in a usual CVD process. The Limited Reaction Processing (LRP) approach [5], which involves establishing the gas flows first and turning the growth on and off with very rapid temperature transients to minimize the thermal exposure, is generally not required.

On the other hand, because different CVD processes have different optimum temperatures, the need for rapid switching of the sample temperature remains, so that the temperature for each layer in a heterostructure may be optimized. For example, at 700 °C the growth rate of silicon from dichlorosilane is an acceptable 3 nm/min, but it decreases to only 0.1 nm/min at 625 °C. On the other hand, because of a fortuitous catalytic reaction when growing $Si_{1-x}Ge_x$ layers, $Si_{0.8}Ge_{0.2}$ layers, which require 650 °C or less to avoid 3-D growth and to enhance metastability, have a growth rate of 10 nm/min at 625 °C. Because of the ability of a RTCVD reactor to rapidly change the sample temperature, the temperature of a wafer is then typically changed for each layer in a multi-layer structure.

For temperatures under 800 °C, silicon-based CVD growth rates are typically an exponential function of temperature. This is a drawback of RTCVD, since the resulting temperature measurement and uniformity requirements are generally more severe than those for higher temperature processes (e.g. rapid thermal oxidation). In our reactor, we measure the wafer temperature at only a single point using an unusual infrared transmission technique (Fig. 1) [6,7]. The transmission of 1.3 and 1.5 μm light through the the substrate is measured in situ, and through lock-in techniques the interference from the lamps can be avoided even though the detected transmitted power is only on the order of pW or nW. The transmission depends strongly on temperature due to both bandgap and free-carrier absorption, both of which exponentially depend on temperature [8]. Using this technique, we routinely measure the wafer temperature in the range of 500 - 800 °C with an absolute accuracy of ~ 1 °C, without any assumption of emissivity, etc. Our reactor is not optimized for uniformity across the wafer, however.

Hydrogen Surface Coverage Effects

At temperatures in excess of 900 °C, it is fairly easy to maintain a clean Si surface (a pre-requisite for high quality epitaxial growth), due to the rapid desorption of SiO and related species. Therefore the common ppm levels of gas contamination are not a substantial impediment for high quality silicon epitaxy. At low temperature the situation is much different, due to the increased stability of water and oxygen on the silicon surface. The original motivation for UHV-CVD (growth pressure of 1 mtorr) was to reduce the partial pressures of water vapor and oxygen from gas contamination or reactor background to levels low enough to prevent the formation of surface oxides, which would degrade epitaxial quality [1]. These critical partial pressures were determined by steady state experiments performed in UHV on silicon surfaces [9] (Fig. 2). For example, from Fig. 2, one may infer that to achieve a clean surface at 700 °C, the partial pressure of oxygen in the growth environment must be less than 10^{-8} torr. Consequently, for a growth pressure of one atmosphere (760 torr) or 6 torr (as used in our reactor), the source gases must be purified to a level of 0.01 or 1 ppb, respectively. This is beyond the range of gas purifiers available on the market today. A growth pressure of 10^{-3} torr could tolerate a gas contamination level of 10 ppm (easily achieved), giving a strong motivation for growth at such low pressures. Similar arguments can be made for water vapor, which in practice is probably a worse problem than oxygen.

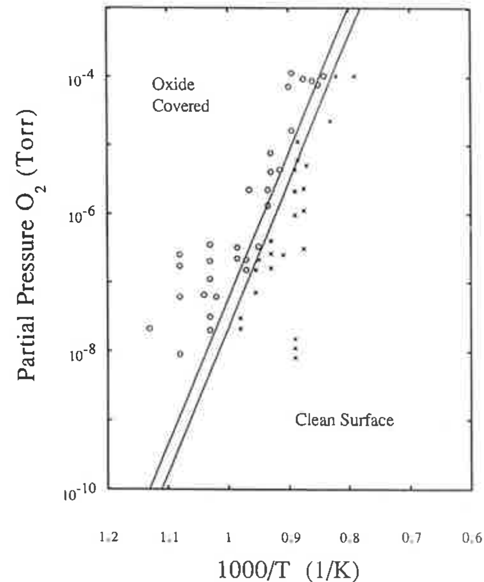

Fig. 2. Criteria for a clean Si surface as a function of temperature and oxygen partial pressure [9].

However, since the initial success of UHV-CVD at low

temperature, others have succeeded in the growth of high quality layers with oxygen levels under 10^{18} cm^{-3} and with low defect densities in the range of 600-700 °C at pressures ranging from several torr up to atmospheric pressure [10,2], even though the partial pressures of contaminants were certainly many orders of magnitude higher than those expected to limit epitaxial growth in the above arguments. To probe the reason for this success, we intentionally introduced oxygen contamination into the growth chamber during the low-temperature epitaxial growth of silicon in the 700-750 °C range using a hydrogen carrier at 6 torr. The resulting oxygen levels in the silicon were then measured by SIMS and infrared absorption and found to be linear with the oxygen gas flow (Fig. 3) [11]. Assuming the oxygen is uniformly distributed through the growth chamber, from the growth rates and oxygen levels we calculated the effective sticking coefficients of the oxygen on the silicon surface. They were found to be $\sim 10^{-4}$ [11], two orders of magnitude smaller than those measured in UHV studies. Extrapolating the high oxygen levels measured in this study (over 10^{20} cm^{-3}) down to the levels of $\leq 10^{18}$ cm^{-3} observed when oxygen was not introduced, we infer that that an oxygen level of 50 ppb is tolerable in the source gases. Such a purity level is within range of gas purifiers, and is consistent with the fact that high quality layers could be grown.

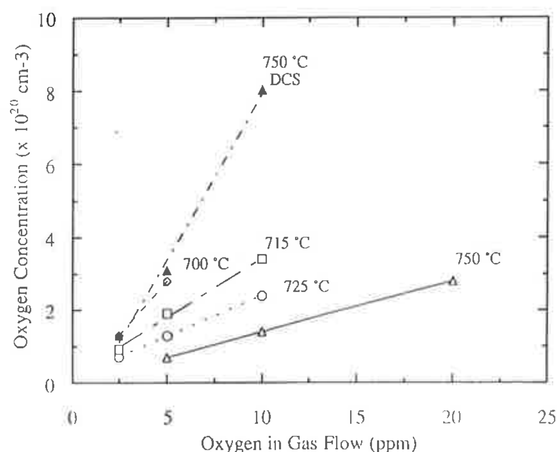

Fig. 3. Oxygen concentration of epitaxial silicon films as a function of oxygen contamination in the CVD feedstock gas. The source gas is silane unless dichlorosilane as indicated (DCS) [11].

The root of the higher gas-phase contaimination levels allowed in practice than those predicted by UHV experiments is the fact that the sticking coefficients in a CVD environment were lower. This fundamentally may be due to the hydrogen passivation on the silicon surface which is due to the overpressure of the hydrogen carrier. Although hydrogen will desorb from a silicon surface already at temperatures of 500 °C or less, having a hydrogen overpressure causes an equilibrium hydrogen coverage to result. This may be calculated from thermodynamic considerations [11] (Fig. 4). (The details of Fig. 4 differ from those in Ref. 11 because of a plotting error in Fig. 4 of Ref. 11). Note that at 700 °C, a hydrogen coverage of ~97% is predicted. While the exact details of oxygen (or water) absorption on silicon are not known, it may be expected that the adsorption of oxygen or water is far less likely on hydrogen-covered sites than at open sites. Thus the hydrogen coverage is in large part probably responsible for the reduction of oxygen/water sticking coefficients, and the fact that projections from UHV considerations are overly pessimistic for CVD growth requirements.

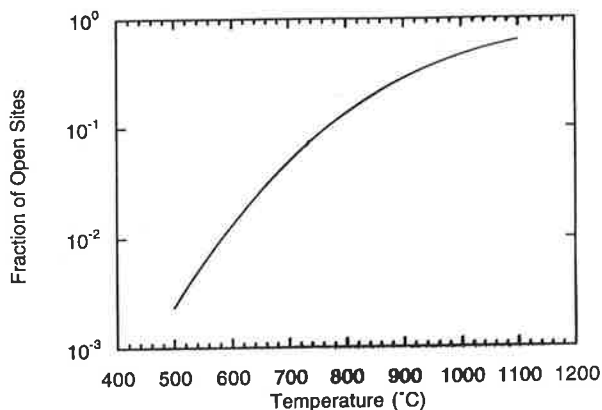

Fig. 4. Fraction of open sites (not covered by hydrogen) on a silicon surface as a function of temperature for a hydrogen pressure of 6 torr.

Chemical Vapor Deposition vs. Molecular Beam Epitaxy

Because MBE is a physical deposition process, growth rates are fairly independent of temperature, a substantial practical advantage compared to most low-temperature CVD processes. Furthermore, both Si and Ge have sticking coefficients near unity, independent of a Si or Ge surface. While there have been occasional reports of monolayer control by CVD for Si/Ge growth [12], the clear superiority of MBE for the growth of arbitrary structures on the monolayer scale is clear.

On the other hand, the energy of the incoming atoms or molecules in physical growth processes can substantially alter the quality of the resulting material. We have used

photoluminescence in $Si/Si_{1-x}Ge_x/Si$ heterostructures to probe the origin of differing luminescence in CVD and MBE samples, and ascribe the difference to such effects. High-quality Si/SiGe/Si quantum wells grown by CVD and free of oxygen contamination typically exhibit band-edge luminescence from the recombination of electrons and holes from the conduction and valence bands, respectively [13]. The emitted photon energy is near that of the bandgap. In some samples grown by MBE band-edge luminescence is observed. However, a deep luminescence is also frequently observed at an energy substantially below that of the bandgap (typically 100 meV) instead of or in addition to the band-edge luminescence in samples from many reactors [14,15]. We probed this difference by introducing radiation damage (by 50 keV Si^+ implantation) into otherwise high quality samples grown by RTCVD which originally exhibited only band-edge luminescence. After a 600 °C anneal, the implanted samples exhibited a deep luminescence similar to that observed in the MBE samples, and the original band-edge luminescence was no longer observed [16]. Fig. 5 shows how the deep luminescence tracks with the Ge fraction, showing that the deep luminescence originates in the SiGe region and not from the Si. The deep luminescence required only a very low dose (10^{10} cm^{-2}) of damage, and was nearly identical to that observed in MBE samples in terms of temperature dependence, pump power dependence, annealing behavior, etc.

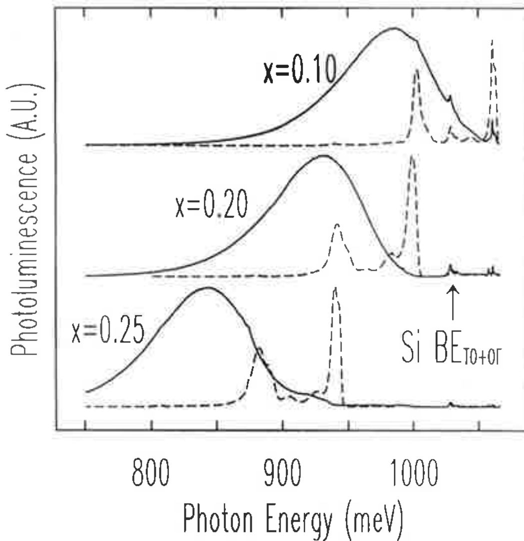

Fig. 5. Luminescence of $Si/Si_{1-x}Ge_x/Si$ for different approximate Ge fractions. Solid lines are for samples implanted with 50 keV Si^+ at 10^{11} cm^{-2}, and dashed lines received no implant. All were annealed at 600 °C.

Calculations of the implant damage profiles showed that the damaged region included both the Si cap and the SiGe regions. (The typical sample structure was a 10 nm quantum well followed by a 10 nm Si cap, and range of the damage was about 150 nm.) To further investigate the effect of the implant, a Si cap region of 0.3 μm was grown on top of a $Si_{0.7}Ge_{0.3}$ quantum well in a new sample, so that the extent of the direct implant damage would be far removed from the SiGe (Fig. 6). After implantation and annealing at 600 °C, however, the band-edge luminescence from the SiGe still disappeared and deep luminescence from the layer was observed (Fig. 7). This implies that a mobile defect created by the implant segregated and collected in the SiGe layers.

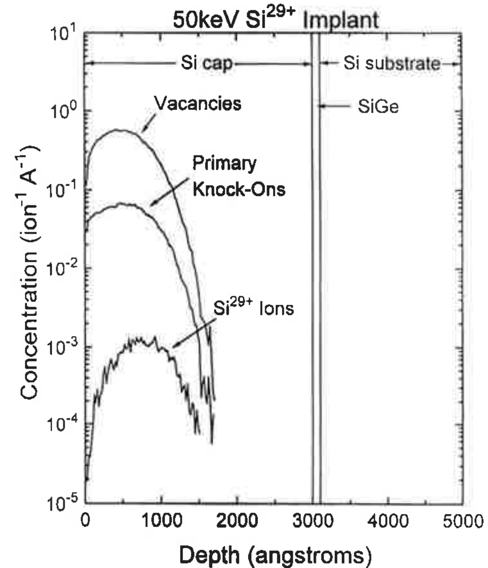

Fig. 6. Calculated damage profiles of a 50 keV Si^+ implant into a sample with a thick Si cap.

From the above evidence, we conclude that radiation damage is the source of the deep luminescence observed in some MBE samples. Such a damage is not inherent to MBE, since it is not observed in all chambers. Stray electron beam irradiation of the samples (from the electron beam evaporators) is probably of too low energy (~5 keV) to cause such damage. Rather, we proposed that the substrate may charge due to stray electron beams if not properly grounded, and that such a negative charge could attract evaporated Si atoms which were positively ionized by the e-beam evaporator [16]. Note that only very low doses (10^{10} – 10^{11} cm^{-2}), levels far less than one monolayer (10^{15} cm^{-2}), are required to see this effect. Strong evidence in support of this hypothesis was

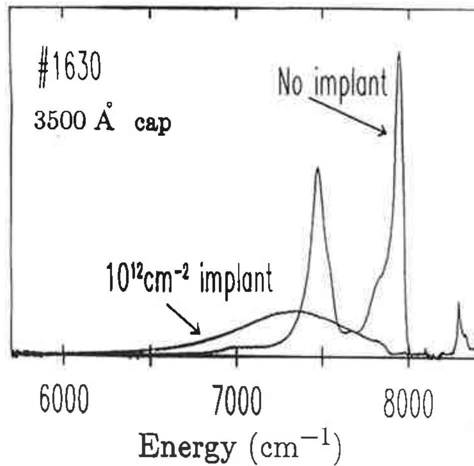

Fig. 7. Luminescence of a Si(300 nm)/$Si_{0.7}Ge_{0.3}$/Si quantum well after a 600°C anneal, both with and without a 10^{12} cm^{-2} 50 keV Si^+ implant.

recently presented from experiments in which the substrate voltage in MBE experiments was directly controlled. In the case of negative substrate bias, deep luminescence was indeed observed, but band-edge luminescence was observed when the sample was grounded [17].

$Si_{1-x-y}Ge_xC_y$ Alloys

For most applications, $Si_{1-x}Ge_x$ is grown commensurately strained on Si (100) substrates to avoid the formation of defects. The strain results in an enhanced reduction in bandgap as Ge is added, but also results in a maximum allowable thickness for the strained layer to be thermodynamically stable (known as the "critical thickness") [18]. This critical thickness imposes a severe constraint on the design of Si-based heterostructure devices. For example, a $Si_{0.8}Ge_{0.2}$ layer, which has a bandgap difference vs Si of 160 meV if commensurately strained on Si (100), has a critical thickness of only 15 nm. It has been known for several years that adding substitutional carbon to SiGe to form a ternary $Si_{1-x-y}Ge_xC_y$ layer reduces this strain because of the small size of the C atom. Layers have been reported by both MBE [19] and low temperature RTCVD [20]. Low temperature is required to suppress the precipitation of SiC. One substitutional C atom compensates the strain induced by 8 - 10 Ge atoms.

Using methylsilane as a carbon source, we have developed the growth of such $Si_{1-x-y}Ge_xC_y$ layers in our lab using a process similar to that of Ref. 20. The layers exhibit band-edge luminescence similar to that observed in $Si_{1-x}Ge_x$ layers, which allows us to measure the bandgap of the layers and determine the effect of the carbon [21, 22]. Adding carbon to pseudomorphic layers of $Si_{1-x}Ge_x$ on Si(100) is found to increase the bandgap at a rate of ~23 meV/%C (measured for up to 1% C). Transport measurements in heterojunction bipolar transistors give a similar result [23]. Unlike previous luminescence [24], our samples did not exhibit deep luminescence or dislocations luminescence, so that it is clear that our samples are fully strained and of high quality.

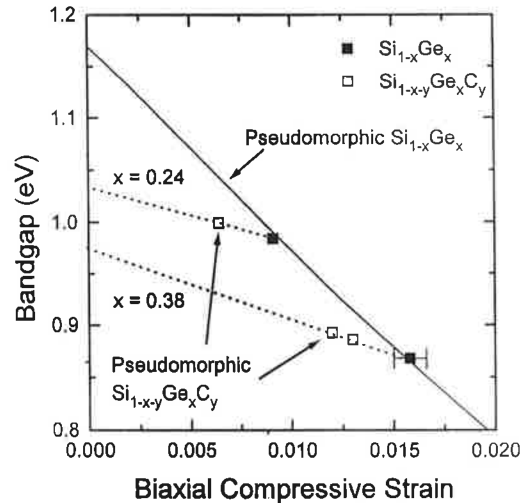

Fig. 8. Bandgap as a function of strain for pseudomorphic strained $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers.

Fig. 8 plots bandgap (measured by photoluminescence) vs strain (measured by X-ray diffraction) of $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers commensurately grown on Si (100). The solid line represents $Si_{1-x}Ge_x$. As C is added, the strain is reduced, and the bandgap increase is substantially less that that which would occur if the strain were reduced by simply reducing the Ge content (the solid line). Therefore, for a given bandgap, SiGeC layers will have a lower strain and an increased critical thickness compared to SiGe layers [20,22]. This is shown in Fig. 8, which plots the calculated critical thickness as a function of bandgap offset from Si, for $Si_{1-x-y}Ge_xC_y$ layers for different carbon fractions (y). Similar elastic properties for SiGe and SiGeC have been assumed, and the calculations are based on the effect of C on the strain and bandgap mentioned above. The lowest curve represents the usual $Si_{1-x}Ge_x$ limit. Adding 1% C, which has already been demonstrated by CVD to give very high quality layers, increases the critical thickness by 50% at an offset of 200 meV and by over a factor of two at an offset of 100 meV. For 2% C, which has been achieved structurally by CVD but not yet shown to be of high enough lifetime to luminesce, the

increases are 3 X and over 10 X, respectively. Cleary, SiGeC alloys will significantly increase the "design window" available to Si-based heterojunction device engineers beyond that available with SiGe alloys.

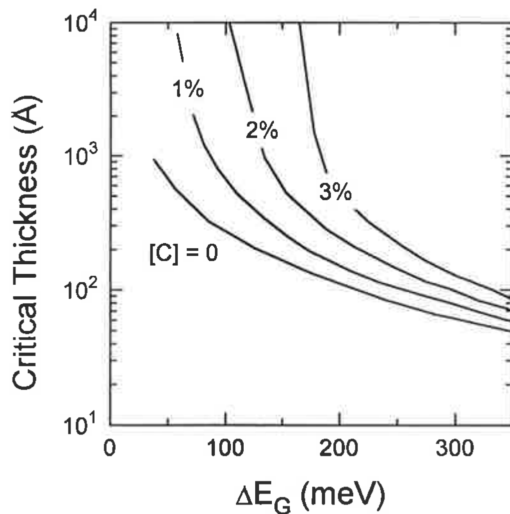

Fig. 9. Calculated critical thickness as a function of bandgap offset vs. Si of $Si_{1-x-y}Ge_xC_y$ layers for different carbon levels (y).

Summary

Rapid Thermal Chemical Vapor Deposition has been shown to be an attractive technique for the low-temperature epitaxial growth of silicon-based heterostructures. The technique has been applied to both $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers with high-quality device and material results in both material systems. Advantages of RTCVD for low-temperature epitaxy are the ability to rapidly change the sample temperature and the presence of a hydrogen surface layer. Disadvantages are the need for precise control of the wafer temperature across the entire substrate. Finally, $Si_{1-x-y}Ge_xC_y$ alloys should allow us to overcome the design limitations Si-based heterojunction device designers have faced for the past decade.

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