

## The Growth of $\beta$ -SiC on Si and Poly-Si on $\beta$ -SiC by Rapid Thermal Chemical Vapor Deposition

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### ABSTRACT

The growth properties of  $\beta$ -SiC on (100) Si grown by rapid thermal chemical vapor deposition, using a single precursor (methylsilane) without an initial surface carbonization step, were investigated. An optimum growth temperature at 800°C was found to grow single crystalline SiC. The single crystalline SiC films were used to be the buffer layers for the growth of subsequent poly Si films. For the poly Si grown at low temperature (625°C), the (110) Si diffraction was found to be the dominant peak in the X-ray diffraction spectra at the initial growth stage, while the poly Si grown on oxide was dominated by (111) texture. A small average misfit (4 %) between (110) Si planes and (100) SiC planes was proposed to explain this effect. To apply the Si/SiC/Si multilayers, SiC/Si heterojunction bipolar transistors (HBT's) were fabricated and compared to Si bipolar junction transistors.

### INTRODUCTION

Despite the success with Si/SiGe/Si heterojunction bipolar transistors(HBT's), there is still a strong desire for a widegap emitter material on Si. Such a widegap emitter on a Si base could yield devices with better high temperature performance than Si/SiGe HBT's (due to higher bandgap) and might be easier to be integrated[1]. Recently, the Si<sub>1-x</sub>C<sub>x</sub> alloys have been studied to serve this purpose[2]. However, only a small fraction of C ( $\leq 2\%$ ) can be incorporated into Si to form device quality materials and as a result, very limited band offset can be obtained. A large band offset can be used, if  $\beta$ -SiC (bandgap 2.2 eV)/Si heterostructures can be fabricated, despite of 20 % mismatch of lattice constants and 8 % mismatch of thermal expansion coefficients between  $\beta$ -SiC and Si. We, therefore, performed the Si/ $\beta$ -SiC heterostructural growth on (100) Si substrates by rapid thermal chemical vapor deposition, and applied this technology to fabricated Si/SiC HBT's.

### $\beta$ -SiC GROWTH on Si

The SiC films were deposited on tilted ( $4^\circ$  towards  $\langle 110 \rangle$ ) and non-tilted Si substrates (within  $1^\circ$  off) with a diameter of 100 mm by Rapid Thermal Chemical Vapor Deposition (RTCVD) at a growth temperature of 700–1100°C. The growth pressure was 1 torr with a 1.5 sccm methylsilane (SiCH<sub>3</sub>) flow and a 500 sccm hydrogen flow. The growth temperature(700-800°C) was accurately determined by the infrared transmission technique[3]. Growth temperatures higher than 800°C were controlled by the tungsten-halogen lamp power which was previously calibrated with a thermocouple welded onto a Si wafer. The SiC thickness was measured by fitting the optical reflection spectra from 500 to 700 nm with the SiC index of refraction of 2.6. The growth rate in the range 700–800°C varied exponentially with the inverse of temperature and the activation energy for this surface-reaction-limited growth was 3.6 eV. This is higher than that of pure silicon growth using silane as a precursor ( $\sim 1.7$  eV)[4] and may reflect the strong C–H bonding energy.

At a higher growth temperature (800–1100°C), the growth rate had a weak temperature dependence, indicating mass-transport-limited growth.

The crystallinity of the films was studied by XRD (X-ray diffraction) and TEM (transmission electron microscope). For the films grown at 750°C, the XRD spectrum of a 80nm film on non-tilted substrates exhibited a single crystalline feature with a broad unresolved  $\text{CuK}_{\alpha 1}$  and  $\text{CuK}_{\alpha 2}$  (400) peak (Full Width Half Maximum, FWHM, of  $2\theta$  is about  $1.6^\circ$ ). But the TEM diffraction pattern of the same sample showed evidence of some slightly in-plane rotated textures and very fine spots in the  $\langle 110 \rangle$  direction. This indicates the poor crystallinity of the 750 °C films. The crystallinity can be improved by increasing the growth temperature to 800°C. The XRD spectrum (Fig. 1) of a  $0.23 \mu\text{m}$  SiC film grown at 800 °C on non-tilted substrates showed that the FWHM of unresolved  $\text{CuK}_{\alpha}$  (400) peak was as small as  $0.75^\circ$ , which was similar to the value ( $0.65 - 0.7^\circ$ ) of  $0.3 \mu\text{m}$  commercial (100) SiC on Si[5], which was grown at a much higher temperature ( $\geq 1300^\circ\text{C}$ ). The TEM diffraction pattern also displayed a well-defined single crystalline feature. TEM also showed very high densities of stacking faults and dislocations, similar to the films of similar thickness grown by conventional high temperature growth techniques. The Fourier transform infrared spectra of a  $0.23 \mu\text{m}$  800°C grown film on non-tilted substrates displayed an absorption peak at  $796 \text{ cm}^{-1}$  (TO phonon absorption) with a FWHM of  $50 \text{ cm}^{-1}$ , which is similar to that of the film grown by conventional high temperature growth methods. The Raman spectrum of the same sample showed a broad peak at  $960 \text{ cm}^{-1}$  with FWHM of  $60 \text{ cm}^{-1}$  and a sharp peak  $510 \text{ cm}^{-1}$ . The  $510 \text{ cm}^{-1}$  peak is associated with the Si substrates, not SiC epilayers. The peak near  $960 \text{ cm}^{-1}$  is probably due to a combination of the LO phonon scattering ( $\sim 970 \text{ cm}^{-1}$ ) and interface defects between SiC and Si[6]. The XRD spectrum of the films grown at 1000 °C and 1100 °C, however, reveals extra (111) and (220) peaks, indicating the growth of polycrystalline material. Therefore, the 800 °C is the optimum growth temperature for the single crystalline  $\beta$ -SiC. The 800 °C-grown films were used to fabricated Schottky diodes with reverse breakdown voltage of 59 V[7].

## Poly-Si GROWTH on SiC

The poly Si films were deposited on the 800°C-grown SiC buffers at the temperature of 625 – 1000 °C at 6 torr using dichlorosilane(26 sccm) or silane(2 sccm) with hydrogen flow rate of 3 slpm. The same growth conditions on Si substrates yield to single crystalline Si layers. At high growth temperature (800 – 1000 °C), the (110), (111), and (311) textures of  $0.6 \mu\text{m}$  poly Si grown by dichlorosilane have been observed by XRD(Fig. 2), and the relative contents of (311) and (111) decrease as the growth temperature decreases, very similar to the poly Si growth on oxide with similar thickness[8]. For poly Si grown on oxide at low temperature ( $\leq 700 \text{ }^\circ\text{C}$ ), the  $0.6 \mu\text{m}$  poly Si film was dominated by (111) textures[8]. However, the poly Si with a thickness of  $0.1 \mu\text{m}$  grown at 625 °C on the SiC buffer using the silane precursor exhibits only (110) texture without diffraction peaks from other textures such as (111) and (311) in the XRD spectrum, but the (400) peak might be hidden behind the (400) Si peak of the substrate. The dominating diffraction of (110) texture in thin ploy Si on SiC can be understood by the small misfit of 4% (area average of two transverse direction) between (110) Si plane and (100) SiC plane as shown in Fig. 3, which makes it possible to grow single crystalline Si. However, due to the (100) Si substrate interference, the single crystalline growth of the epitaxial Si can not be confirmed. The poly grown Si

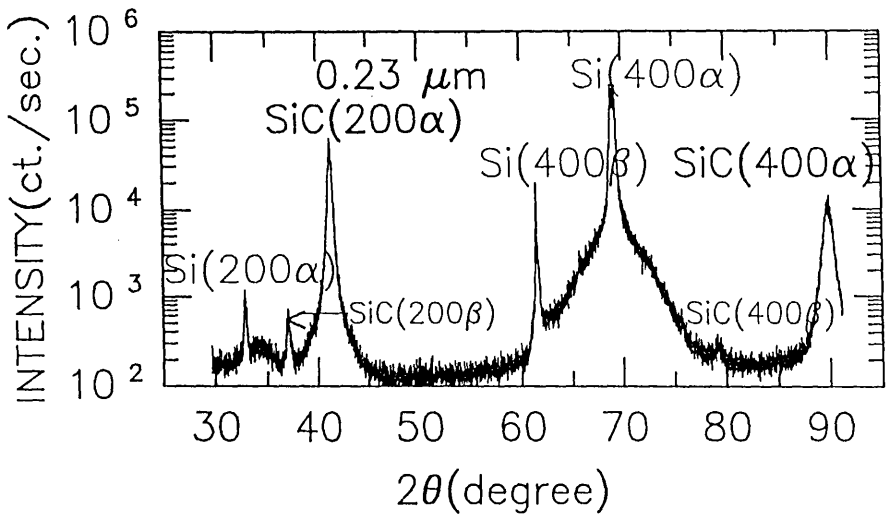


Fig. 1 The XRD spectrum of a 0.23  $\mu\text{m}$  single crystalline SiC film grown on (100) Si at 800 °C.

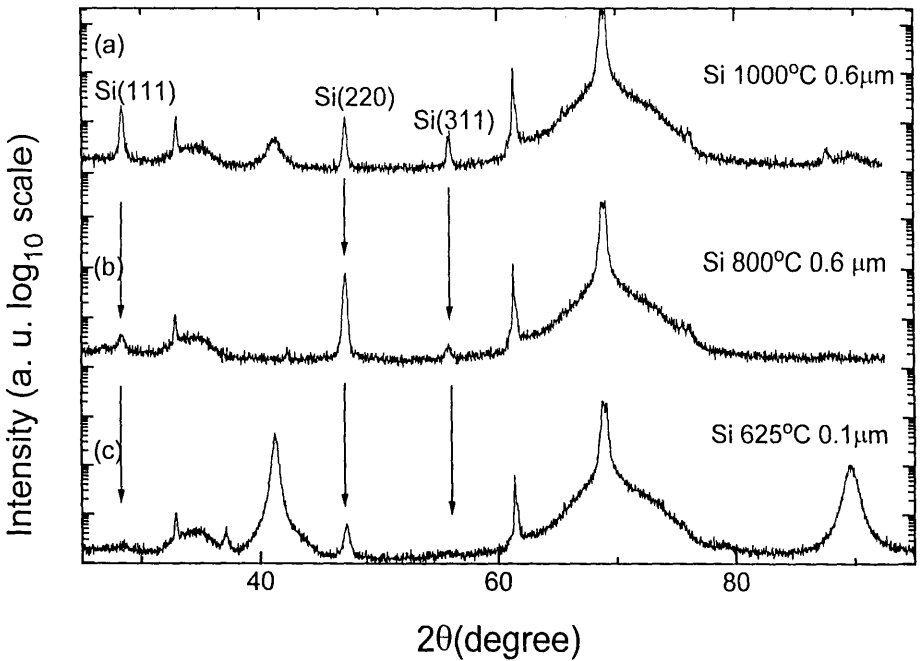


Fig. 2 The XRD spectra of poly Si films grown on (100) SiC at (a) 1000, (b) 800, and (c) 625 °C.

on SiC will be used as the ohmic contact material in SiC/Si HBT's.

## SiC/Si HETEROJUNCTION APPLICATIONS

A current gain of 800 has been obtained by Si/ $\beta$ -SiC HBT's grown by a special technique at 1000 °C on (111) Si substrates[9]. However, the high temperature process of 1000 °C would produce excessive back diffusion and prevent the integration with other Si devices. The single crystalline  $\beta$ -SiC grown at 800 °C on (100) Si substrates was used for the wide bandgap emitter material of Si/SiC HBT's. Fig. 4 displays the layer structures of a Si control device (Si bipolar junction transistors) and a SiC/Si HBT. In the SiC/Si HBT, there is an additional 2000 Å unintentionally doped SiC layer ( $n = 10^{18} \text{cm}^{-3}$ ) between the n-Si emitter and the  $n^+$ -Si emitter. The poly  $n^+$  Si emitter on the SiC layer grown at 800°C in the SiC/Si HBT structure was used to form better ohmic contacts than directly on SiC layers. The n-SiC emitter should block back-injected hole current (base current) ideally and thus should increase the current gain. The transistors were fabricated using a simple mesa process, which was detailed in [10]. The base contact was established by boron implant. Before base implantation, the emitter mesas were formed by plasma etching ( $\text{SF}_6$  for Si and 8% $\text{O}_2$  in  $\text{CF}_4$  for SiC). The devices were isolated by plasma-etched mesas and passivated with  $\text{SiO}_2$  deposited by plasma deposition at 350 °C. Before contact metallization, the wafers were given a RCA clean, and annealed at 700°C for 30 min in a forming gas. The emitter size was  $60\mu\text{m} \times 60\mu\text{m}$  for both HBT's and BJT's.

Fig. 5 shows the base current and collector current as a function of the emitter-base voltage (Gummel plot). The collector-base voltage is fixed at 2 V. The collector currents for both devices showed same voltage ( $V_{be}$ ) dependence with ideality factor of 1.0 and the same absolute magnitude. This result is expected, because both devices have the same base structures. The base currents also showed near-ideal behavior with ideality factors of 1.2 and 1.1 for Si BJT's and SiC/Si HBT's, respectively. However, the desired enhancement of current gain ( $I_c/I_b$ ) was not observed, because the base currents of SiC/Si HBT's was higher than thoses of Si BJT's. The increase of base currents in the SiC/Si HBT's, compared to the Si BJT's, was probably due to the interface defects between Si and SiC, which acted as recombination centers for back-injected holes and thus increased the hole currents, instead of being the barrier to stop the hole currents. Note also the apparent high series resistance of the HBT's. This is thought to result from the SiC layer in the emitter. Furthermore, the improvement in the ideality factor in the HBT's indicates that the excess base current is occurring in a neutral device region, and not in a space charge region or a device edge (surface). This is further evidence that the base current is occurring within the n-type emitter region. To reduce the defect density at the interface and to increase the current gain, a passivation technology of the interface will be desired in the future.

## SUMMARY AND ACKNOWLEDGMENTS

Si/ $\beta$ -SiC heterostructure has been grown at 800°C on Si. The growth temperature of 800 °C was optimum for single crystalline SiC layers on Si (100) substrates. The thin (0.1  $\mu\text{m}$ ) poly Si grown on SiC at 625°C has dominating (110) textures, in contrast to the growth on oxide, where (111) textures dominate. The SiC/Si HBT's has been fabricated,

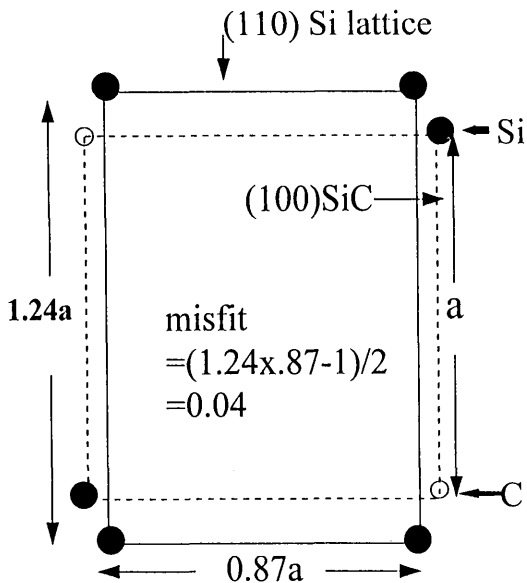


Fig. 3 The schematic illustration of Si (110) lattice plane and SiC (100) lattice plane. The average misfit is about 4 %.

### Si BJT

$n^+(10^{18}\text{cm}^{-3})$	- Si emitter	$\sim 2000 \text{ \AA}$	(800 °C)
$n(10^{17}\text{cm}^{-3})$	- Si emitter	$\sim 3000 \text{ \AA}$	(800 °C)
$p^+(10^{19}\text{cm}^{-3})$	- Si base	$\sim 600 \text{ \AA}$	(700 °C)
$n(10^{17}\text{cm}^{-3})$	- Si collector	$\sim 3000 \text{ \AA}$	(800 °C)
$n^+(10^{19}\text{cm}^{-3})$	- Si collector	$\sim 2\mu\text{m}$	(1000 °C)

Fig. 4 Layer structures of a Si bipolar transistors and a SiC/Si HBT. There is an additional SiC layer between the n-Si emitter and the  $n^+$ -poly Si emitter in the SiC/Si HBT.

< 100 > non-tilted n Si substrates

### SiC/ Si HBT

$n^+(10^{18}\text{cm}^{-3})$	- Si emitter	$\sim 2000 \text{ \AA}$	(800 °C)
$n^+(10^{18}\text{cm}^{-3})$	- SiC emitter	$\sim 2000 \text{ \AA}$	(800 °C)
$n(10^{17}\text{cm}^{-3})$	- Si emitter	$\sim 3000 \text{ \AA}$	(800 °C)
$p^+(10^{19}\text{cm}^{-3})$	- Si base	$\sim 600 \text{ \AA}$	(700 °C)
$n(10^{17}\text{cm}^{-3})$	- Si collector	$\sim 3000 \text{ \AA}$	(800 °C)
$n^+(10^{19}\text{cm}^{-3})$	- Si collector	$\sim 2\mu\text{m}$	(1000 °C)

< 100 > non-tilted n Si substrates

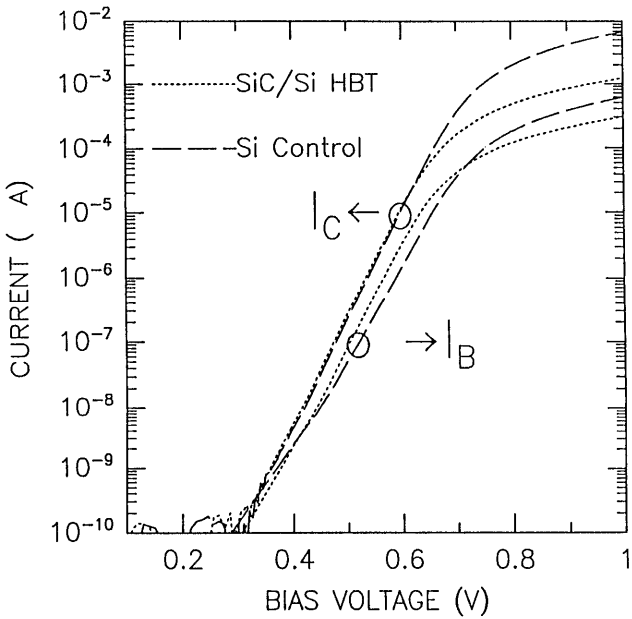


Fig. 5 The Gummel plots of a SiC/Si HBT and a Si control device.

but the density of interface defects should be further reduced for desired SiC/Si HBT performance. The TEM assistance of Dr. E.A. Fitzgerald of AT&T Bell Labs, and Prof. P. Pirouz and Dr. J. W. Yang of Case Western Reserve University are gratefully appreciated. The support of the US office of Naval Research (N000121-90-J-1316) is gratefully acknowledged. One of the authors (C. W. Liu) would like to thank the support of National Science Council of ROC (NSC 86-2221-E-002-089).

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