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# **Defects and Diffusion in Silicon Processing**

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## Suppression of Boron Transient Enhanced Diffusion in SiGe HBTs by Carbon Incorporation

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### ABSTRACT

In this paper we demonstrate, using both SIMS and transistor electrical characteristics, that substitutional carbon fractions of 0.5% in heavily doped  $\text{Si}_{0.8}\text{Ge}_{0.2}$  base heterojunction bipolar transistors (HBTs) reduce both thermal diffusion and transient enhanced diffusion (TED) of boron. Furthermore we show that carbon suppresses TED of boron in carbon-free regions that surround the carbon layers.

### INTRODUCTION

The outdiffusion of boron from heavily doped npn SiGe base HBTs is a severe limit to device integration. This outdiffusion, which degrades  $\beta$ ,  $V_A$ , and  $f_T$  [1-4], may be caused by high temperature processes and is particularly enhanced following arsenic implantation that is used to contact a lightly doped single crystalline emitter [1]. While SIMS may be used to detect outdiffusion of boron from SiGe bases, changes in the electrical characteristics of devices are a far more sensitive tool with which to probe boron diffusion. In this paper, we use both the electrical characteristics of transistors as well as SIMS to measure the effects of substitutional carbon on boron diffusion following a thermal anneal used to simulate a high temperature postgrowth process and following an arsenic emitter implant and activation anneal used to simulate an n+ emitter contact.

### EXPERIMENT

The epi-layers were grown by rapid thermal chemical vapor deposition using methylsilane as the carbon source. Following a 1  $\mu\text{m}$  thick buffer layer doped  $10^{18} \text{ cm}^{-3}$  with phosphine, a 2000  $\text{\AA}$   $\sim 10^{17} \text{ cm}^{-3}$  n-type collector was grown at 1000°C. The 20% Ge base was grown at 625°C with 50  $\text{\AA}$  undoped spacer layers on either side of the 50-200  $\text{\AA}$ ,  $10^{20} \text{ cm}^{-3}$  boron doped base. Substitutional carbon fractions of 0.5% as measured by X-Ray were incorporated in  $\text{Si}_{0.8}\text{Ge}_{0.2}$  by injecting methylsilane together with germane [5]. SIMS measurements show that these carbon levels have no significant effect on  $\text{Si}_{1-x}\text{Ge}_x$  growth rate. Following the base, the 3000  $\text{\AA}$  n-type emitter was grown at 700°C for 1 hour doped  $10^{19} \text{ cm}^{-3}$  with phosphine.

Transistors were fabricated using a zero thermal budget, double mesa process [6] in order to eliminate possible dopant diffusion as well as carbon precipitation during transistor fabrication. Therefore, in the absence of any post-growth thermal processing, the transistor characteristics correspond identically to that of the as-grown layers. This process gives the ideal collector currents (60 mV/decade) necessary to analyze electron transport across the base, but is not manufacturable due to non-ideal base currents generated by the unpassivated surfaces. Such base currents are not relevant for this work, however.

Figures 1a and 1b show transistor characteristics of as-grown  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and  $\text{Si}_{0.795}\text{Ge}_{0.2}\text{C}_{0.005}$  transistors. The absence of collector saturation current dependence on  $V_{\text{BC}}$  (equivalently, the high Early voltages) is due to both the high doping in the bases and the absence of barriers caused by boron outdiffusion from the base into the collector. If some boron had diffused into the collector, however, turning the formerly n-type Si collector p-type, a barrier would have been formed at the base collector junction because of the difference in bandgap between Si and  $\text{Si}_{0.8}\text{Ge}_{0.2}$ . Increasing  $V_{\text{BC}}$  reduces the height of this barrier leading to increased collector current, or equivalently, a decreased Early voltage. This barrier may be caused by postgrowth processing steps or by too narrow undoped spacer layers surrounding the doped SiGe [4].

Figure 1c shows electrical characteristics of a transistor identical to that of Figure 1a with the exception that it has  $\sim 25 \text{ \AA}$  undoped spacer thicknesses. In contrast to the transistor from Figure 1a, increasing  $V_{\text{BC}}$  to 1V increases the collector saturation current by a factor of 2.2 which results in the low Early voltage. While the diffusion of boron is identical in both transistors, the boron in the transistor from Figure 1c moved into the Si collector beyond the undoped SiGe spacer. This results in the low transistor Early voltages. This data shows the power of electrical techniques to probe boron movements at a far more sensitive scale than observable by SIMS.

To measure the effect of substitutional carbon on boron diffusion in sub-critical thickness  $\text{Si}_{0.8}\text{Ge}_{0.2}$  bases (150  $\text{\AA}$  total thickness, to avoid misfit dislocations), pieces of the as-grown wafers were annealed (15 min. in  $\text{N}_2$ ) at temperatures up to 890 $^\circ\text{C}$  and transistors were fabricated. One might expect that at a certain annealing temperature, the boron will diffuse outside the SiGe, resulting in decreased collector saturation currents due to barrier formation. Figure 2 shows collector currents as a function of temperature for both no-carbon and carbon devices. For a thermal anneal of 855 $^\circ\text{C}$ ,  $I_{\text{C}}$  drops by a factor of 25, whereas the SiGeC collector currents are identical to that of the as-grown devices. Only after annealing at temperatures above 855 $^\circ\text{C}$  does the SiGeC transistor collector saturation current deviate from the as-grown value. Since the carbon transistors have the ability to withstand a higher temperature anneal than that of SiGe, we may conclude that substitutional carbon in SiGe reduces the thermal diffusion of boron, since the undoped spacer layer thicknesses are identical in both transistors.

Figure 3 compares SIMS of as-grown SiGeC and SiGe HBT layers to that of the 855 $^\circ\text{C}$  annealed wafers. For this annealing condition, outdiffusion in SiGe is expected from Figure 2a but is not expected in SiGeC. This is not readily apparent from the SIMS profiles in Figure 3b except

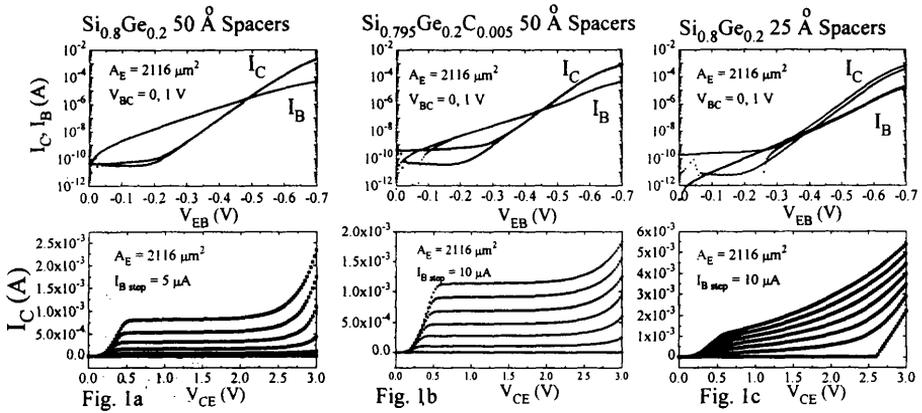


Fig. 1 Transistor characteristics of as-grown devices

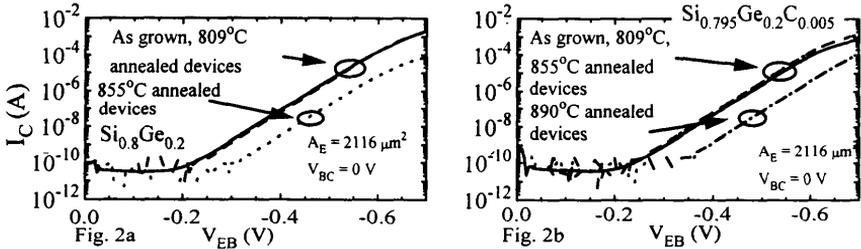


Fig. 2 Collector currents of annealed wafers

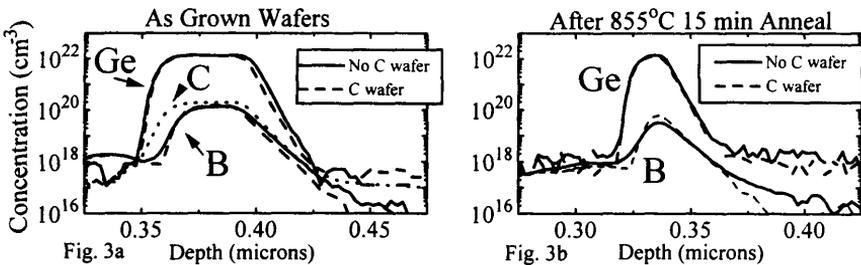


Fig. 3 SIMS of as-grown and annealed wafers

for the decrease in factor of  $\sim 2$  in boron peaks and the slightly wider boron profile in SiGe compared to that of SiGeC. These differences are not present in as-grown layers with 300 Å bases, as shown in Figure 3a. Thus SIMS also suggests that boron diffusion is reduced in SiGeC. This difficulty of resolving boron profiles of the order of 50 Å highlights the usefulness of electrical techniques for probing boron movement.

Shallow arsenic emitter implants to contact lightly doped crystalline silicon emitters of heavily doped SiGe base HBTs should be advantageous for device integration. Although the implant range is only  $\sim 1000$  Å deep, mobile damage migrates through the 3000 Å emitter to the base during the activation anneal, drastically increasing boron diffusion [1]. This effect is known as transient enhanced diffusion (TED). To examine the effects of carbon on boron TED in SiGe caused by arsenic emitter implantation, pieces of the as-grown wafers were implanted with arsenic ( $1.5 \times 10^{15} \text{ cm}^{-2}$ , 30 keV;  $3 \times 10^{14} \text{ cm}^{-2}$ , 15 keV; chosen to follow [7]) and annealed at 647°C prior to device fabrication. Figure 4 shows electrical characteristics of SiGe and SiGeC transistors fabricated following arsenic implantation and 647°C anneal. The high Early voltage of the carbon transistor compared with that of the no-carbon transistor implies that carbon in SiGe reduces TED of boron. Figure 5 shows SIMS of wafers following implantation and 755°C anneal which confirms the electrical predictions.

Device layers were also grown in which the doped 100 Å SiGeC layers were surrounded on both sides by  $10^{20} \text{ cm}^{-3}$  boron doped 50 Å SiGe layers (*no carbon*), which, in turn, were surrounded by undoped 50 Å SiGe spacers. SIMS of such a "sandwich" structure (Figure 6a) clearly shows the as-grown boron layers outside of the carbon layer, in contrast to Figure 3a which shows boron inside the carbon layers. One might expect boron TED to occur in these structures following implantation and anneal since carbon does not exist at the edge of the p-type base, as shown in Figure 6a. However, electrical characteristics of transistors fabricated following arsenic implant and 742°C anneal (Figure 7), show high Early voltages indicating that no boron outdiffusion has occurred. SIMS following arsenic implantation and 755°C anneal, shown in Figure 6b, supports the electrical evidence that the boron outside the carbon layers has not experienced TED.

From the sandwich base transistor results we may conclude that substitutional carbon in SiGe reduces TED of boron not only in itself but also in nearby carbon-free areas. Since TED is caused by mobile point defects generated by implantation damage, we may conclude that carbon in SiGe is a point defect sink which reduces the concentration of interstitials in nearby carbon-free areas. This in turn suppresses TED of boron in those areas. Previous work on carbon in Si has shown that substitutional carbon atoms tie up Si interstitials by forming  $\text{SiC}_x$  complexes [8]. Our work suggests that a similar process occurs in SiGeC. TEM micrographs (not shown here) of SiGeC bases following implantation and anneal show that these complexes must be smaller than 20 Å in size, however. While it has been shown using SIMS that  $2 \times 10^{19} \text{ cm}^{-3}$  carbon levels in Si reduce TED in  $2 \times 10^{19} \text{ cm}^{-3}$  boron-doped superlattices following Si implant and 790°C, 10 min.

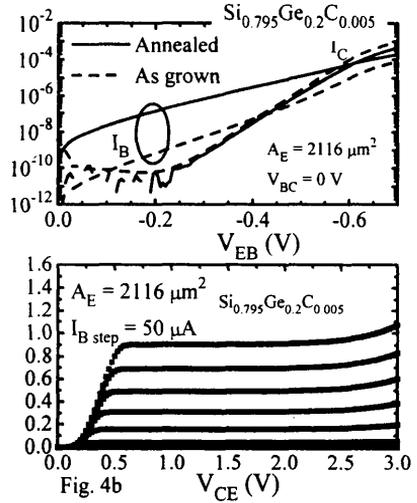
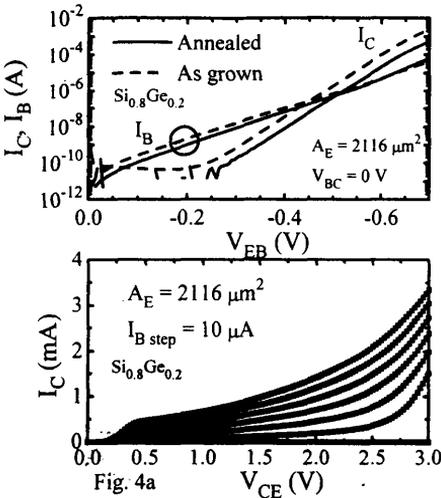


Fig. 4 Collector currents of wafers following arsenic implantation, 647°C anneal

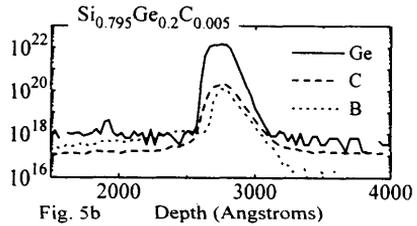
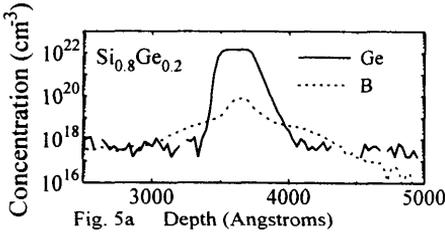


Fig. 5 SIMS following arsenic implant and 755°C anneal

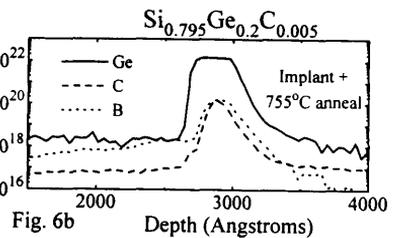
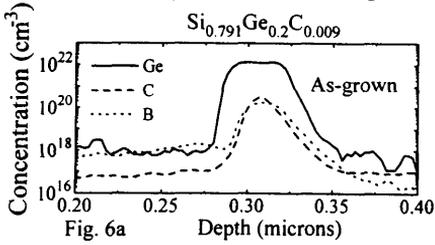


Fig. 6 SIMS of as-grown and arsenic implanted, 755°C annealed sandwich bases

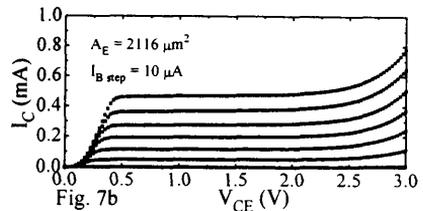
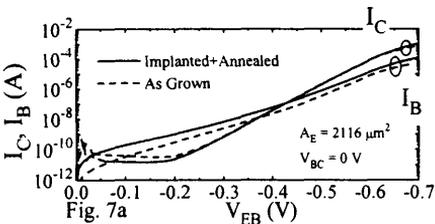


Fig. 7 Transistor characteristics of sandwich bases following arsenic implant, 742°C anneal

anneal [9], neither electrical measurements nor the reduction of boron TED outside the carbon doped layers have been previously reported.

In conclusion, we have demonstrated that substitutional carbon can reduce TED of boron in heavily doped SiGe bases. These results may find future application in SiGe HBT device integration.

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