10:40 AM, P7

Growth and In Situ Ellipsometric Analysis of $Si_{1-x}Ge_x$ Alloys Deposited by Chemical Beam Epitaxy: P. BOUCAUD[a], F. Glowacki[b], Y. Campidelli[b], F. Ferrieu[b] and D. Bensahel[b] a) IBG Universitc Paris XI - Bai 220, 91405 Orsay, France b) CNET-CNS, Chemin du vieux chene, 38243 Meylan France *on leave from ISA-RIBER

The deposition of $Se_{1-x}Ge_x$ strained layers or Si_mGe_n atomic layer superlattices is of considerable interest for its application to novel optoelectronic devices compatible with standard silicon signal processing. In this context, chemical beam epitaxy (CBE) of hydrides like silane and germane is a growth process which presents numerous advantages over standard CVD or MBE. In this communication, we present a detailed study of the growth kinetics by CBE along with its monitoring by in and ex situ ellipsometry.

Good uniformity as well as selectivity on SiO_2 patterned substrates are easily achieved using this technique for x values varying between 0 and 25%. The incorporation rate of germanium and the growth kinetics of $Si_{1-x}Ge_x$ strained layers are analyzed as a function of the hydride gas flows and substrate temperature. At 700°C a decrease of the alloy growth rate is observed for germanium composition lower than 5% followed by a quasi-linear increase. The reported features will be analyzed by the help of a model involving the main surface reactions.

The in situ ellipsometric analysis of the growth process is investigated at different wavelengths. Results on the silicon homoepitaxy and alloy heteroepitaxy of bulk or multiquantum wells structures will be presented. These characterizations are completed and interpreted with a spectroscopic ellipsometry measurements at room or growth temperature.

11:00 AM P8+

Structural and Electrical Characteristics of Low-Temperature Cubic SiC on (100) Si: C. W. LIU, J. C. Sturm and E. A. Fitzgerald* Dept. of Electrical Engineering, Princeton University, Princeton, NJ 08544, *At&T Bell Laboratories, Murray Hill, NJ 07974

The unique thermal and electronic properties of SiC make it a promising material for electronic and optoelectronic devices designed to operate in severe conditions. Conventionally, high growth temperatures (~ 1300°C) are required for chemical vapor deposition growth, which prevents the possibility of integration with or into silicon-based devices. Furthermore, the low material quality is reflected in very leaky Schottky barriers with a highest reported soft breakdown of 8 - 10 V. In this paper, we report the structural and electrical characteristics of cubic SiC on (100) Si grown at temperature as low as 700°C using a single gas precursor.[1]

The SiC films were deposited on 4 in. Si (100) substrates (not tilted) by Rapid Thermal Chemical Deposition at growth temperatures of 700 - 1100°C. The growth pressure is 1 torr with 1.5 sccm methylsilane flow and 500 sccm hydrogen flow. The crystal structure was investigated by X-ray diffraction (XRD), electron channeling patterns (ECP), and transmission electron microscope (TEM). XRD (FWHM of 2θ = 0.75° for (400) diffraction), TEM diffraction patterns and ECP (clear (400) and (220) bands) all showed a 800°C sample of thickness of 300 nm to be single crystal. Although XRD indicated single crystal growth (FWHM = 1.6°) of 750° films of thickness of 80 nm, TEM diffraction showed evidence of some slightly in-plane-rotated cystallites. On the other hand, he XRD spectra of films grown at 1000°C and 1100°C consisted of extra (111) and (220) peaks, indicating the growth of polycrystalline material. However, "two step growth", namely, a thin layer grown at 800°C first, then followed by high temperature growth, yielded single-crystalline films again. This shows that a low growth temperature (800°C) of the initial SiC layer is required for single-crystlaline films, in contrast to what is often observed in conventional growth techniques.

Schottky diodes using Al contacts were fabricated on boron-compensated n-type SiC grown at 800°C. The reverse I-V characteristics exhibit a hard breakdown, with breakdown voltage exceeding 13 V. This is the first time that sharp breakdown has been observed and to the best knowledge of the authors, represents the highest breakdown voltage reported to date for cubic SiC grown on Si under any conditions. The support of ONR (N00014-90-J-1316) is gratefully acknowledged.

1. I. Golecki, F. Reidinger and J. Marti, Appl. Phys. Letter 60, 1703 (1992).

11:20 AM, P9

Properties of Deep Level Defects in Epitaxial $Si_{1-x}Ge_x$ Layers: K. NAUKA and T. I. Kamins Hewlett-Packard Company, Palo Alto, CA 94304

Deep level transient spectroscopy was employed to investigate properties of deep states related to intentionally introduced metallic (Au) and non-metallic (N) impurities in $Si_{1-x}Ge_x$ epitaxial layers grown on Si substrates. The strained and partially relaxed $Si_{1-x}Ge_x$ epitaxial layers were deposited using CVD at 625 - 7000°C. Their thicknesses were between 150 nm and 500 nm, and Ge content varied from x = 0 to x = 0.25. N was introduced by conducting the epitaxial process in a N-containing atmosphere; Au was diffused by rapid thermal annealing with Au source in contact with the $Si_{1-x}Ge_x$ layer.

Au introduced deep donor and acceptor levels corresponding to different charge states of the substitutional Au and Au complex related hole trap. Their respective activation energies in Si were: 0.49 eV, 0.28 eV, and 0.52 eV. Both the activation energies and capture cross sections depended on the Ge content and degree of relaxation. Investigating layers with fixed Ge content and various degrees of relaxation related the activation energies to the strain, allowing calculation of deep level spectra in the layers with Si-like band structure and any degree of relaxation.

N in $Si_{1-x}Ge_x$ introduced three electron traps with activation energies between 0.51 eV and 0.20 eV. Their concentrations were in the range $4x10^{14}$ - $1x10^{15}$ cm^{-3}. No N-related deep states have been seen in a Si epitaxial layer grown in a similar N-containing ambient. N incorporation has been considered as a means of increasing mechanical strength of strained $Si_{1-x}Ge_x$, and deep donors associated with N could have a deleterious effect on the performance of N-doped $Si_{1-x}Ge_x$-based devices.

11:40 AM, P10

Contacts to Si/SiGe Heterostructures: S. F. NELSON, T. N. Jackson[1] IBM Research Division, T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598, [1]The Pennsylvania State University, Center for Electronic Materials and Processing, University Park, PA 16802

Si/SiGe heterostructures with strained Si channels are of interest because the strain results in a conduction band offset that allows the Si channel to form a quantum well, which can be used for high-mobility modulation doped structures. To date, Si/SiGe heterostructures with 2-dimensional electron mobility over 173000 cm^2/V s at low temperature[1] have been studied, and n-channel Si/SiGe MESFETs with large transconductance have been fabricated[2].

However, little has been published about contracts to Si/SiGe heterostructures. Au/Sb has commonly been used for material evaluation contacts, but such contacts are often unreliable at low temperature or under high magnetic field, and are not suitable for high performance devices since the eutectic temperature between Au and Si/SiGe is low and contact resistance is large after low temperature contact anneals.

We have investigated two alternative approaches to Si/SiGe contacts. The first technique uses Ag/Sb as a replacement for Au/Sb. Although we have not determined the eutectic temperature between Ag and the Si/SiGe compositions we typically use, the Ag eutectic to elemental Ge is 651° C and the eutectic to Si is larger still. This allows Ag/Sb contacts to be alloyed at temperatures large enough to form stable, low-resistance contacts. We have found that thin layers of Sb (1-5 nm) with Ag cover layers (50-100 nm) alloyed at 400° C for a few minutes will form useful contacts.

Although Ag/Sb contacts are simple and fairly reliable, such contacts may not be suitable for high-performance devices. We have investigated contacts formed by ion-implantation and annealing, since such techniques may be more compatible with typical device fabrication. By implanting P and annealing at temperatures high enough to get useful activation, but not large enough to cause dopant movement in our modulation doped structures, we have been able to make stable, reliable