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High Hole Mobility p-channel MOSFET's Using MOS-gated $Si/Si_{1-x}Ge_x$ Heterostructures

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Through the use of strained $Si_{1-x}Ge_x$ buried-channel structures grown by Rapid Thermal Chemical Vapor Deposition, high mobility p-channel MOSFET's have been successfully fabricated and demonstrated. A room-temperature mobility enhancement of 50% and a low-temperature (90 K) enhancement of 100% have been observed compared to conventional all-silicon enhancement mode structures without any degradation in subthreshold slope.

Introduction

CMOS integrated circuits are in large part limited by the low mobility of holes in p-channel devices. For gates with symmetrical electrical characteristics, the p-MOS devices must have widths 2-3 times larger than the n-channel devices, leading to excessive input capacitance. It has been proposed[1-3], that confining holes to a thin $Si_{1-x}Ge_x$ strained layer, separated from the oxide gate by a thin silicon spacer, would improve the hole mobility because of the lower effective mass in the $Si_{1-x}Ge_x$ and because the holes are moved away from scattering sites at the $Si\text{-}SiO_2$ interface. That holes could indeed be confined to such $Si_{1-x}Ge_x$ layers and gated was confirmed by C-V[2,3] and Hall[3] measurements. In this paper we present the first clear evidence of substantial mobility enhancement in such structures. Improvements of up to 50% are seen over a wide range of gate voltages compared to conventional all-silicon devices at room temperature. Excellent uniformity and a larger improvement at lower temperatures are also reported.

A typical band diagram of the device for various gate voltages is shown in Fig. 1. Because of the large valence band offset, inversion is first reached in the $Si_{1-x}Ge_x$ layer for a properly designed structure. At very large gate voltages, however, inversion will occur at the Si/SiO_2 interface. The devices were formed by growing the $Si/Si_{1-x}Ge_x/Si$ layers by Rapid Thermal Chemical Vapor Deposition (RTCVD)[4] on epitaxial silicon layers on silicon substrates. The silicon growth temperature of 700 °C and the $Si_{1-x}Ge_x$ growth temperatures of 600-625 °C were controlled by the infrared transmission technique [5]. The three experimental structures had germanium fractions and silicon cap thicknesses of x=0.3, t_{Si}=105Å ; x=0.2, t_{Si}=75Å , and x=0.4, t_{Si}=75Å . The $Si_{1-x}Ge_x$ strained layer thicknesses were ~100Å in all cases, with the result that the x=0.2 and x=0.3 layers were near or below the equilibrium critical thickness for commensurate growth, while the x=0.4 device was substantially (~2X in thickness) beyond this limit. All-silicon control devices were fabricated in similarly doped n-type silicon substrates for comparison. A plasma-CVD gate oxide (t_{ox}=125Å) and a non-self-aligned metal gate process were used. The source-drain implant anneal was performed at 700 °C for 30 minutes.

Results and Discussion

Well-behaved device characteristics were obtained in all cases. The room temperature drain conductance of long-channel (100 μm) $Si_{1-x}Ge_x$ devices were larger than the silicon control devices by a factor up to 25% in the x=0.2 and 50% in the x=0.3 device over a wide range of gate voltages at room temperature (Fig. 2), indicating a commensurate increase in the effective hole mobility. This is the first time that this result has been conclusively demonstrated. In Fig. 3 the effective hole mobility vs. effective

vertical field of the $Si_{0.7}Ge_{0.3}$ device is compared to the silicon control of our experiment and the ideal silicon data of Watt and Plummer[6]. A factor of $\eta=1/3$ was used in calculating the contribution of the hole charge to the effective vertical field, and the simple gate oxide capacitance was used to relate the gate voltage to the hole charge in all strucutures. Note that the increase in mobility occurs not just at low gate voltages, but over a wide range of effective vertical field. Our silicon control device has a mobility less than that of Ref. 6, which is consistent with the large interfacial fixed charge in our deposited oxide of 8×10^{11} cm^{-2}. In spite of this large fixed charge, the $Si_{0.7}Ge_{0.3}$ device still had an effective mobility which was 15-20% larger than the Watt and Plummer silicon result over the entire range. Even higher mobilities would be expected in the $Si_{1-x}Ge_x$ devices with a high quality gate oxide. The subthreshold characteristics of the $Si_{1-x}Ge_x$ and Si devices were nearly identical, with a slope of 110 mV/decade (Fig. 4). This indicates a low interface state density at the $Si/Si_{1-x}Ge_x$ interface and hence a low defect density in the strained layers. The results were very consistent from device to device as shown in a mobility histogram in Fig. 5. At present it is not known if the performance of the x=0.3 device was better than the x=0.2 device due to the increased amount of germanium or due the thicker Si cap layer. This is under further investigation.

At 90K the peak hole mobility in the $Si_{0.7}Ge_{0.3}$ devices increases to $780 cm^2/V{\cdot}s$ and is roughly twice as large as that in that of the virgin silicon control device (Fig. 6) (compared to a 50% improvement at room temperature). The increase in effective mobility from room temperature to low temperature is monotonic, and is consistent with the reduction in phonon scattering at low temperatures. The decrease in phonon scattering will make surface scattering more significant so that an improved performance in the $Si_{1-x}Ge_x$ device relative to the silicon device is expected.

In contrast to the other two devices, the $Si_{0.6}Ge_{0.4}$ device had a mobility which was substantially worse (less than half) of the control device. Furthermore, the subthreshold slope of this device was also substantially degraded, indicating the presence of excessive interface states. Since the $Si_{1-x}Ge_x$ layer in this device is well over the equilibrium critical thickness limit, it is assumed that misfit dislocations at the $Si/Si_{1-x}Ge_x$ interfaces caused the device degradation (Fig. 7).

Summary

In summary, RTCVD has been used to demonstrate that confining holes to a $Si_{1-x}Ge_x$ layer below the surface of a MOS gate on silicon substrates leads to substantially improved hole mobilities. Enhancements compared to silicon devices of up to 50% at room temperature and 100% at 90K for hole densities to 4×10^{12} cm^{-2} have been shown. Misfit dislocations must be avoided for optimum device performance. The support of NSF (ECS8615) and DOE (DE-AC02-76-CH03073) is gratefully appreciated.

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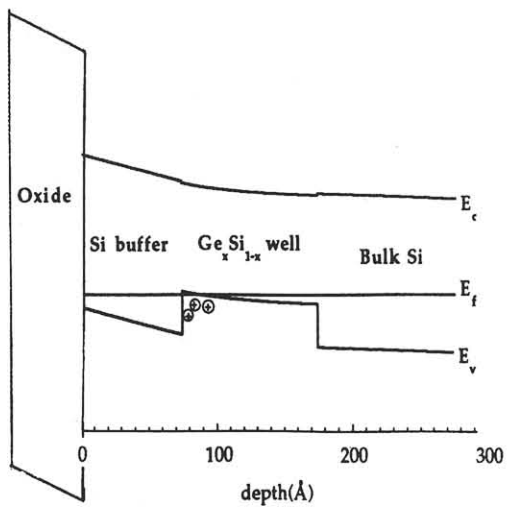

Fig. 1. Band diagram of $Si_{1-x}Ge_x/Si$ MOSFET in inversion.

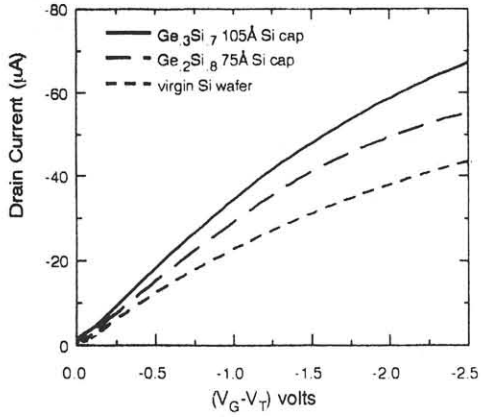

Fig. 2. Drain current vs. gate voltage for several devices at room temperature (V_{DS} = 0.1V, W/L = 314 μm/97 μm).

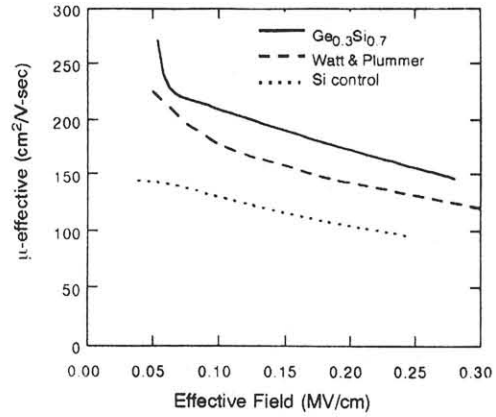

Fig. 3. Effective room-temperature mobility vs. effective vertical field data (η = 0.33) compared to that of Watt and Plummer [6].

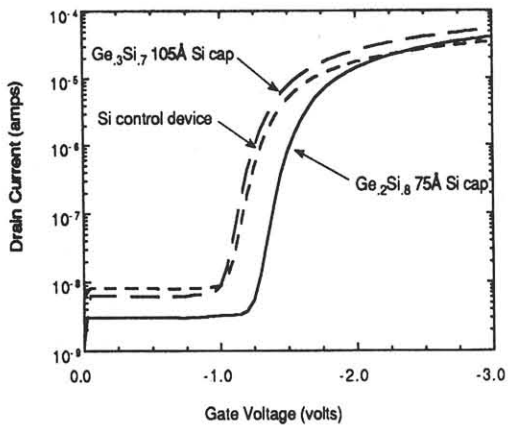

Fig. 4. Subthreshold current of the devices in fig. 2. The large leakage currents are due to the room light and the large junction area of $\sim 10^4$ μm^2.

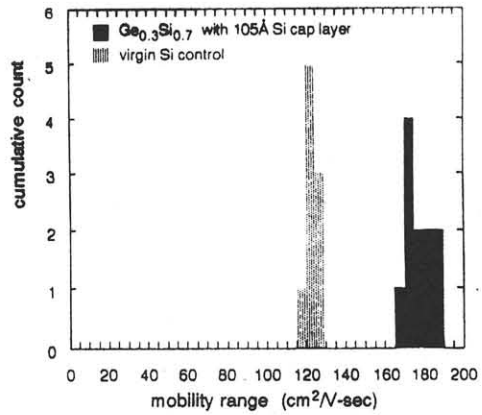

Fig. 5. Histogram of effective mobility at V_G - V_T = -1V for $Si_{0.7}Ge_{0.3}$ and all-silicon devices at room temperature indicating device uniformity.

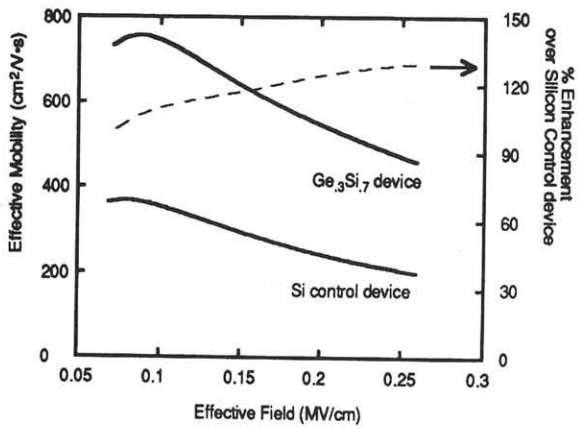

Fig. 6. Effective mobility vs. vertical field at 90K

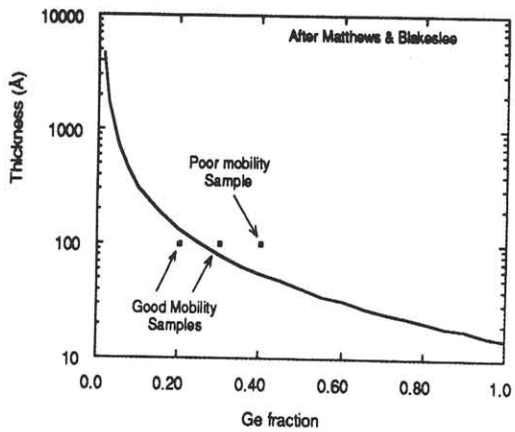

Fig. 7. Equilibrium critical thickness for $Si_{1-x}Ge_x$ strained layers on Si compared to our experimental structures.