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CONTROL OF INDIVIDUAL LAYER GROWTH TEMPERATURES BY RAPID TEMPERATURE SWITCHING IN $Si_{1-x}Ge_x$ MULTILAYER STRUCTURES GROWN BY RAPID THERMAL CHEMICAL VAPOR DEPOSITION

J.C. Sturm, H. Manoharan, V. Venkataraman, P.V. Schwartz, and P.M. Garone
Department of Electrical Engineering, Princeton University, Princeton, NJ 08544

ABSTRACT

In this paper the combination of rapid thermal processing (RTP) and chemical vapor deposition (CVD) is applied to the growth of silicon/silicon-germanium multilayer structures with critical vertical dimensions on the order of 100 Å . Using the measurement of infrared absorption to measure the wafer temperature in situ for feedback control, the ability to rapidly switch sample temperature makes it possible to optimize the growth temperature of individual layers in multilayer structures such as heterojunction bipolar transistors, superlattices, and modulation-doped layers. Measurements of the quantum properties of 2-D hole gases are used to place an upper limit of 8 Å to any non-abruptness of interfaces grown by this technique.

INTRODUCTION

The scaling of silicon device technology over the last 30 years has reduced typical vertical dimensions of critical features in the silicon from several microns to the order of 1000Å today. Such critical device dimensions are currently controlled by ion implantation. However, because of channeling, straggle, and the impracticality of fabricating heterojunctions, it is unlikely that ion implantation can produce vertical device dimensions scaled down a factor of 10 from current technology. Alternatively, this paper will apply the combination of rapid thermal processing and chemical vapor deposition to grow silicon and silicon-germanium device structures with layer thicknesses on the order of 100 Å .

It will be shown that longer growth times at low temperatures are favored over short times at higher temperatures when the abruptness of interfaces is limited by thermal diffusion, making it unnecessary to use rapid temperature switching to initiate and terminate growth cycles. However, a specific advantage offered by Rapid Thermal Chemical Vapor Deposition (RTCVD) is the ability to optimize the growth temperature of each layer in a multilayer structure. This degree of freedom does not exist in conventional MBE and CVD techniques. The growth technique is then applied to Si/SiGe superlattices and modulation doped structures, and a worst case estimate of the interface abruptness in these structures is established.

EXPERIMENTAL APPARATUS

The experiments were all carried out on 100-mm silicon wafers suspended horizontally on quartz pins (no susceptor) in a horizontal quartz tube with a diameter of about 175 mm. The source gases were introduced into one end of the tube, and the

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other end was connected to a vacuum system pumped by a two-stage rotary vane pump. The gas supplies were controlled by five-ported valves which allow the mass flow controllers to be stabilized before gas flows are switched into the growth chamber. The wafer heating was accomplished by a 70 KW-bank of tungsten-halogen lamps located outside the reaction tube. Because the quartz tube stays relatively cool, there is no deposition on the quartz tube, and only the wafer is heated. After loading, all samples were cleaned in situ by a bake in hydrogen (1000-1200 ° C) for 30s to 120s. All layers were grown at a pressure of 6.0 torr in a 3 lpm H_2 carrier with a dichlorosilane (SiH_2Cl_2) flow of 26 sccm. Germane (GeH_4) was added to the gas flow as a germanium source gas for the growth of $Si_{1-x}Ge_x$ layers.

Although the vacuum technology was similar to that of typical LPCVD polysilicon systems, all samples grown at temperatures as low as 625 ° C were single crystal with no dislocations, stacking faults, etc., evident in TEM micrographs. The surfaces of all wafers were specular with absolutely no "haze" or diffuse reflection observable in ultraviolet or visible light.

GROWTH KINETICS: HIGH VS. LOW TEMPERATURE AND TEMPERATURE SWITCHING

One clear obstacle to growing structures with vertical features on the order of 100Å is thermal diffusion. Early experiments carried out in a rapid thermal CVD apparatus were described as Limited Reaction Processing (LRP) [1]. The central feature of LRP is to establish the gas flows while the wafer is cold, and then to use a rapid change in sample temperature (~300 K/s) to start the growth reaction. (This is contrasted to conventional CVD where the wafer temperature is established before reactive gases are turned on). A motivation for LRP approach is to minimize the time the wafer spends at high temperature to reduce thermal diffusion. With LRP, the wafer is only at high temperature during the growth itself and not before or after the actual growth during any gas switching or purge cycles. Indeed, initial LRP results [1] of lightly-doped silicon epitaxial layers grown on heavily-doped substrates had epi-substrate interfaces indistinguishable (by SIMS) from those of similar structures grown by MBE at 600 ° C. However, subsequent energy dependent SIMS measurements on i-p^+-i structures (doping level ~5 x $10^{18}cm^{-3}$) grown at 1000 ° C revealed a doping interface abruptness of about 80Å /decade for interfaces at a depth of ~500Å [2]. Clearly such abruptness is not acceptable for the growth of device features on the 100Å scale. Using the actual growth rates of 0.2μm/min to establish times at growth temperatures, SUPREM process simulation indeed predicts similar interface abruptness without any excess time at the growth temperature. This clearly shows that even with rapid temperature switching, it will not be possible to grow structures at 1000 ° C with well-defined features on the 100Å scale.

Typical growth rate vs inverse temperature in our RTCVD reactor is shown in Figure 1. As expected, at high temperatures, growth is limited by mass transport, and at low temperatures surface reactions with an effective activation energy of ~1.9 eV are the limiting step. A similar activation energy is seen in low-temperature epitaxial growth from silane sources, and is thought to physically result from the rate of hydrogen desorption from the silicon surface [3]. The exact physical mechanism in the case of growth from dichlorosilane has not yet been indentified, however. Since typical activation energies for substitutional diffusion are 4-5 eV, diffusion will

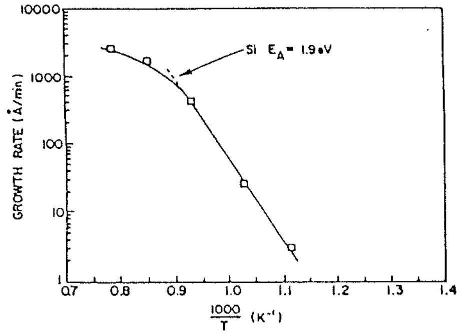


Fig. 1. Silicon growth rate vs inverse temperature.

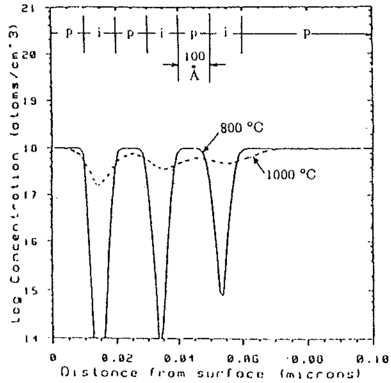


Fig. 2. SUPREM simulation of doping superlattice growth at temperature of 1000 ° C (0.25μm/min) and 800 ° C (0.02 μm/min)

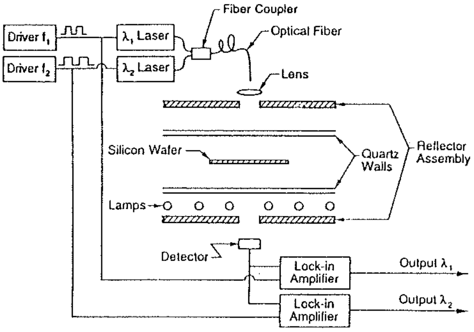


Fig. 3. Cross section of the experimental RTCVD apparatus for the in situ measurement of infrared transmission.

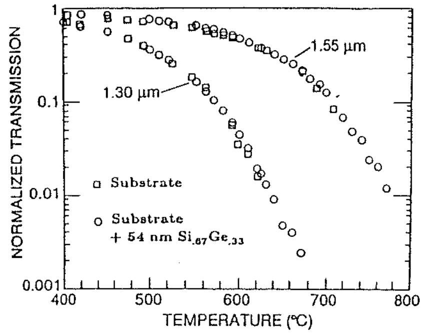


Fig. 4. Normalized transmission vs. temperature for a lightly doped p-type wafer (thickness = 445 μm) before and after the growth of 540 Å of $Si_{0.67}Ge_{0.33}$ on both sides of the substrate.

decrease faster than growth rates as the growth temperature is lowered. Therefore, even though longer growth times are required at lower temperatures, diffusion broadening of interfaces will be reduced compared to that at higher temperature growth. For example, using the growth rates of Fig. 1, SUPREM-III was used to simulate the growth of a doping superlattice (i-p^+-i-p^+) with alternating 100Å p^+ and i layers. The growth of the entire structure was simulated at both 1000 °C and 800 °C, with no excess time at the growth temperature (Fig. 2). The improvement in interface abruptness at 800 °C is clearly evident, with an abruptness of ~10Å /decade at 800 °C at a depth of 500Å . Therefore one can consider growth temperatures on the order of ~800 °C to be an upper limit for structures with well-resolved 100 Å layers.

At low growth temperatures, slower growth rates and longer growth times substantially reduce the motivation for using rapid switching of the sample temperature to control the growth interval. For example, if growth of a 100Å layer at 700 °C requires three minutes, one extra minute at the growth temperature to stabilize the temperature will have only a minimal marginal effect on the interface abruptness in the final structure (contrasted to one minute at 1000 °C for only a 10-second growth). To avoid potential problems with contamination of cold wafers between growth cycles and growth of low quality layers during temperature ramps up to the growth temperature, all samples described in the rest of this paper were not grown by controlling growth interval by temperature switching as in Limited Reaction Processing. Alternatively, in our approach to RTCVD, the wafer is first brought to the growth temperature in a hydrogen ambient, and the growth is then initiated and terminated by turning on and off the growth source gases. The characteristic time for gas partial pressures in our reactor to reach steady state after switching (reactor volume/total flow rate) is ~2 sec.

The above argument shows that using rapid temperature switching to initiate and terminate growth has little if any advantage from a diffusion perspective for layers on a 100 Å scale. However, the ability to rapidly switch sample temperature during growth is still very useful for the growth of multilayer samples in which different layers have different optimum growth temperatures. Because of three-dimensional growth tendencies and lattice strain, $Si_{1-x}Ge_x$ layers must be grown at a maximum temperature of ~625 °C for optimum results [3]. Although the silicon growth rate in our system is only a few Å /min at 625 °C, the growth rate for $Si_{1-x}Ge_x$ alloys can easily exceed 100Å /min because of the catalytic effect of germane on silicon growth [4]. Because the silicon growth rate in our reactor is so low at this temperature, it is useful to grow Si layers at 700 °C or above, while $Si_{1-x}Ge_x$ layers must be grown at 625 °C or less. In conventional CVD or MBE, one would have to pick a single growth temperature that was non-optimal for at least one of the two layers. However, with the ability to quickly change the sample temperature, in a RTCVD system all layers can still be grown at an optimum temperature. In our work, the growth of each layer is initiated and terminated by gas switching, and between layers the wafer temperature is rapidly changed directly to the new growth temperature in several seconds. This differs from Limited Reaction Processing, in which the sample is cooled to near room temperature between the growth of each layer, involving a growth interuption on the order of one minute. In the next sections, a method for measuring the sample temperature in situ will be described, and then our approach to RTCVD will be used for the growth of a 50-period superlattice.

TEMPERATURE MEASUREMENT BY INFRARED TRANSMSISSION

To enable rapid switching of the wafer temperature, a rapid thermal processing reactor configuration, with the wafer suspended on quartz pins without a susceptor, has been used in our experiments. A clear drawback of such a configuration, however, is the difficulty of measuring and controlling the wafer temperature. In a CVD process, accurate control of the wafer temperature is necessary for controlling the film composition and growth rate, especially when growing in the surface-reaction-limited regime. In a system without a susceptor, thermocouples cannot be used to measure the wafer temperature because it is not possible to non-invasively achieve good thermal contact between the sample and the thermocouple. Pyrometry is often used at temperatures above 800 ° C, but is unreliable at lower temperatures for several reasons. For example, the emissivity is well known to be a function of temperature [5], surface finish, doping, etc., and extra care must be taken to avoid interference from the lamps.

To overcome these problems, we instead monitor the wafer temperature by measuring the optical absorption of the wafer [6], instead of its optical emission as in pyrometry. In the near-infrared (1.3 - 1.5 μm) the optical absorption of silicon can proceed by both band-to-band and free carrier mechanisms. As the temperature increases, bandgap decreases (which increases the free carrier concentration) and the phonon population also increases. Both of the absorption mechanisms will then increase with increasing temperature. Therefore one can use optical absorption as a monitor of the wafer temperature. Our RTCVD growth apparatus was modified to perform these measurements in-situ during growth cycles (fig. 3). Key features of the system are the use of semiconductor lasers coupled to optical fibers, which makes it easy to "pipe" the light into the reactor, and the use of lock-in amplifiers to remove lamp interference. Finally, the transmission of all samples is normalized (divided) by its room temperature value to remove effects such as detector efficiency, wafer backside roughness scattering, etc. Typical results of normalized transmission vs growth measured in the RTCVD apparatus, with the absolute temperature measured by a welded thermocouple, are presented in fig. 4 as the data labelled substrate. The data agree well with that measured in a specially-adapted conventional furnace where the temperature was measured with conventional thermocouples. One notes a strong dependence of the absorption on temperature, with transmission falling by an order of magnitude within a 75 ° C temperature spread at higher temperatures. This makes absolute temperature measurement with an accuracy on the order of 1 ° C practical on a routine basis.

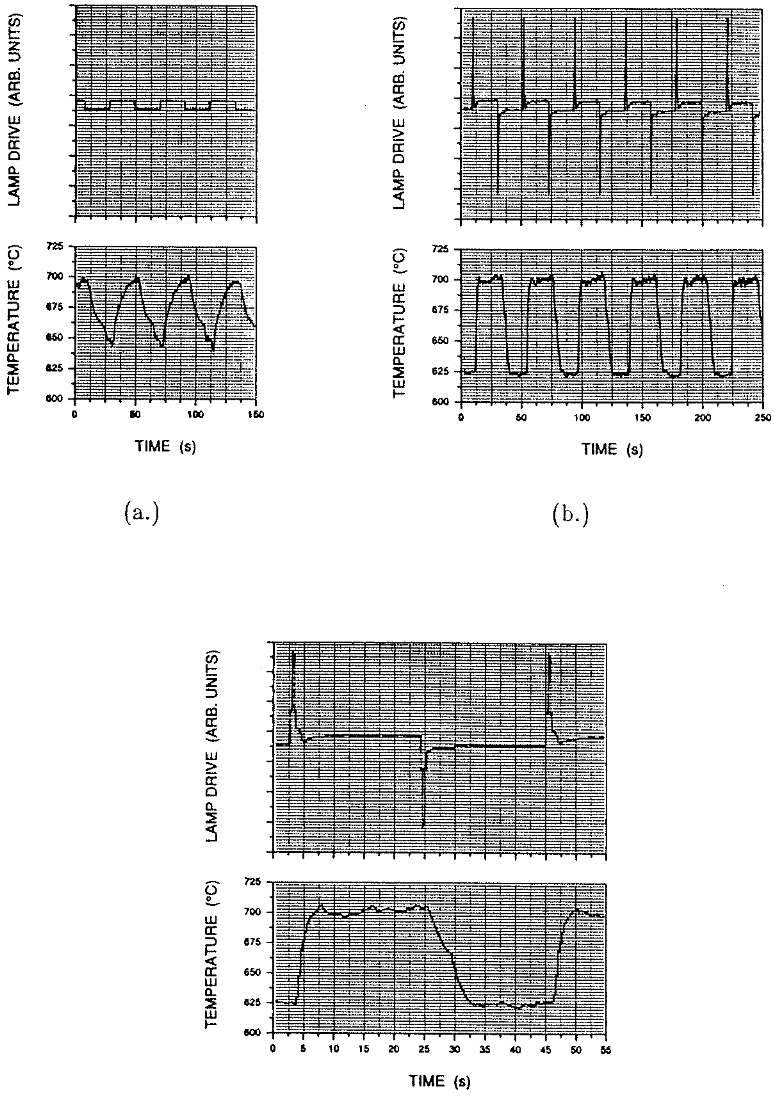
When growing $Si_{1-x}Ge_x$ layers on silicon, it is possible that the narrow bandgap $Si_{1-x}Ge_x$ would lead to significant extra absorption, causing the transmission vs temperature relationship of a silicon substrate to vary as the sample is growing. This was tested by growing a 540 Å layer of $Si_{0.67}Ge_{0.33}$ on both sides of the wafer of fig. 1. Although the layer was mostly strained (giving a minimum bandgap), this wafer had virtually the same transmission vs temperature (fig. 4) as the substrate, within the experimental error (10%) of the measurements. Other experiments have shown that the absorption from unstrained $Si_{0.57}Ge_{0.43}$ up to 1.1 μm in thickness and from strained $Si_{0.55}Ge_{0.45}$ up to 1100 Å in thickness (total thickness of many layers in a multiple quantum well sample) have less than a 20% effect on transmission. Below these thickness limits, therefore, the transmission vs absorption data of fig. 4 can be used to measure the sample temperature during SiGe growth cycles.

ACTIVE TEMPERATURE CONTROL AND SUPERLATTICE GROWTH

As described earlier, the optimum growth temperature for silicon in our system using dichlorosilane is higher ($\geq$ 700 ° C) than that for $Si_{1-x}Ge_x$ grown from dichlorosilane and silane (625 °C). With the ability to rapidly switch temperature afforded by RTP-CVD, one can optimize the growth of individual layers. For example, consider the growth of a $Si/Si_{0.80}Ge_{0.20}$ structure with desired growth temperatures of 700 and 625 ° C and growth rates of 30 Å /min and 80 Å /min for the Si and SiGe, respectively. A structure with layer thicknesses of ~ 10's of Å will require growth times under one minute, making temperature switching times on the order of seconds desirable. Previous growth of SiGe/Si multilayer structures by RTP-CVD has been done by the Limited Reaction Processing approach, where the sample was allowed to cool at room temperature between the growth of each layer and no active temperature control was used [7]. One drawback of the LRP technique include the fact that considerable time (~ 1 min.) is required to wait for the sample to cool between each layer (with the possibility of interfacial contamination occurring during the growth interruption). Furthermore, wafer-to-wafer variation or aging in the lamps could cause open loop temperature control to yield inaccurate results. In our approach to RTCVD, the initiation and termination of growth is controlled by gas switching (not the sample temperature as in LRP), the lamp power is actively controlled by feedback, and the temperature is directly changed to the new growth temperature for each layer without first cooling to room temperature.

Due to the relatively slow wafer cooling in the 600 °C range, the open loop natural response of the wafer temperature to a step in the lamp control signal is fairly slow. For example, fig. 5(a) shows the temperature of a wafer as the lamp control signal is switched between its values for steady-state temperatures of 625 and 700 ° C on 20 s intervals. Slow response on this time scale, with a time constant of ~ 10 s is seen. Improved performance can be achieved by actively controlling the lamp power, using the optical transmission to measure the wafer temperature as a feedback signal. A PC linearizes the feedback signal and implements closed loop PID control (fig. 6). Using active control, the much improved results of fig. 5(b) can be obtained in response to a step change in the desired temperature (alternating between 625 and 700 ° C on 20 s intervals). An expanded time scale (fig. 5(c)) shows that the risetime of the temperature is ~ 3 sec., and the falltime is ~ 6 sec.

We routinely apply such active temperature control by infrared transmission to the growth of $Si/Si_{1-x}Ge_x$ multilayer structures. For example, a 50 period superlattice structure of 22Å Si/24Å $Si_{0.80}Ge_{0.20}$ (period = 46 Å) was grown by alternating 43 s of silicon growth (using dichlorosilane) at 700 ° C with 18 s of $Si_{0.80}Ge_{0.20}$ growth (from dichlorosilane and germane) at 625 ° C. To allow for temperature stabilization and any possible gas switching latencies, the germane flow was turned on 15 s after the temperature was first lowered and was turned off 10 s before the temperature was raised. A single-crystal X-ray diffractometer scan of this sample using Cu-k_α radiation is shown in fig. 7. (The double peaks in the fine structure of the diffraction peaks results from the two Cu-k_α X-ray lines.) The average composition of the superlattice can be inferred from the position of the zeroth-order superlattice peak with respect to the silicon substrate signal. From the shift in 2θ of 0.65 ° , one calculates an average composition of $Si_{0.88}Ge_{0.12}$, which agrees well with the targeted $Si_{0.89}Ge_{0.11}$. From the position of the first order satellites, one can calculate a period of 46 A , also in excellent agreement with the targeted structure. Note that the



(a.)

(b.)

(c.)

Fig. 5. Wafer temperature as a function of time (a.) in response to a step in the lamp drive signal (open loop), and (b., c.) in response to a step change in the temperature setpoint using active control and infrared temperature feedback.

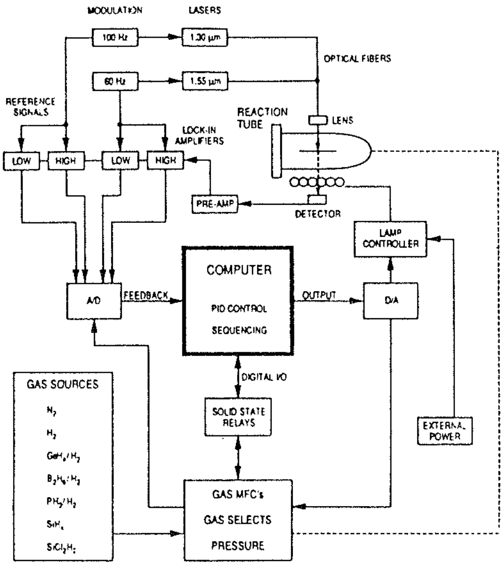


Fig. 6. Schematic diagram of the computer-controlled growth system implementing active temperature control.

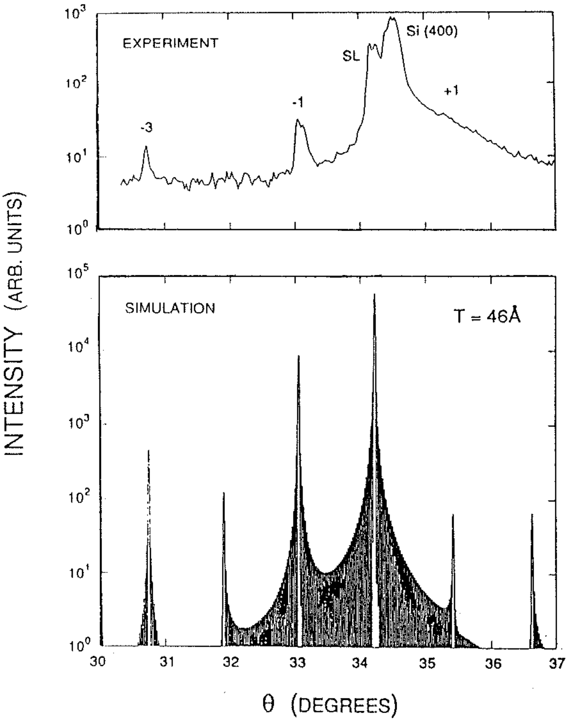


Fig. 7. X-ray diffraction spectrum of a 50-period superlattice of Si (22 Å)/$Si_{0.80}Ge_{0.20}$ (24 Å) and a first principles simulation of such a superlattice with abrupt interfaces.

study interface abruptness from the magnitude of the superlattice satellite diffraction peaks. Such a study was limited by the signal/noise ratio of the spectrometer, however. Instead, interface abruptness was studied by observing the electrical performance of 2-D hole gases at Si/SiGe interfaces.

TWO-DIMENSIONAL HOLE GASES

Because the bandgap discontinuity in strained $Si_{1-x}Ge_x$ on Si substrates lies primarily in the valence band, the fabrication of 2-D hole gases at a $Si_{1-x}Ge_x$/Si interface by modulation doping is in principle straightforward. A boron-doped Si layer should yield a 2-D hole gas in an adjacent undoped SiGe layer. To improve the mobility in such structures, one typically also adds a thin (~100 Å) undoped Si spacer layer between the doped Si and the $Si_{1-x}Ge_x$. Because it is very sensitive to minute changes in the structure parameters such as germanium concentration, spacer thickness, etc., the hole concentration is a useful parameter for comparing these structures.

As an experiment, an undoped $Si_{0.8}Ge_{0.2}$ layer was grown at 625 ° C between two heavily-boron-doped ($3x10^{18}cm^{-3}$) Si layers grown at 700 ° C (fig 8). The doped Si layers were separated from the $Si_{0.8}Ge_{0.2}$ layers by undoped Si spacers of ~50Å width. The interface between the i and p^+ Si was achieved by simply switching the doping source on or off, and between SiGe and Si growth was interrupted as the temperature was changed, similar to the procedure in the superlattice described earlier. After growth, aluminum alloying was performed to contact both 2-D gases in parallel. This symmetric structure should ideally form two identical 2-D hole gases, one at each SiGe/Si interface. However, the lower 2-D hole gas results from a spacer grown on top of heavily doped Si, and the SiGe is grown on top of the Si. The top 2-D hole gas has the sequence reversed. Because any autodoping, latències caused by gas switching, surface segregation of B or Ge, etc., would cause the structure to be somewhat asymmetric, one in practice rarely finds two identical 2-D hole gases in such structures, even when grown by MBE [8].

To probe our strucuture, low-temperature Hall measurements were performed. Low magnetic field measurements (Fig. 9) confirmed a 2-D gas, since a constant hole density at low temperature is seen. The total number of carriers at both interfaces equal to $2.6 \times 10^{12}cm^{-2}$. Such data does not discriminate between the carriers at the two interfaces, however. The maximum mobility of 1000 $cm^2/V{\cdot}s$ is thought to be limited by the residual background doping in our SiGe films, which is $\sim 10^{17}$ cm^{-3} even in thick films. High magnetic field measurements were then performed, and Shubnikov-de-Haas oscillations of the magnetoresistance vs magnetic field were observed. According to theory, the oscillation frequency depends only on the number of carriers in the 2-D gas. A single oscillation frequency in 1/B was observed by taking the Fourier power spectrum of R_{xx} (Fig. 10). That one frequency is observed means that if two 2-D gases are present, both must have the same carrier density. Further evidence of two identical gases is given by the fact that from the oscillation frequency one find a 2-D gas carrier density of $\sim 1.3 \times 10^{12}cm^{-2}$, half of the low-field total carrier density (which thus consists of two identical 2-D gases.) Still stronger evidence is given by R_{xy} data exhibiting the quantum Hall effect (Fig 11). Simple theory predicts that the plateaus in resistance for a single gas are given by $R_{xy} = h/\nu e^2$, where ν is an even integer. As can be seen in Fig. 11, $\nu = 12,14,18$,etc. are missing from the data. This is because two identical channels in parallel will halve the measured resistance, so the measured R will be $h/2\nu e^2$.

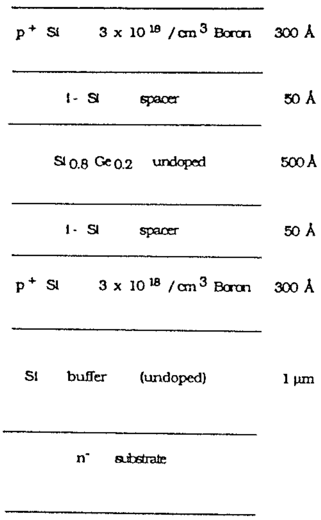


Fig. 8. Cross section of the two 2-D hole gas structure.

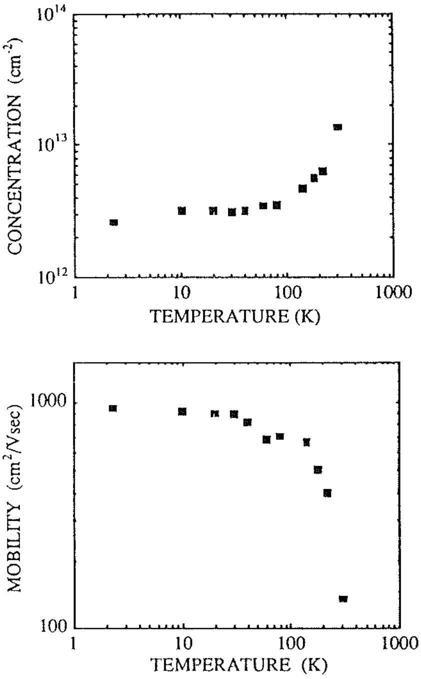


Fig. 9. Hole density and mobility vs temperature from Hall and Shubnikov-de-Haas measurements.

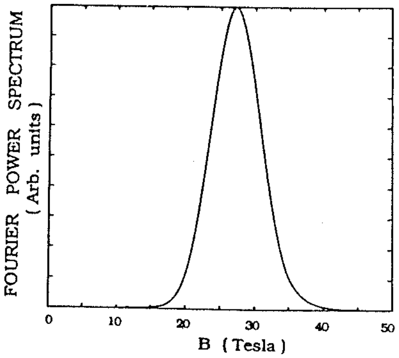


Fig. 10. Fourier power spectrum of magnetoresistance R_{xx} from Shubnikov-de-Haas oscillations.

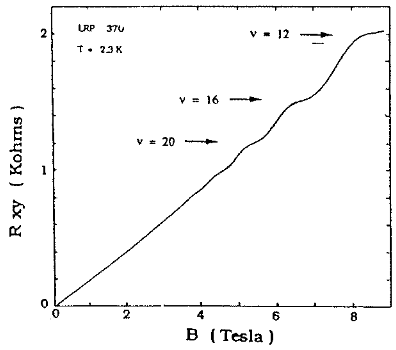


Fig. 11. R_{xy} of the quantum hall effect at 2.3 K. Plateau index ν is from $R = e^2/h\nu$.

Based on the finite width of the peak in fig. 10, one can infer that the carrier concentrations of the two hole gases must be equal to within ~10% To relate this maximum asymmetry in hole concentration to possible structure asymmetries, simulations of the expected hole density for various structure parameters and interface gradings were performed. It was found that the i Si spacers (nominally 50 Å) can differ in thickness by at most 8 Å . Effects such as autodoping, doping due to residual gas pockets after gas switching, or boron surface segregation all would cause opposite effects in one 2-D gas compared to the other, hence causing an asymmetry. Therefore the effect of any of these phenomena, if they occur, is less than 8 Å in this structure. Since the 2-D hole gases are at the interfaces, they are not sensitive to the width of the SiGe layer. They are very sensistive to the Ge concetration at the interface and any grading of the interface, however. Comparsion of the maximum 10% difference in hole density shows that any asymmetric grading of the Si/SiGe interface (caused by Ge segregation, for example), occurs over a distance of less than 8 Å . Similar results have been reported in structures grown at $\leq 550\,^\circ$C by the UHV-CVD technique [9]. Our structures were exposed to temperatures as high as 700 ° C, however, with no degradation in the quantum electron transport properties.

CONCLUSION

For the growth of next generation device profiles by direct epitaxial growth, growth temperatures on the order of 800 ° C or less will be required. At these lower temperatures the motivation to rapidly switch temperature to start and stop growth becomes less important, and conventional gas switching can be used. However, the ability to switch sample temperature remains very valuable for optimizing the growth temperature of each layer. Using infrared transmission for feedback control, the sample temperature can be changed in times on the order of seconds. This technique has been applied to the growth of $Si/Si_{1-x}Ge_x$ strained-layer superlattices, and also to ideally symmetric 2-D hole gas structures.

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