Device Research Conference, Boulder, CO, June 17-19, 1991

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IIB-4 Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's—C. M. Ransom, T. N. Jackson, and J. F. DeGelormo, IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598.

We have fabricated the first gate-self-aligned germanium MOSFET's. Using a germanium oxynitride gate-dielectric [1], we have fabricated n- and p-channel germanium inversion-mode MOSFET's with record transconductance (> 100 mS/mm at room temperature at a gate length of 0.6 μm for both n- and p-channel devices).

Germanium MOSFET's are of interest because germanium offers large and nearly equal channel mobilities for both electrons and holes (~ 2000 cm^2/V · s for lightly doped material). Historically, Ge MOSFET performance has been limited by materials quality and processing technology. In particular, the germanium native oxide (the analog of SiO_2) is hygroscopic, and it has been difficult to build useful inversion-mode devices with deposited dielectrics due to large interface-state densities. Recently, germanium MOSFET devices have been built using a grown germanium oxynitride with a best reported transconductance of 27 mS/mm for a 2.3-μm p-channel device [1].

The devices reported in this work are gate-self-aligned inversion-mode germanium MOSFET's. By gate-self-aligned we mean that the gate is used as the mask structure for the ion implantation that forms heavily doped source and drain regions (previous self-aligned Ge MOSFETs used a dummy-gate process [1]). The devices reported here use a 200-Å-thick gate dielectric formed by nitridation of a thermally grown germanium oxide on 10-Ω · cm germanium substrates. Aluminum gates with length from 0.25 to 2.0 μm were fabricated by lift-off using a two-layer resist process. Electron-beam lithography was used for gate lengths ≤ 0.5 μm. Aluminum was chosen to provide a low sheet resistance since the aluminum–dielectric interface will withstand the relatively low temperature processing required to activate the self-aligning implant in Ge. After gate patterning, a 3×10^{14}/cm^2, 15-kV, phosphorus-ion implantation was used to form the self-aligned source and drain regions for the n-channel devices. Similarly, a 2×10^{14}/cm^2, 10-kV, boron-ion implantation was used to form the p-channel self-aligned source and drain regions. The self-aligning ion implantations were activated by annealing at 350–400°C which also reduces the interface-state density for the aluminum–oxynitride-germanium system. After the anneal and a contact lithography, Pd/Au ohmic contacts were deposited and patterned by lift-off to complete the devices.

The n-channel MOSFET's fabricated as described above had a maximum transconductance of 120 mS/mm at room temperature for 0.6-μm gate-length devices. p-channel MOSFET's had a maximum transconductance of 104 mS/mm at room temperature for 0.6-μm gate-length devices. The maximum transconductance for both n- and p-channel devices remained essentially unchanged as temperature was reduced from 300 to 77 K. Channel mobilities were greater than 1000 cm^2/V · s for both n- and p-channel devices obtained from long-channel device characteristics. Short-channel, n-channel, and p-channel 0.25-μm devices have maximum transconductance over 80 mS/mm at room temperature. These are the shortest gate-length germanium devices yet reported.

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IIB-5 Current Gain–Early Voltage Products in Graded-Base Si/Si$_{1-x}$Ge$_x$/Si Heterojunction Bipolar Transistors—E. J. Prinz and J. C. Sturm, Dept. of Electrical Engineering, Princeton University, Princeton, NJ 08544.

The product of common emitter current gain β and Early voltage V_A is a figure of merit for analog applications of bipolar transistors. In homojunction transistors there is a tradeoff between high gain and high Early voltage, determined by the neutral base charge Q_B. For a 3-GHz analog process, βV_A is typically 5000 V [1]. Here we examine the β–V_A tradeoff for graded base Si/Si$_{1-x}$Ge$_x$/Si heterojunction bipolar transistors (HBT's). Using a two-layer stepped-based structure, we have achieved a βV_A product greater than 100 000 V at room temperature for a device predicted to have a cutoff frequency f_T in excess of 10 GHz. This is an improvement of this figure of merit by a factor greater than 20.

In a homojunction bipolar transistor, V_A is determined by the neutral base charge Q_B and the base collector capacitance C_{BC}, as in $V_A = qQ_B/C_{BC}$, and β is inversely proportional to Q_B. For a flat-base Si/SiGe/Si HBT, V_A is essentially the same, but the lower bandgap of the SiGe base causes β to increase by $\exp(\Delta E_G/k_BT)$, where ΔE_G is the bandgap reduction in the SiGe base with respect to silicon. It is therefore possible to achieve a high Early voltage by increasing Q_B and compensating for the decreasing β by adding Ge to the base layer. For high Ge concentrations in the base, however, exceeding the equilibrium critical thickness of the strained SiGe layer causes misfit dislocations at the Si/SiGe interfaces which degrade the electronic properties of the structure.

Here we show that the Early voltage in a bipolar transistor can be improved dramatically by inserting a thin heavily doped p$^+$-SiGe layer at the collector side of the base, without any reduction in gain. For such a stepped base structure, β is determined by the low Ge part of the base, whereas V_A depends on the smaller bandgap caused by the higher Ge concentration at the edge of the base-collector depletion region. The improvement in V_A is by a factor of $\exp(\Delta E/k_BT)$, where ΔE is the bandgap reduction at the collector side of the base compared to the widest bandgap region in the base. This can be seen from a simple model, based on Kroemer's approach for HBT's with arbitrary base gradings [2]. For an HBT in which the base current is determined by hole injection into the emitter, $I_B = I_{B,0}\exp(qV_{BE}/k_BT)$

$$\beta = \frac{q}{I_{B,0}}\left(\int_0^W \frac{N_A(x)}{n_i^2(x)D_n(x)}\,dx\right)^{-1}$$

and

$$V_A = \frac{q}{C_{BC}}\, n_i^2(W)D_n(W)\int_0^W \frac{N_A(x)}{n_i^2(x)D_n(x)}\,dx$$

where N_A, n_i, and D_n are boron concentration, intrinsic carrier concentration, and minority-carrier diffusion coefficient in the base, and W is the neutral base width. Since the Ge-rich region can be made very thin (<50 Å), there are virtually no critical thickness limitations.

HBT structures with various base germanium profiles were grown by RTCVD, and devices processed as described in [3]. Devices with a 14% Ge flat base, and stepped-base devices with 14% Ge near the emitter and 25% Ge near the collector, and *vice versa*, all had gains between 750 and 2000, as expected, and near ideal base current characteristics. The device with 25% Ge near the collector had an Early voltage of 92 V, leading to a βV_A of more than 100 000 V, compared to 13 000 and 6600 V, respectively, for the other two devices. These values, as well as values obtained from other devices with various base gradings, are in good agreement with our

model. The high value of βV_A is an improvement by a factor of 20 compared to state-of-the-art bipolar devices.

[1] J. Lapham, Analog Devices, private communication.
[2] H. Kroemer, *Solid State Electron.*, vol. 28, pp. 1101–1103, 1985.
[3] E. J. Prinz *et al.*, *IEEE Electron Device Lett.*, vol. 12, pp. 42–44, 1991.

IIB-6 SiGe/Si Camel-Barrier Heterojunction Internal Photoemission LWIR Detector—T. L. Lin, S. M. Dejewski, A. Ksendzov, and E. W. Jones, Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Drive, Pasadena, CA 91109.

Si-based infrared detectors are very attractive for focal plane array applications because they have good pixel-to-pixel uniformity, use normal incident radiation (in contrast to quantum-well devices), and can be easily integrated with Si readout circuitry to form large arrays. Previously, a SiGe/Si heterojunction internal photoemission (HIP) detector has been demonstrated with tailorable long-wavelength infrared (LWIR) response [1]. The HIP detector utilizes the SiGe/Si valence-band offset, which can be tailored by varying the Ge composition in the SiGe layer, as the energy barrier for internal photoemission of photo-excited carriers. Quantum efficiencies (QE) of 3–5% in the 8–12-μm range have been reported for nonoptimized detectors.

There is strong interest in detectors which offer a dynamically tailorable response for real-time image discrimination, for example, by varying the biasing voltage. Previously, a Si homojunction infrared detector has been reported with electrically tailorable LWIR response with ~0.001% QE [2]. This detector utilizes the camel barrier, which is formed by the space charge of a depleted p-type barrier layer sandwiched between an n^+ emitter layer and n-Si substrate, as the energy barrier. The camel-barrier height can be adjusted by varying the detector doping profiles and the biasing voltage. The low QE results mainly from the fact that photoexcited carriers have to travel a larger distance and thus suffer significant scattering before they can reach the energy barrier, located well within the barrier layer.

We report here a novel SiGe/Si camel-barrier heterojunction internal photoemission (CHIP) infrared detector, which is a combination of the HIP detector and the camel-barrier detector, with both statically and dynamically tailorable LWIR photoresponse. The CHIP detector consists of a p^+-SiGe emitter layer, an n-Si camel-barrier layer, and a p-Si substrate as the collector. The p^+-SiGe layers and the n-Si camel-barrier layers were grown on patterned p-Si substrates using molecular beam epitaxy (MBE). The detection mechanism involves the generation of hot holes through infrared absorption in the p^+-SiGe layer, followed by internal photoemission of the photoexcited holes over an energy barrier consisting of the SiGe/Si valence-band offset and the camel barrier. Strong infrared absorption was achieved by utilizing degenerate boron doping in the p^+-SiGe layers. For example, absorption of 40–45% in the 5–15-μm regime has been achieved in a 50-nm-thick SiGe layer doped with 5×10^{20} cm^{-3} boron. The energy barrier of the CHIP detector is the sum of the SiGe/Si valence-band offset and the camel barrier. The CHIP detector offers statically tailorable response by varying the Ge composition in the SiGe as for the HIP detector, and electrically tailorable response by varying the biasing voltage as for the camel-barrier detector.

Preliminary CHIP detectors have been fabricated by MBE growth of 30-nm-thick SiGe layers with 30% Ge composition and 10-nm-thick Sb-doped Si layers on patterned p-type Si substrates. The detectors incorporate n-type guard rings defining the periphery of the active device areas to suppress leakage current. QE of 2–3% has been observed at 8–12 μm at −1.5 V bias. The electrical tailorability of the CHIP detector was demonstrated by the increasing detector response with increasing biasing due to reduction of the camel barrier. For example, the QE at 8 μm increases from 0.2% at −0.6-V bias to 3.2% at −1.5-V bias.

In conclusion, a novel SiGe/Si CHIP detector has been demonstrated with electrically tailorable LWIR response in addition to the statically tailorability of the previously proposed HIP detector. Photoresponses at wavelengths of 5 to 12 μm have been obtained with electrically tailorable QE's of 0.2–3.0% in these nonoptimized device structures. The electrical tailorability of the CHIP detector offers significant flexibility for infrared imaging applications.

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[2] S. Tohyama, N. Teranishi, K. Konuma, M. Nishimura, K. Arai, and E. Oda, in *IEDM Tech. Dig.*, 1988, p. 82.

IIB-7 A New Device Structure and Process Flow for a Low-Leakage p-i-n Diode-Based Integrated Detector Array—Walter Snoeys, James Plummer, Sherwood Parker* and Chris Kenney*, Center for Integrated Systems, Stanford University, Stanford, CA 94305.

Several types of radiation such as X-rays, infrared light, and ionizing particles can be detected by means of reverse-biased p-i-n diodes. In this paper a novel device structure enabling integration of a one- or two-dimensional array of p-i-n diodes (providing one- or two-dimensional spatial resolution, respectively) with readout circuitry on the same high-resistivity substrate is presented. The spatial resolution is maximized by building the circuitry "on top" of the detecting elements, while avoiding loss of signal charge into the circuitry. A special gettering step to obtain low leakage in the p-i-n diodes is presented as well. The specific application for which this method was developed is a particle detector for high-energy physics, but many other applications are also possible.

The following device structure was implemented: the substrate is high resistivity p-type (approx. 10^{12} cm^{-3}), and a junction common to all detecting elements is formed by an n-type diffusion on the back side of the wafer. The circuitry needed for each detecting element is placed inside an n-well on the front side of the wafer. The n-well has cuts in it which are p-type, and form contacts to the p-type substrate. Their size is limited by lithographic limits and can therefore be made quite small. The substrate is depleted from the back side up by reverse biasing the junction on that side. Once the substrate is fully depleted the contacts to the substrate are electrically isolated from each other. They each correspond to a separate detecting element, which consists of the contact and that fraction of the depleted substrate from which they collect the generated charge. This device structure is an improvement over a structure proposed earlier [1], which used a well of the same type as the substrate, but had much less resolution, and over other approaches, which are prone to catch signal charge in the readout circuitry where it would be lost for readout. In [1], the top-side contacts formed the junction of the p-i-n diodes and had to have a much larger area to prevent breakdown. However, the improvement comes with a price: one needs to pattern the back side to ensure proper junction termination when the wafer is diced.

The devices were built in a sixteen-mask process, based on the