1989 SOS/SOI TECHNOLOGY WORKSHOP

October 3-5, 1989

AGENDA

Monday, October 2

8:00-10:00 pm Conference Registration

Wine and cheese reception

Tuesday, October 3

7:00-8:00 am Continental Breakfast

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2:40-3:00 pm BREAK

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5:00-6:30 pm SEMI SOS Subcommittee Meeting

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2: Ballot: Secondary Flat Orientation
3: Task Force Report: Proposed Specifications for 125 and 150 mm diameter sapphire substrates
4: New Business
5: Next meeting date

8:00 pm CONFERENCE BANQUET

Banquet Speaker: Dr. John Moll
Hewlett-Packard Laboratory
Palo Alto, CA

Wednesday, October 4

7:00-8:00 am Continental Breakfast

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L2	"A 6.2 GHz Digital CMOS Circuit in Thin SIMOX Films" G.K. Celler, H.-I. Cong, R.L. Field, S.J. Hillenius, A. Kamgar, W.S. Lindenberger, L. E. Trimble (ATT Bell Labs, Murray Hill, NJ) J. C. Sturm (Princeton University, Princeton, NJ)	139
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3:20 pm **CONCLUDING REMARKS:** J.-P. Colinge

1989 SOS/SOI Technology Conference, Stateline, NV, Oct. 3-5, 1989

Substrate Bias and Temperature Dependence of Anomalous Subthreshold Slopes in Fully-Depleted Submicron SOI MOSFET's

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Recently, anomalously sharp subthreshold slopes have been reported in non-fully depleted short-channel SOI MOSFET's [1,2]. Since this effect varies with drain voltage and can cause excessive leakage currents in circuit operation, it could be a serious impediment to the widespread use of SOI for VLSI applications. We here report observation of the effect in fully-depleted ultra-thin SOI MOSFET's, but have found that it can be eliminated by control of the lower SOI interface charge condition. The temperature dependence of this effect has also been investigated.

Classically, the subthreshold slope of a MOSFET is independent of drain voltage, with an optimum value of kT/q ln(10) /decade, corresponding to 59 mV/decade at room temperature. One expects to measure this ideal value when there are no parasitic capacitances coupling to the channel. In fig. 1 is shown the normalized subthreshold slope "n" (measured slope/ideal value) as a function of drain voltage and substrate bias of 0.8-µm n-channel SOI FET's for temperatures from 86 K to 370 K. The 1000-Å SOI films were formed by oxygen implantation and relatively low temperature (1250 C) annealing. The gate oxide thickness was 250 Å, and the film doping was chosen to yield full depletion during FET operation. At all temperatures, several universal trends are noted.

First, for $V_D = 0.1$ V, a minimum subthreshold slope is consistently observed for V_{BB} (substrate bias) of about - 3 V, increasing to a much larger value for $V_{BB} = -10$ V. Separate measurements of threshold voltage vs. substrate bias show that -3 V corresponds to full depletion of the SOI film and lower interface. In this condition parasitic channel capacitances are minimized, and an optimum substhreshold slope is indeed expected [3]. For a substrate bias of -10 V, the lower SOI interface is accumulated, pinning the backside potential and introducing a parasitic channel capacitance. Calculations based on a simple capacitor model predict a "n" of 1.8 in this case, in good agreement with experiment. For substrate biases more positive than -3V, conduction in the lower SOI channel becomes significant. This current is not as efficiently modulated by the front gate voltage, resulting in a degradation of subthreshold slope in all cases.

The subthreshold slope for $V_D = 0.1$ V scales well with temperature from 200K to 370 K, with a constant minimum "n", as expected from simple theory. The minimum "n" of 1.3 is consistent with an interface state density of about 10^{11} eV^{-1} cm^{-2}. At 86 K, the minimum n increases to 1.9. This could be caused by a surface potential fluctuation in space which would be insignificant at larger kT.

For larger drain voltages, the subthreshold slopes are virtually unchanged in the case of full depletion at the lower SOI interface. However, a radical drop in subthreshold slope is seen when the substrate bias is decreased below -3V. Although the SOI film body is depleted, accumulation at the lower SOI interface causes an effective hole "trap" to be present in the band diagram at the lower interface. Holes injected into the SOI film from thermal leakage or avalanche at the drain junction will be trapped, leading to a positive SOI body bias and increased current. This multiplication mechansism leads to the anomalously sharp slopes, exactly as in thicker non-fully depleted films [2]. When the lower interface is fully depleted, the hole "trap" is removed from the band diagram, inhibiting the multiplication mechanism and the anomalous slopes. Since the anomalous slopes can lead to increased leakage in circuits, the fully-depleted operating condition is the optimum design condition for VLSI operation.

The support of Hewlett Packard, Rucker and Kolls, and IBM is acknowledged.

1. J.R. Davis, A.E. Glaccum, K. Reeson, and P.L.F. Hemment, IEEE Elec. Dev. Lett. **EDL-7**, 570-572 (1986).
2. J.G. Fossum, R.Sundaresan, and M.Matloubian, IEEE Elec. Dev. Lett. **EDL-8**, 544-546 (1987).
3. J-P. Colinge, IEEE Elec. Dev. Lett. **EDL-7**, 244-246 (1986).

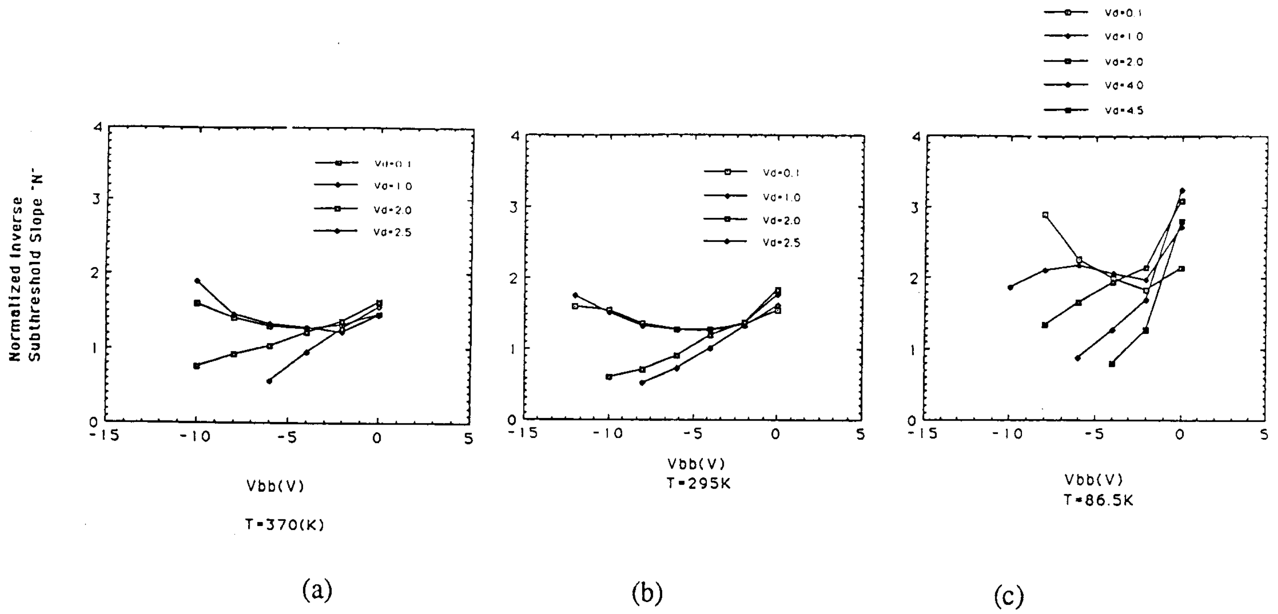

Fig. 1. Drain voltage and substrate bias dependence of normalized subthreshold slope at 370 K, 295 K, and 86 K.

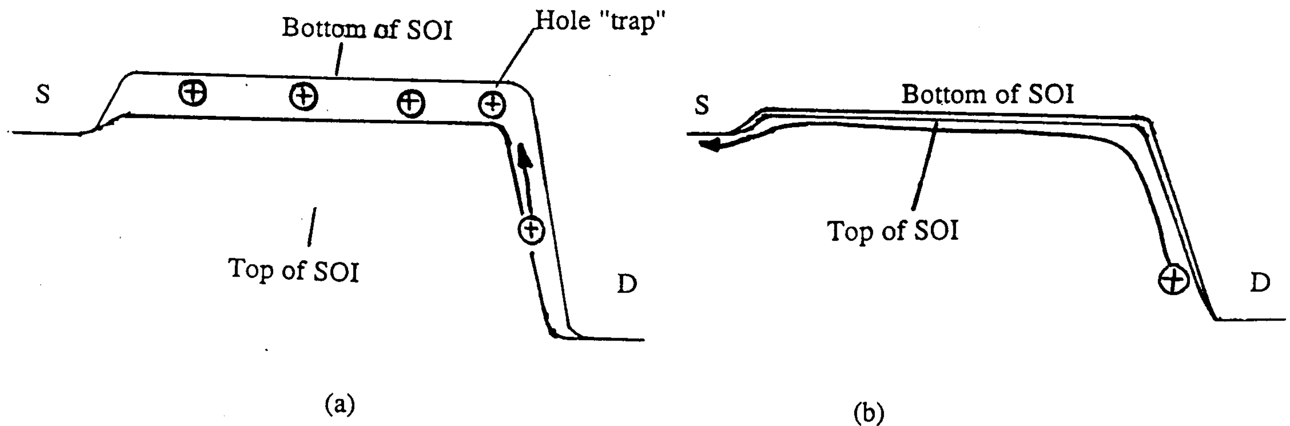

Fig 2. Valence band diagrams of a fully-depleted SOI MOSFET in subthreshold with (a) an accumulated lower interface, and (b) a depleted lower interface.