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CARRIER CONFINEMENT IN MOS-GATED Ge_xSi_{1-x} / Si HETEROSTRUCTURES

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ABSTRACT

In this paper the confinement of carriers in a MOS-gated Ge_xSi_{1-x} heterostructure is numerically modeled and experimentally confirmed. The structure, which may be useful for improved pMOS device performance[1], uses a MOS gate to modulate the hole density at a buried Si/Ge_xSi_{1-x} interface. Numerical modeling is used to predict the maximum number of carriers achievable at the interface as a function of the structure design, and clear experimental evidence for such carrier confinement is given.

INTRODUCTION

The performance of CMOS circuits is, in a large part, limited by the low transconductance of pMOS transistors. This transconductance could be improved by raising the hole mobility. One path to such mobility improvement may be to place a buried Ge_xSi_{1-x} layer under the gate of a pMOS transistor. A "quantum" well for holes is then created, since the bandgap discontinuity is predominantly in the valence band[2] (Figure 2a). A typical device structure is shown in Figure 1. The MOS gated Ge_xSi_{1-x} heterostructures may be able to increase the mobility in two ways:

1. Reducing the surface scattering by forming an inversion layer, not at the Si-SiO_2 interface but rather in a Ge_xSi_{1-x} layer separated from the surface by a Si spacer.
2. Enhanced hole mobility resulting from the strain of the Ge_xSi_{1-x} layer[3].

By applying a negative gate voltage, one can modulate the number of holes in the Ge_xSi_{1-x} well , eventually forming an inversion layer (figure 2b). However if a large gate bias is applied the dominant hole population will be at the Si-SiO_2 interface (figure 2c). This paper determines how many holes can actually be confined in the Ge_xSi_{1-x} buried layers as a function of the design parameters. Simulations of such a structure will be shown along with experimental evidence for the formation of an inversion layer in the Ge_xSi_{1-x} well of several test structures.

SIMULATIONS

A numerical model was developed which finds the one dimensional electrostatic solution of Poisson's equation for a MOS-gated Ge_xSi_{1-x} capacitor at a given gate bias. Information regarding the band offsets was taken from calculations by Van de Walle et al.[4] for commensurately strained $Ge_x Si_{1-x}$ on silicon substrates. The splitting of the band degeneracy is included. The device structures for the simulations consists of a 100 Å gate oxide and a 100 Å Ge_xSi_{1-x} well which lies underneath a Si spacer layer (see figure 1). The background doping is 10^{16} cm^{-3} n-type.

In Figure 3a. simulations of the hole density versus gate voltage for a device with a Si spacer thickness of 30 Å and a well with a Ge fraction of x=0.20 show that initially (after threshhold) the holes will predominantly be added to the Ge_xSi_{1-x} well up to a point, which we will call the "kink", where the rate of increase of holes at the Si-SiO_2 interface ($dp_{Si/SiO2}/dV_g$) equals the rate of increase of holes in the Ge_xSi_{1-x} well (dp_{GeSi}/dV_g). After this point the additional holes will be added predominantly to the inversion layer at the Si-SiO_2 interface instead of the Ge_xSi_{1-x} well. The slope of the total 2D hole density versus gate voltage will follow the slope of the hole density in the Ge_xSi_{1-x} well (dp_{GeSi}/dV_g) below the kink and the slope of the hole density at the Si-SiO_2 interface ($dp_{Si/SiO2}/dV_g$) above the kink. This is due to the fact that when the carriers are building up in the well they are further away from the interface and therefore gives the gate a smaller effective capacitance. Such a kink is one piece of evidence we can look for in a device to determine whether or not any carriers are building up in the Ge_xSi_{1-x} well.

Another important point on these curves is the point at which the number of holes in the Ge_xSi_{1-x} well equals the number of holes at the Si-

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SiO_2 interface. We will refer to this as the crossover point. One key to optimizing the structure is to have this cross-over point occur at the highest possible hole density, maximizing the number of carriers in the well where one hopes to have a higher mobility. In Figure 3b. one sees that the maximum number of holes confined in the Ge_xSi_{1-x} well decreases as the Si spacer width increases to 60 Å. Also, in Figure 3c. the number of holes in the Ge_xSi_{1-x} well increases due to the increase in Ge fraction from x = 0.20 to x = 0.40.

From the simulations of the total charge versus gate voltage one can also obtain low frequency capacitance-voltage curves (shown in figure 4). The plateau below C_{ox} in the inversion region corresponds to the build-up of holes in the Ge_xSi_{1-x} well (compare with figure 3). The transition from the plateau to C_{ox} represents the change in effective gate capacitance seen at the kink in the total holes vs gate voltage plots. These features are a second piece of evidence we can look for in an actual device to show that inversion is actually occuring in the Ge_xSi_{1-x} well.

EXPERIMENTAL RESULTS

The MOS-gated devices were epitaxially grown using a combination of rapid thermal processing and chemical vapor deposition. The temperature was stabilized prior to introduction of the deposition gases for each layer and continuously controlled using an IR transmission technique[5]. The Ge_xSi_{1-x} layers were grown at 600°C with dichlorosilane (Si source) and germane (Ge source) and the Si spacer layer was grown at 700°C. Source/drain implants were done with two boron (B^+) implants, one at 50keV and a dose of $2x10^{15}$ cm^{-2} and one at 25keV and a dose of $2x10^{15}$ cm^{-2}. The gate oxides were plasma deposited at 350°C and then annealed at 700°C for 30 minutes in N_2. (This also served as our implant anneal.) The gate metal is evaporated aluminum. During processing the thermal budget was held to a minimum to minimize relaxation of strain in the Ge_xSi_{1-x} layer and Ge outdiffusion.

A MOS capacitor was made for measurement of the high and low frequency C-V characteristics. The MOS capacitor was made on a sample with 40% Ge in the Ge_xSi_{1-x} well (100 Å) and a 75 Å Si spacer. The high frequency curves were well behaved (see Figure 5) and confirmed the gate oxide thickness. The low frequency measurements, made by the quasi-static method with a ramp rate of 800 mV/sec. (Fig 5), clearly show the plateau just below C_{ox} that indicates that holes are being added to the Ge_xSi_{1-x} well. The plateau is at a value of 106 pF which corresponds well with the estimated (from growth data) thickness of the Si spacer and corresponds well to our simulations of the structure (Fig 6). The transition from carriers being added to the Ge_xSi_{1-x} well to holes being added to the Si-SiO_2 interface occurs at a hole density of $2x10^{12}$ cm^{-2}, which is what we expect from simulations. By contrast a all Si control device displays no such plateau.

Curve tracer FET characteristics of a long channel device are well behaved (Figure 7), but this does not show whether or not the holes are confined in the Ge_xSi_{1-x} well or at the Si-SiO_2 interface. To prove the confinement a MOS gated van der Pauw device was made for Hall and van der Pauw measurements to obtain the hole density and the Hall mobility vs gate voltage. These measurements were done at 100 K with a ramped magnetic field to reduce noise. Figure 8 shows the hole density vs gate voltage for a device with 40% Ge (100 Å) and a 75 Å Si spacer. Note the kink in the curve indicates a change in the effective gate capacitance. At low gate voltages (below -4.2 volts) the effective gate oxide thickness is 142Å indicating that the holes are being added to the Ge_xSi_{1-x} well. Above a gate voltage of -4.2 volts the slope of the curve indicates that the holes are now being added at the Si-SiO_2 interface ($t_{ox,eff}$ = 104Å).

CARRIER CONFINEMENT OPTIMIZATION

Numerical simulations of a wide range of Ge fractions and Si buffer layer thicknesses were performed for MOS-gated heterostructures with a gate oxide of 100Å (no fixed charge or surface states) and a background n-type doping of 10^{16} cm^{-3}. The crossover point (where the number of holes in Ge_xSi_{1-x} well equals the number of holes at the Si-SiO_2 interface) was extracted and was plotted as a response of the combinations of Ge fraction and Si spacer thickness to obtain a series of "isohole" lines for the crossover point. The resulting plot is shown in Figure 9.

As noted earlier the maximum number of holes in the well before crossover increases as the Ge fraction increases and the Si spacer layer width decreases. The design that gives the maximum number of holes in the Ge_xSi_{1-x} well may not correspond to the device with the optimum FET performance however. This is because a small space width may lead to only a negligible reduction in the surface scattering and increase in mobility. Also the amount of Ge incorporated will be limited by processing constraints, to avoid relaxation of the strain in the layer.

SUMMARY

Numerical modeling and experiment show that it is possible to confine holes in a MOS-gated Ge_xSi_{1-x} - Si heterostructure device. This is confirmed by a kink in the carrier concentration vs gate voltage and a plateau in the inversion region of the low frequency C-V curve. Also, simulations have shown that it is desirable to employ a minimal Si buffer thickness

and a maximum Ge fraction to maximize the number of holes confined in the Ge_xSi_{1-x} well, subject to the constraints of surface scattering and processing considerations.

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[5] J.C. Sturm, P.V. Schwartz and P.M. Garone, Appl. Phys. Lett. 56 (10), 961 (1989).

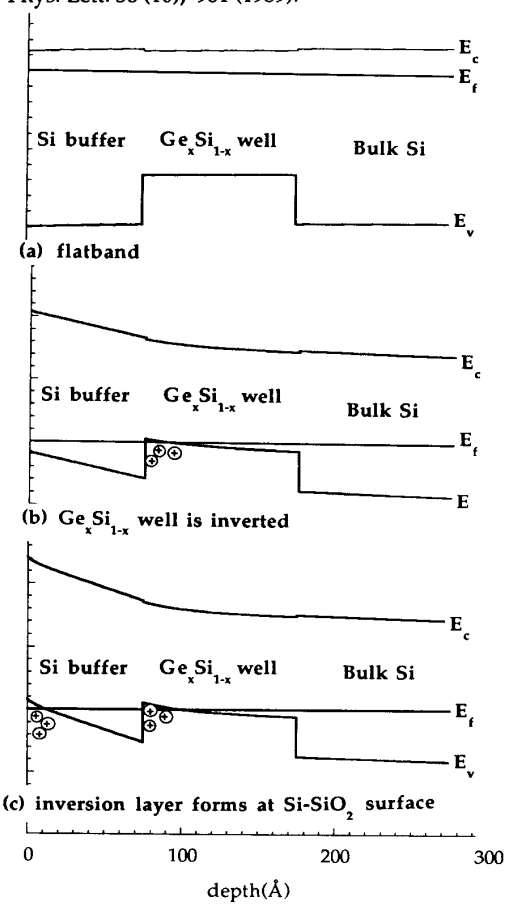

Figure 2: Band diagram near the surface of a MOS - gated structure with a 75Å Si buffer and a 100Å $Ge_{0.4}Si_{0.6}$ well.

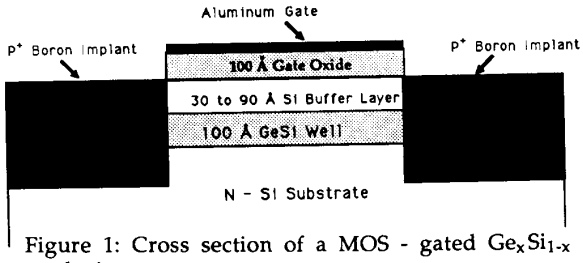

Figure 1: Cross section of a MOS - gated Ge_xSi_{1-x} device.

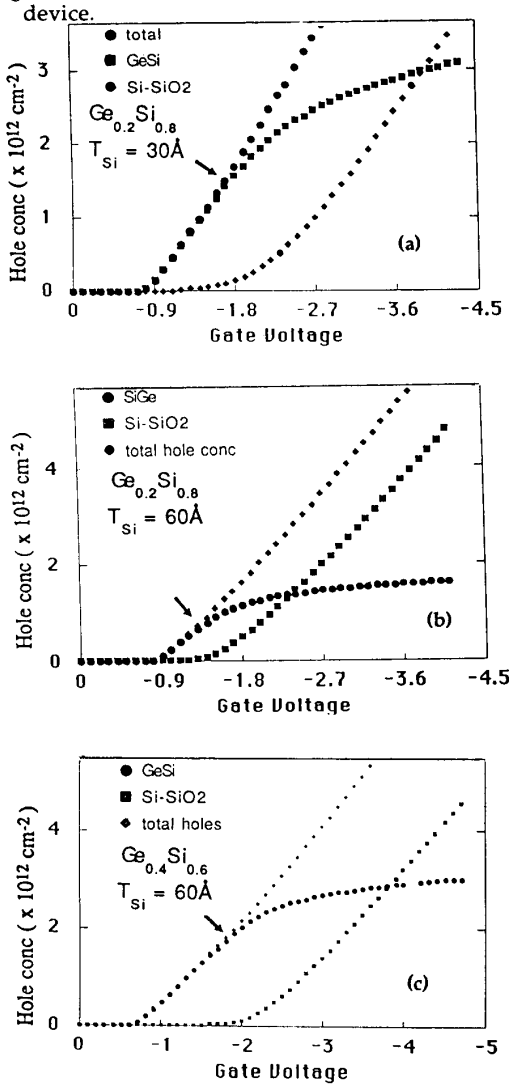

Figure 3: Simulated hole concentrations in the Ge_xSi_{1-x} well and at the Si-SiO_2 interface vs gate bias. Note the kink in the total holes curve as the new holes are added to the Si-SiO_2 interface rather than to the Ge_xSi_{1-x} well.

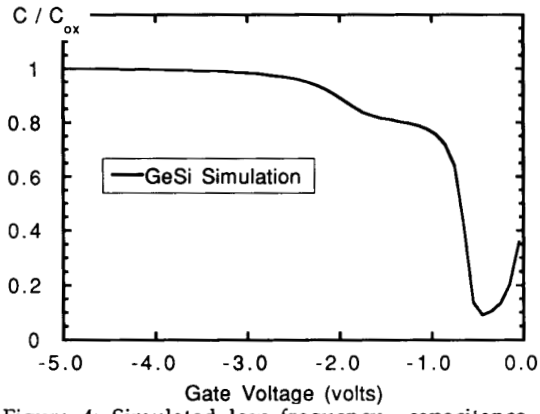

Figure 4: Simulated low frequency capacitance - voltage curve for a $Ge_{0.4}Si_{0.6}$ device with a 75Å Si spacer and a 106Å gate oxide ($N_f = 1.3 \times 10^{11}cm^{-2}$).

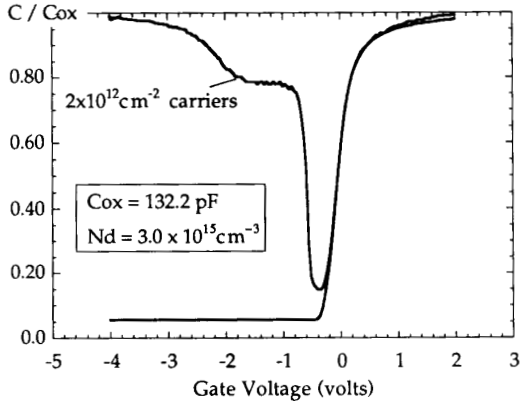

Figure 5: Low and high frequency (1MHz) capacitance voltage curves for a $Ge_{0.4}Si_{0.6}$ device with a 75Å Si spacer and a 106Å gate oxide.

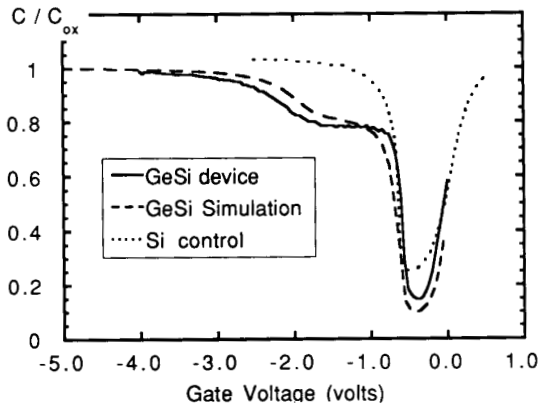

Figure 6: Comparison of the low frequency capacitance - voltage curve for a $Ge_{0.4}Si_{0.6}$ device with a 75Å Si spacer and a 106Å gate oxide to a simulation and a all Si control device.

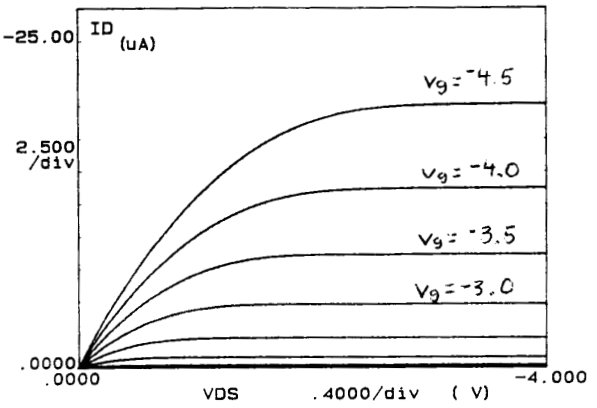

Figure 7: Operation of a long channel MOS - gated Ge_xSi_{1-x} device at room temperature.

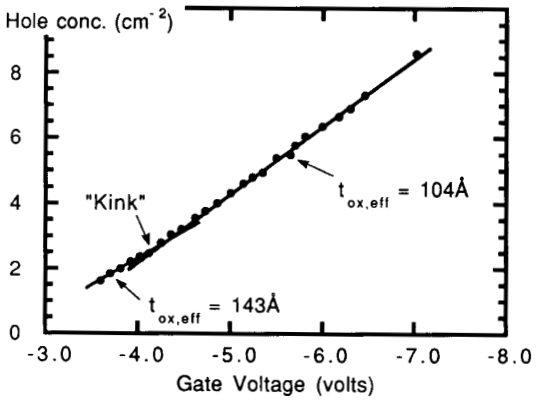

Figure 8: Hole concentration vs gate voltage from Hall measurements at 100K for a $Ge_{0.4}Si_{0.6}$ device with a 75Å Si cap and a 100Å gate oxide. Note that the kink at -4.2 volts ($p=2.5x10^{12}cm^{-2}$) represents the transition from adding holes to the $Ge_{0.4}Si_{0.6}$ well to adding holes at the Si-SiO_2 interface.

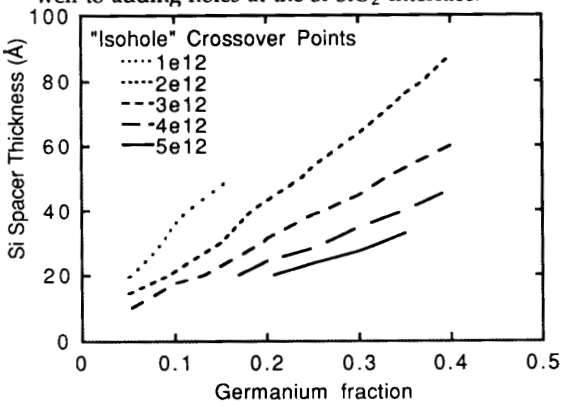

Figure 9: Hole confinement in the Ge_xSi_{1-x} well at crossover as a function of germanium fraction and Si buffer layer thickness.