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Interface Abruptness in Epitaxial Silicon and Silicon-Germanium Structures Grown by Rapid Thermal Chemical Vapor Deposition

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In this paper the combination of rapid thermal processing and chemical vapor deposition (CVD) is applied to the growth of silicon-based device structures with critical vertical dimensions on the order of 100's of Å . For the ultimate in interface abruptness, long times at low growth temperatures are favored over short times at high temperatures, but rapid temperature switching is still a desirable feature for optimizing the growth of individual layers. The interface abruptness in $Si/Si_{1-x}Ge_x$ stained layer structures grown at temperatures as low as 625 °C by RTCVD is then probed by electron transport in heterojunction bipolar transistors and two-dimensional hole gases. The results are consistent with an interface abruptness of ~10Å .

Introduction

The scaling of silicon device technology over the last 30 years has reduced typical vertical dimensions of critical features in the silicon from several microns to the order of 1000Å today. Such critical device dimensions are currently controlled by ion implantation. However, because of channeling, straggle, and the impracticality of fabricating heterojunctions, it is unlikely that ion implantation can produce vertical device dimensions scaled down a factor of 10 from current technology. Alternatively, this paper will apply the combination of rapid thermal processing and chemical vapor deposition to grow silicon and silicon-germanium device structures with layer thicknesses on the order of 100's of Å . The abruptness of interfaces in these layers will be inferred by observing the performance of heterojunction bipolar transistors and two-dimensional hole gases fabricated in these films. It will be shown that longer growth times at low temperatures are favored over short times at higher temperatures, and that rapid temperature switching is extremely useful when

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substrates had epi-substrate interfaces indistinguishable (by SIMS) from those of similar structures grown by MBE at 600°C. However, subsequent energy dependent SIMS measurements on i-p$^+$-i structures (doping level ∼5 x 10^{18}cm^{-3}) grown at 1000°C had a doping interface abruptness of about 80Å/decade for interfaces at a depth of ∼500Å [3]. Clearly such abruptness is not acceptable for the growth of device features on the 100Å scale. Using the actual growth rates of 0.2μm/min to establish times at growth temperatures, SUPREM process simulation indeed predicts similar interface abruptness without any excess time at the growth temperature. This clearly shows that even with rapid temperature switching, it will not be possible to grow structures at 1000°C with well-defined features on the 100Å scale.

Typical growth rate vs inverse temperature in our RTCVD reactor is shown in Figure 1. As expected, at high temperatures, growth is limited by mass transport, and at low temperatures surface reactions with an effective activation energy of ∼1.9 eV are the limiting step. Since typical activation energies for substitutional diffusion are 4-5 eV, diffusion will decrease faster than growth rates as the growth temperature is lowered. For example, using the growth rates of Fig. 1, SUPREM-III was used to simulate the growth of a doping superlattice (i-p$^+$-i-p$^+$) with alternating 100Å layers at 1000°C and 800°C, with no excess time at the growth temperature (Fig. 2). The improvement in interface abruptness at 800°C is clearly evident, with an abruptness of ∼10Å/decade at 800°C at a depth of 500Å. Therefore we can consider growth temperatures on the order of ∼800°C to be an upper limit for next generation devices.

At low growth temperatures, slower growth rates and longer growth times substantially reduce the motivation for using rapid switching of sample temperature to control the growth interval. For example, if growth of a 100Å layer at 700°C require three minutes, one extra minute at the growth temperature to stabilize the temperature will have only a minimal marginal effect on the interface abruptness in the final structure (contrasted to one minute at 1000°C for only a 10-second growth). To avoid potential problems with contamination of cold wafers between growth cycles and growth of low quality layers during temperature ramps up to the growth temperature, all samples described in the rest of this paper were not grown by controlling growth duration by temperature switching as in Limited Reaction Processing. Alternatively, after the high temperature hydrogen clean, growth was initiated by turning on appropriate source gases without cooling the sample to room temperature.

Because of three-dimensional growth tendencies and lattice strain, Si$_{1-x}$Ge$_x$ layers must be grown at a maximum temperature of 625°C for optimum

switching between layers with different optimum growth temperatures.

Experimental Apparatus

The experiments were all carried out on 100-mm silicon wafers suspended horizontally on quartz pins (no susceptor) in a horizontal quartz tube with a diameter of about 175 mm. The source gases were introduced into one end of the tube, and the other end was connected to a vacuum system pumped by a two-stage rotary vane pump. The gas supply and vacuum system are very typical of those of a conventional low-pressure polysilicon deposition system. The wafer heating was accomplished by a 70 KW-bank of tungsten-halogen lamps located outside the reaction tube. Because the quartz tube stays relatively cool, there is no deposition on the quartz tube, and only the wafer is heated. The sample temperature was determined either by first calibrating power cycles using a wafer with an internally welded thermocouple, or by monitoring the infrared transmission of the sample wafer in situ during growth [1]. After loading, all samples were cleaned in situ by a bake in hydrogen (1000-1200 °C) for 30s to 120s. All layers were grown at a pressure of 6.0 torr in a 3 lpm H_2 carrier with a dichlorosilane flow of 26 sccm. Germane (GeH_4) was added to the gas flow as a germanium source gas for the growth of $Si_{1-x}Ge_x$ layers.

Although the reaction chamber was vented to atmospheric pressure to load and unload samples, all samples grown at temperatures as low as 625 °C were single crystal with no dislocations, stacking faults, etc., evident in TEM micrographs. The surfaces of all wafers were specular with absolutely no "haze" or diffuse reflection observable in ultraviolet or visible light.

Growth Kinetics: High vs Low Temperature

One clear obstacle to growing structures with vertical features on the order of 100Å is thermal diffusion. Early experiments carried out in a rapid thermal CVD apparatus were described as Limited Reaction Processing (LRP) [2]. The central feature of LRP is to establish the gas flows while the wafer is cold, and then to use a rapid change in sample temperature (~300 K/s) to start the growth reaction. (This is contrasted to conventional CVD where the wafer temperature is established before reactive gases are turned on). A motivation for LRP approach is to minimize the time the wafer spends at high temperature to reduce thermal diffusion. With LRP, the wafer is only at high temperature during the growth itself and not before or after. Indeed, initial LRP results [2] of lightly-doped silicon epitaxial layers grown on heavily-doped

results [4]. Although the silicon growth rate in our system is only a few Å /min at 625 ° C, the growth rate for $Si_{1-x}Ge_x$ alloys can easily exceed 100Å /min because of the catalytic effect of germane on silicon growth [5]. Because the silicon growth rate in our reactor is unacceptably low at this temperature, it is useful to grow Si layers at 700 ° C or above, while $Si_{1-x}Ge_x$ layers are grown at 625 ° C. The ability to rapidly switch sample temperature is thus a valuable feature for the growth of multilayered samples containing $Si_{1-x}Ge_x$ layers.

Studying interface abruptness on the scale of 10's of Å is difficult since it is beyond the sensitivity of many analytical techniques. Instead, we have probed the interface abruptness by observing the electrical behavior of certain devices. The performance of $Si/Si_{1-x}Ge_x/Si$ narrow-bandgap-base npn heterojunction bipolar transistors (HBT's) and symmetrical 2-D hole gas structures will now be described.

Heterojunction Bipolar Transistors

Silicon npn bipolar transistors with a narrow-bandgap-base made of strained $Si_{1-x}Ge_x$ are an attractive candidate for high performance device technology [6]. The principle of such a structure is the increased electron emission into the base (and hence increased collector current) because of the reduced base bandgap. This increased emitter efficiency can be traded off to reduce base resistance and also used to decrease the turn-on voltage of the device. In the most straightforward device structure, a heavily-boron-doped p^+ $Si_{1-x}Ge_x$ base is sandwiched between lighter doped n-type emitter and collector regions. A potential problem with such structures is autodoping of minute amounts of boron from the $Si_{1-x}Ge_x$ into the Si emitter region, or thermal diffusion of boron into the emitter during the emitter growth. Such diffusion will move the metallurgical p-n junction into the silicon away from the heterojunction interface. Parasitic barriers in the conduction band will then be introduced which will impede the flow of electrons from the base to the collector, thereby degrading the device performance [7] (Fig. 3). Modelling the outdiffusion as a gaussian profile, for a base doping of $5x10^{18}cm^{-3}$, a diffusion length of only 20Å is predicted to have a substantial effect on the device performance. Such an outdiffusion would reduce the effective bandgap reduction in the base, $\Delta E_{G,eff.}$ (a figure of merit for the device), by roughly 20 meV. This deleterious effect can be reduced by placing undoped SiGe spacer regions between the emitter and the base so that the diffusion is contained within the SiGe base.

As an experiment, multilayer HBT structures were grown in-situ in our reactor. The structure consisted of an n-type Si collector grown at 850 ° C, a

p^+ $Si_{0.82}Ge_{0.18}$ base grown at 625°C, followed by an n-type Si emitter ($10^{17}cm^{-3}$) grown for 3 minutes at 850°C. Final transistor structures were then formed by a process that had a thermal budget small compared to the 3 minutes at 850°C. TEM confirmed that there were negligible dislocations in all samples. On some samples undoped SiGe spacers ($\sim100\text{Å}$ and up) were inserted between the n-emitter and p^+-base. Temperature dependent measurements of the ratio of collector current to that in similar homojunction transistors were then performed to determine the effective base bandgap reduction in the HBT's. (In Fig. 4, the slope is proportional to the effective bandgap reduction.) Samples with base dopings of $\sim10^{19}cm^{-3}$ had an effective bandgap reduction of $\sim$130-140meV, which did not depend on the presence of a spacer. Therefore one concludes that any outdiffusion of boron from the heavily-doped base in these samples was characterized by a diffusion length of less than 20Å. Another sample prepared with no spacers and a base doping of $\sim8\times10^{19}cm^{-3}$ showed an effective bandgap reduction of only 40-55meV. Computer modelling showed that because of the higher base doping, such a degradation can be explained by a boron diffusion length of only $\sim35\text{Å}$. Furthermore, SUPREM modelling predicts a thermal outdiffusion of this magnitude caused by the emitter growth cycle. Therefore it appears that the device degradation is consistent with thermal broadening of the interface, and there is no evidence for degradation of the interface due to mixing or slow gas transients when switching from one layer to another.

Two Dimensional Hole Gases

Because the bandgap discontinuity in strained $Si_{1-x}Ge_x$ on Si substrates lies primarily in the valence band, the fabrication of 2-D hole gases at a $Si_{1-x}Ge_x$/Si interface by modulation doping is in principle straightforward. If there are any transient delays related to switching source gases or surface segregation of dopants or germanium, one would expect 2-D hole gases with the SiGe alloy on top of the heavily-doped silicon to differ substantially from those with the heavily-doped Si over the SiGe. Because it is very sensitive to the doping and germanium profiles, the hole concentration is a useful parameter for comparing structures.

As an experiment, an undoped $Si_{0.8}Ge_{0.2}$ layer was grown at 625°C between two heavily-boron-doped ($3\times10^{18}cm^{-3}$) Si layers grown at 700°C (fig 5). The doped Si layers were separated from the $Si_{0.8}Ge_{0.2}$ layers by undoped Si spacers of $\sim50\text{Å}$ width. This symmetric structure should ideally form two identical 2-D hole gases, one at each SiGe/Si interface. However, because the 2-D hole density is very sensitive to the abruptness of the germanium profile, any diffusion of boron into the spacer, etc, one in practice rarely finds a symmetrical structure, even when grown by MBE [8]. For example, any latencies

caused by gas switching or surface segregation effects (of dopant or germanium) would yield an asymmetry in the structure. After growth aluminum alloying was performed to contact both 2-D gases in parallel, and the structure was probed by low-temperature Hall measurements. Low magnetic field measurements (Fig. 6) confirmed a 2-D gas as a constant hole density at low temperature is seen with the total number of carriers at both interfaces equal to 2.6 x $10^{12} \mathrm{cm}^{-2}$. High magnetic field measurements were then performed, and Shubnikov-de-Haas oscillations of the magnetoresistance vs magnetic field were observed. According to theory, the oscillation frequency depends only on the number of carriers in the 2-D gas. A single oscillation frequency in $1/B$ was observed by taking the fourier power spectrum of R_{xx} (Fig. 7). That one frequency is observed means that if two 2-D gases are present, both must have exactly the same carrier density. Further evidence of two identical gases is given by the fact that from the oscillation frequency one find a 2-D gas carrier density of ~1.3 x $10^{12} \mathrm{cm}^{-2}$, half of the low-field total carrier density (which thus consists of two identical 2-D gases.) Still stronger evidence is given by R_{xy} data exhibiting the quantum Hall effect (Fig 8). Simple theory predicts that the plateaus in resistance for a single gas are given by $R_{xy} = h/\nu e^2$, where ν is an even integer. As can be seen in Fig. 8, $\nu = 12,14,18,$etc. are missing from the data. This is because two identical channels in parallel will halve the measured resistance, so the measured R will be $h/2\nu e^2$.

Based on the observed symmetries in electrical measurements in our structure, an upper limit to asymmetry due to dopant profiles, interface abruptness, etc., of roughly 10Å can be estimated. Similar electrical results have been reported in structures grown at $\leq 550\,^\circ$C by the UHV-CVD technique [9]. Our structures were exposed to temperatures as high as $700\,^\circ$C, however, with no degradation in the quantum electron transport properties.

Conclusion

For the growth of next generation device profiles by direct epitaxial growth, growth temperatures on the order of $800\,^\circ$C or less will be required. At these lower temperatures the motivation to rapidly switch temperature to start and stop growth becomes less important, and conventional gas switching can be used. However, the ability to switch sample temperature remains very valuable for optimizing the growth temperature of each layer. Ideal performance of HBT's with simple box profiles is observed for base dopings $\leq$ $1 \times 10^{19} \mathrm{cm}^{-3}$, but for doping in the high $10^{19} \mathrm{cm}^{-3}$ range, degradation on the scale of 30Å is evident at $850\,^\circ$C. For structures grown at $700\,^\circ$C, ideally symmetrical 2-D hole gas structures have been grown, an ultimate test of interface abruptness and quality.

Acknowledgements

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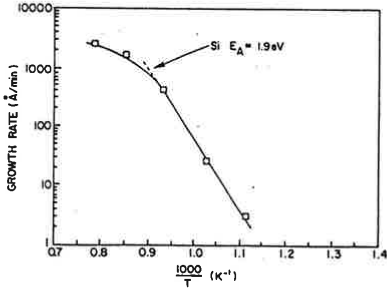
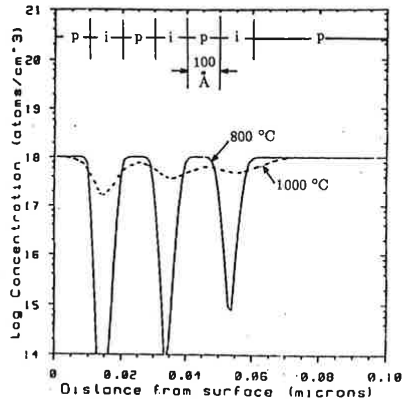Fig. 1. Silicon growth rate vs inverse temperature.

Fig. 2. SUPREM simulation of doping superlattice growth at temperature of $1000\,^\circ$C $(0.25\mu m/min)$ and $800\,^\circ$C $(0.02\ \mu m/min)$
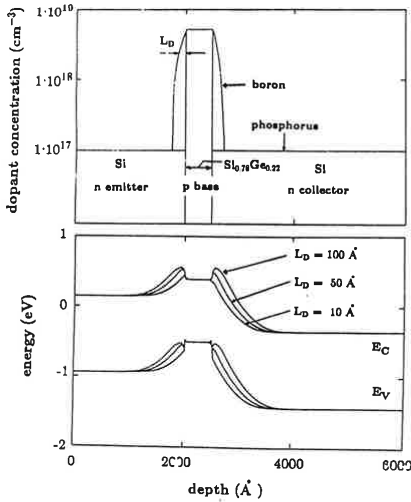

Fig. 3. Schematic view of boron outdiffusion in $Si/Si_{1-x}Ge/Si$ HBT structures and its simulated effect on band diagrams.
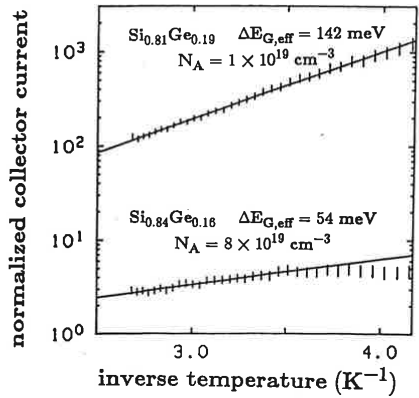

Fig. 4. Ratio of HBT collector current to homojunction collector current vs inverse temperature.

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p⁺ Sı	3 x 10¹⁸ /cm³ Boron	300 Å

p$^+$ Si	3×10^{18} /cm^3 Boron	300 Å
i - Si	spacer	50 Å
Si$_{0.8}$Ge$_{0.2}$	undoped	500 Å
i - Si	spacer	50 Å
p$^+$ Si	3×10^{18} /cm^3 Boron	300 Å
Si	buffer (undoped)	1 μm
n$^-$	substrate	

Fig. 5. Cross section of the two 2-D hole gas structure.
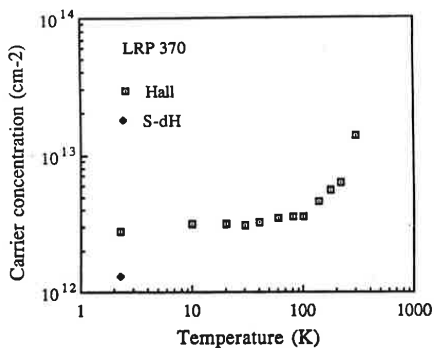
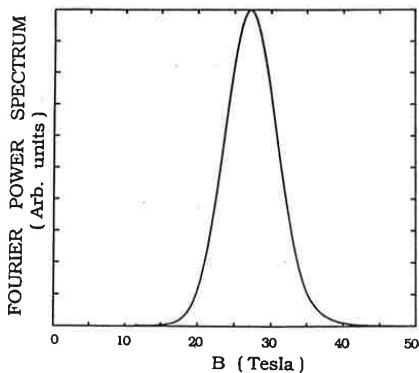Fig. 6. Hole density vs temperature from Hall and Shubnikov-de-Haas measurements.

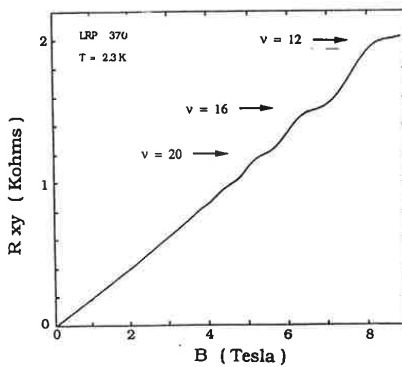Fig. 7. Fourier power spectrum of magnetoresistance R_{xx} from Shubnikov-de-Haas oscillations.

Fig. 8. R_{xy} of the quantum hall effect at 2.3 K. Plateau index ν is from R $= e^2/h\nu$.

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