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Beam-Solid Interactions and Transient Processes

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LIMITED REACTION PROCESSING

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ABSTRACT

Limited reaction processing (LRP), a new technique which provides precise control of thermally driven surface reactions, was used to grow multilayer structures composed of semiconductors and insulators. Results are presented for group IV-based materials including epitaxial Si, SiGe alloys, SiO_2, and polysilicon. III-V materials such as GaAs, AlGaAs, and InGaAs have also been successfully grown. A number of diagnostic techniques were used to define the advantages and capabilities of LRP, including TEM, SIMS and AES. In addition, some preliminary device results are presented.

INTRODUCTION

The fabrication of thin, high quality layers of semiconductor and insulator films is critical to the future of semiconductor processing. It is also of potentially great importance to be able to fabricate several films sequentially without removing the substrate from the processing chamber. This latter feature is important to minimize chemical and particulate contamination. Regarding the layers themselves, we want to maintain interfaces between layers that are as abrupt as possible, which generally argues for a minimum high-temperature exposure; and we want good intra-layer material quality and low defect interfaces, which argues for high temperature processing in many cases. The Limited Reaction Processing (LRP) technique was developed in an attempt to meet these objectives [1-4].

The Basic Process

It is convenient to think of the Limited Reaction Process as a technique that uses temperature rather than gas flow as a reaction switch. Conceptually, what we have is a CVD reactor of small volume that is driven by a source of high intensity, incoherent radiation that can be switched on and off quickly. The wafer being processed rests on three quartz pins and represents most of the thermal mass in the system, similar to a conventional RTA apparatus. Details of the chamber and related equipment are given in Ref. [1]. In a typical process sequence we first purge the chamber, then establish a carrier flow of inert gas and appropriate flows of reactive gases with the substrate at low temperature (unilluminated). We then raise the wafer temperature quickly (>300°C/sec) to the desired processing temperature, normally in the range of 1000°C, leave it there for the time required to achieve the desired layer growth, and then switch the light source off again. After the wafer has cooled, we switch off the reactive gases and purge the chamber again to set up the next cycle.

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The potential of such a system for semiconductor processing can be judged in terms of the quality of the layers that can be grown; the abruptness of the doping gradient between layers; and the interface characteristics that are achieved in a multilayer growth. In what follows we will use these broad criteria to examine results obtained in the growth of both column IV and III-V semiconductor compounds.

Epitaxial Silicon

We report first on our attempts to grow single crystal, epitaxial silicon on a silicon substrate. The substrates used for these experiments were (100) Si. Typically the wafers are chemically cleaned using an RCA process and then baked in H_2 (250 Torr) at 1150-1200°C for 20-60 sec directly before deposition.

The system was operated at a pressure of 1-10 Torr to reduce vertical autodoping, improve thickness uniformity, and allow single crystal deposition at relatively low substrate temperatures. Typical deposition temperatures were 850-1000°C for growth rates from .05-0.2 μ/min. Source gases were SiH_2 or $SiHCl_2$, and AsH_3 and B_2H_6 were used for doping.

Abruptness in the doping concentration was measured by growing an undoped film on an n+ (heavily antimony doped) silicon substrate. Secondary ion mass spectroscopy profiles are shown in Fig. 1 for samples grown by both MBE and LRP processes. In both cases the antimony concentration changes by two orders of magnitude (10^{16}-10^{18}/cm^3) over a distance of

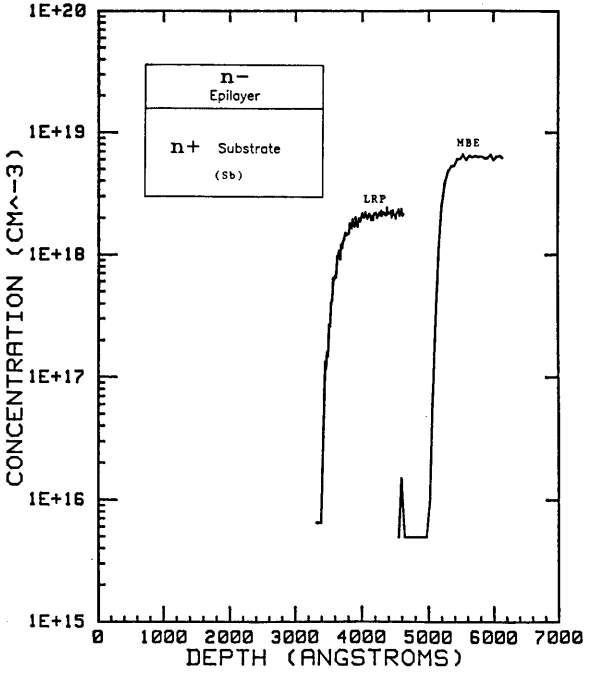


Figure 1. SIMS plots of Sb concentration vs depth for undoped epilayers deposited on an n+ substrate.

less than 30 nm. Hence the LRP process appears to provide an abruptness in doping concentration that is comparable to MBE, to within the resolution of SIMS.

The LRP epitaxial films were specular and indistinguishable from polished substrates when viewed under a Nomarski contrast microscope. Further electronic properties of these films will be described under later headings.

Multilayer Growth

A more rigorous test of such a system can be obtained by using it to grow multi-layer structures consisting of alternating undoped and heavily doped regions. Such structures were deposited in-situ by changing the gas composition between high temperature cycles. For these experiments, silicon was grown from a silane precursor at a pressure of 4.2 Torr in a hydrogen carrier flowing at 3 litres per minute. To introduce dopants, the hydrogen carrier was switched off and 5.2 ppm of B_2H_6 in H_2 was used.

A SIMS profile of a sample with two p+ regions is shown in Fig. 2. The p+ pulses with a full width at half maximum of 10 nm can be reproducibly grown [3]. The boron concentration can be observed to change four orders of magnitude over a distance of less than 40 nm (10 nm/decade).

Figure 3 shows a plot of the measured transition slope vs SIMS beam energy for the sample shown in Fig. 2 and one grown at 1000°C. In both

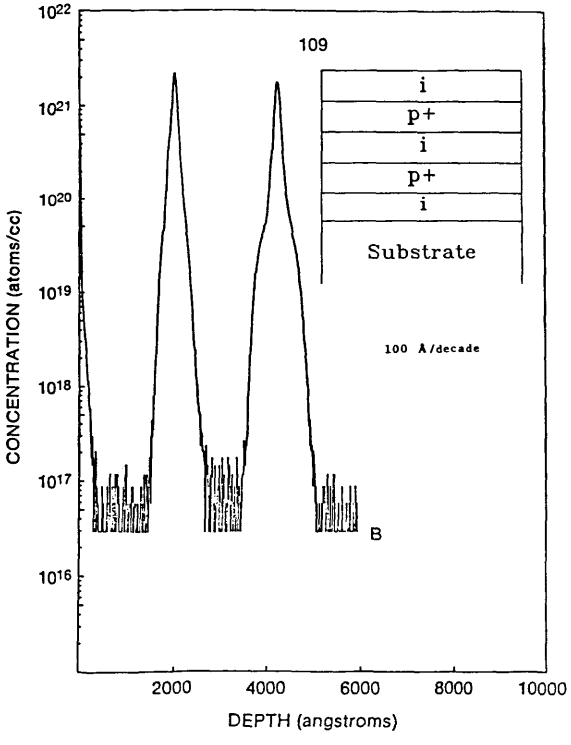


Figure 2. SIMS plot of B concentration vs depth for the LRP p+ multipulse structures shown in the inset.

cases the trailing edge is less abrupt because of knock-on by the SIMS oxygen sputtering beam. The lines can be extrapolated back to zero beam energy in order to eliminate the interface smearing caused by the SIMS technique, and thus provide a better estimate of the true transition slope of the doping profile [5]. Note that the trailing edge of the 1000°C sample does not intersect the leading edge at the ordinate, presumably because the trailing edge received a greater thermal exposure as this multilayer test sample was grown.

For electrical measurements, p+ layers having a thickness of .1-.5μ were deposited on n+ substrates. Van der Pauw measurements showed a sheet resistivity of 58 ohms/square and a hole mobility of 42 $cm^2/V\text{-}sec$. This value of mobility is comparable to that of bulk material with the same hole concentration.

By comparing the chemical concentration of dopant determined by SIMS with the hole concentration determined by spreading resistance, the degree of boron activation can be estimated. However, since the SIMS data are considered to be accurate only to about a factor of 2, the level of activation is difficult to determine with precision. The highest hole concentration measured was in the range of $2x10^{20}/cm^3$, whereas SIMS indicated significantly higher boron concentrations. Inactive boron is almost certainly present, the nature of which is currently being investigated.

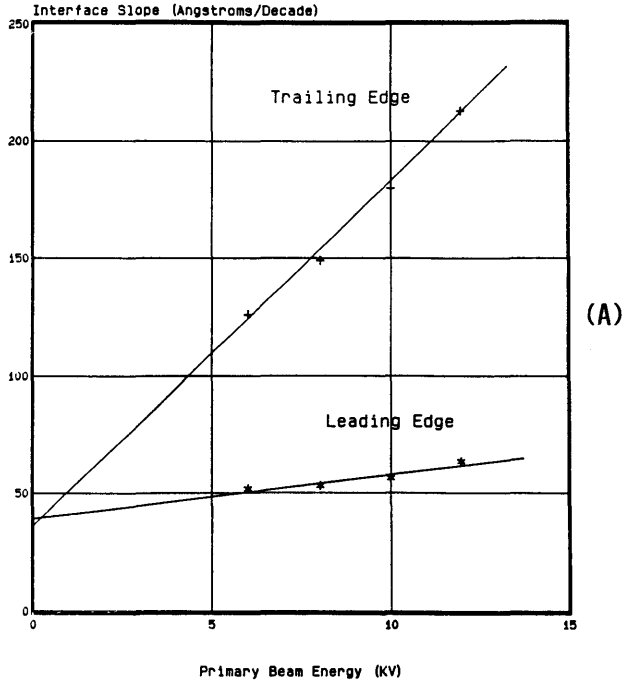
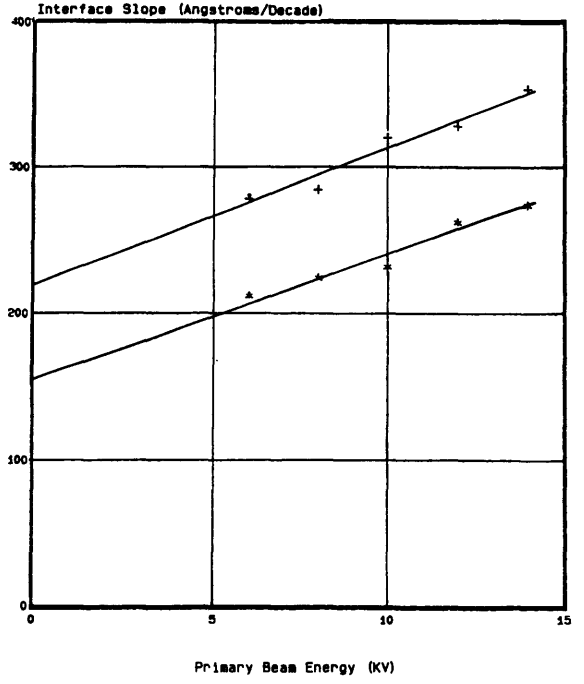


Figure 3. Plots of SIMS B transition slopes vs O_2+ primary beam energy. (a) LRP i/p+/i sample deposited at 900°C.

(b) LRP i/p+/i sample deposited at 1000°C



(B)

Si_xGe_{1-x}/Si superlattices have also been grown using the Limited Reaction Processing technique in which as before each layer of the multi-layer structure was fabricated in-situ by changing the gas composition between high temperature cycles. Commensurate SiGe alloy layers as thin as 15 nm were reproducibly deposited by this technique. Further details on such heterostructures are given in the paper by Gronet et al. [6].

Thermal and Mass Flow Uniformity

Figure 4 is a thickness map of a thin thermal oxide grown on a 4-inch Si wafer in the LRP chamber. This map can be used as a measure of thermal uniformity since the thermal oxidation of silicon is limited by a surface reaction and not mass flow. Using a 6-inch diameter Si ring placed around the 4-inch wafer to reduce edge effects, we can achieve an oxide thickness uniformity of ±3% on the central 3.0-inch diameter portion of the wafer.

To determine mass flow uniformity, we performed sheet resistivity measurements on a p-type epilayer deposited on an n-type substrate. Figure 5 is a map of sheet resistivity on a 4-inch wafer in which the major flat was aligned upstream in the LRP reactor. The increase in resistivity downstream is caused by both diborane and dichlorosilane depletion. SIMS measurements indicate that the film near the flat is 1.5 times thicker and has a born concentration 4 times higher than the epilayer on the other side of the wafer. We intend to improve this uniformity by increasing the flow velocity and tilting the water.

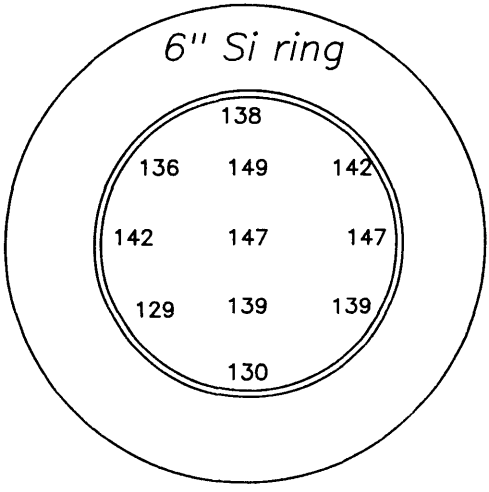


Figure 4. Thermal oxide thickness map of a 4" Si LRP wafer. A 6" diameter Si ring is placed around the wafer to improve temperature uniformity. The oxide was grown at ~1200°C, 500 Torr in dry oxygen. The perimeter values were taken <4mm from the wafer edge.

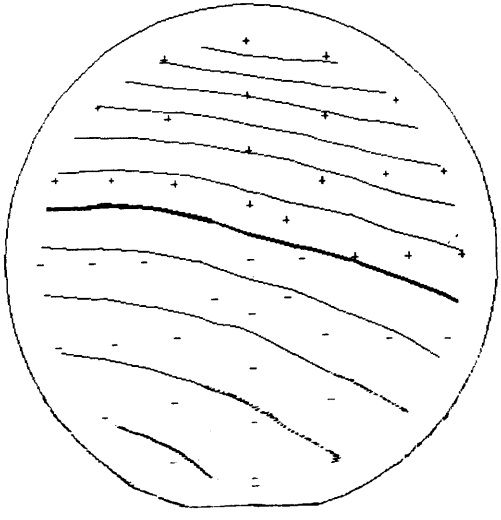


Figure 5. Sheet resistivity map for a p-type LRP Si epilayer deposited on an n-substrate. Each contour line corresponds to a 10% change. The resistivity increases across the wafer because of SiH_2Cl_2 and B_2H_6 depletion in the gas stream.

In Situ MOS Capacitors and MOSFETS

By changing the ambient gases between high temperature cycles from silane to oxygen, for example, thin layers of different compositions (oxides and polysilicon on a single crystal epitaxial film) can be grown in a single reactor without removing the sample from the processing chamber. Because the system is essentially a cold-wall reactor without a susceptor, only the wafer gets heated during a deposition or growth cycle. Thus "history" effects from one cycle to the next due to wall and susceptor deposition should be negligible.

A stringent test of such a system for practical application in MOS VLSI can be obtained from a study of the properties of MOS capacitors deposited in situ in an LRP chamber [4]. Oxidation was performed on an oxygen ambient with 4% HCl at a temperature of 1150°C in a pressure of 500 Torr. A typical oxidation time of .2 minutes yielded an oxide thickness of approximately 250Å. This oxide was capped in situ by a layer of LRP boron-doped polysilicon using SiH_4 at a substrate temperature of 580-600°C.

Conventional high and low frequency capacitance-voltage measurements were performed to measure the quality of the substrate silicon/silicon dioxide interface. From the high frequency curve, the oxide thickness, substrate doping, and interfacial fixed charge can be extracted. N_f was determined by this process to be $2x10^{11}/cm^2$, which is comparable to the current industrial state-of-the-art. The interface state density in the middle of the gap was determined to be $3x10^9/cm^2$ eV, which is again comparable to the state-of-the-art.

After the polysilicon deposition, one of the samples processed in situ received a further 1150°C, 15 second anneal in an argon ambient. It is well known that such anneals improve interface quality. With this anneal the fixed charge was reduced to $1\text{-}4x10^{10}/cm^2$. The breakdown field measured for the oxide by tunneling measurements was determined to be 10 MV/cm, the value expected for high quality SiO_2 films.

The quality of the MOS capacitors fabricated encouraged us to proceed with the fabrication of MOSFETS [7]. For these experiments a p-type epitaxial silicon layer was grown selectively through a previously prepared oxide hole onto a heavily doped silicon substrate. The primary source gases for this experiment were 7% SiH_2Cl2 and 2% HCl in an H_2 carrier. The HCl flow was chosen to achieve selective growth; i.e., to grow epitaxial silicon in the oxide holes but to avoid polysilicon deposition on top of the field oxide. For n-channel MOSFETS, 1.8μ of p-type epi was grown on a p+ substrate. 1.8μ of n-type epi was grown on an n+ substrate for p channel devices. The pressure during these epitaxial growth runs was 4.2 Torr, the wafer temperature was 925°C, and the growth rate was approximately 1μ/min. The epitaxial layer doping in both cases was approximately $5x10^{16}/cm^3$. The epitaxial layer grown by this process was roughly 3 times thicker than the field oxide. The detailed nature of the faceting at the edge of the epitaxial silicon surface was not investigated. Gate oxide and doped polysilicon layers were then grown and patterned with the gate being used as a self-aligned mask for implantation of source and drain wells. Rapid thermal annealing of the source drain implants was performed to minimize out-diffusion from the heavily doped substrates.

The n channel devices were found to have threshold voltages of 1.25 ± .05 V and electron surface mobility of 500 cm^2/Vsec. For the p channel devices we obtained a threshold voltage of -0.8 ± .05 V and a hole mobility of 120 cm^2/Vsec. In subsequent experiments on non-selective epitaxial layers we have achieved electron and hole mobilities in excess of 800 cm^2/Vsec and 200 cm^2/Vsec, respectively. The sub-threshold behavior of both types of devices was well behaved. Both n and p channel devices showed sub-threshold slopes of approximately 90 mV/decade. The source to substrate breakdown voltages for both types of devices ranged from

12 to 20 volts. Such breakdown voltages are consistent with the measured epitaxial layer doping.

III-V Compounds

In this section we report on the thermally switched growth of epitaxial layers of GaAs and related compounds. Layers of GaAs were grown with trimethylarsenic and trimethylgallium. We have also used the technique with equal success to grow $Al_xGa_{1-x}As$ ($0<x<.25$) and $In_yGa_{1-y}As$ ($0<y<0.1$), both on GaAs substrates. Good electrical characteristics and surface morphology, featureless to within the resolution of Nomarski microscopy (1100 X), have been consistently obtained. This technique maintains a growth rate of 10 Å/sec at atmospheric pressure while producing abrupt interfaces. The substrates used for these experiments were undoped and Si-doped Czochralski (100) material. These were degreased and given a 5:1:1 $H_2SO_4:H_2O_2:H_2O$ etch prior to loading. Layers were grown at 670 to 720°C with a 3.5 litre/min flow of H_2 carrier gas and a trimethylarsenic pressure of about 0.5 Torr. Gallium arsenide layers having n-type background doping in the range of $2x10^{16}/cm^3$-$10^{17}/cm^3$ and electron mobilities of 2500-3000 $cm^2/Vsec$ at room temperature were grown. We believe the high background doping is due to impurity incorporation from the trimethylarsenic, as has been reported [8]. Trimethylarsenic was selected on the basis of safety; we believe that superior films could be grown with arsine.

For the growth of III-V compounds, the wafer rests on a thin (20 mil) graphite susceptor which is heated from the underside by a bank of high power tungsten halogen lamps, as in a rapid thermal annealer. Temperature is measured with a thermocouple inserted down a 2mm outer diameter sealed quartz tube in contact with the susceptor (Fig. 6). We believe that supporting this sample on quartz pins alone and measuring temperature with an optical pyrometer would improve this technique by reducing thermal rise and fall times. To date wall deposition prevents this from being a useable strategy.

As was the case for silicon, a critical test of such a system lies in its ability to grow multi-layer compound heterostructures with abrupt interfaces. In Fig. 7, we show a process timing diagram for the growth of a $GaAs/Al_xGa_{1-x}As$ multilayer structure. Figure 8 is an Auger depth

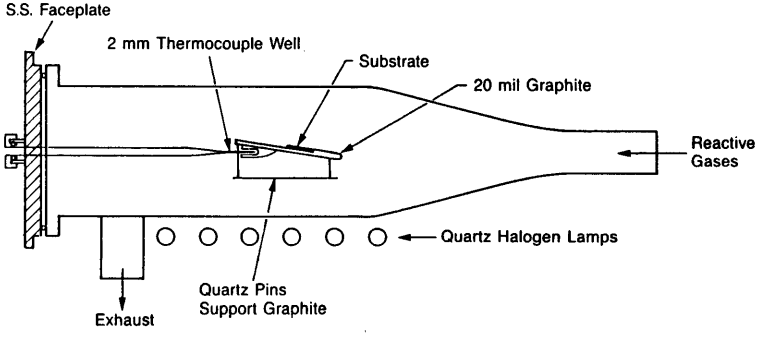


Figure 6. Schematic drawing of the quartz reaction chamber used in our experiments. The wafer sits on a low thermal mass graphite susceptor and temperature is monitored by a thermocouple sheathed in a 2 mm outer diameter quartz tube.

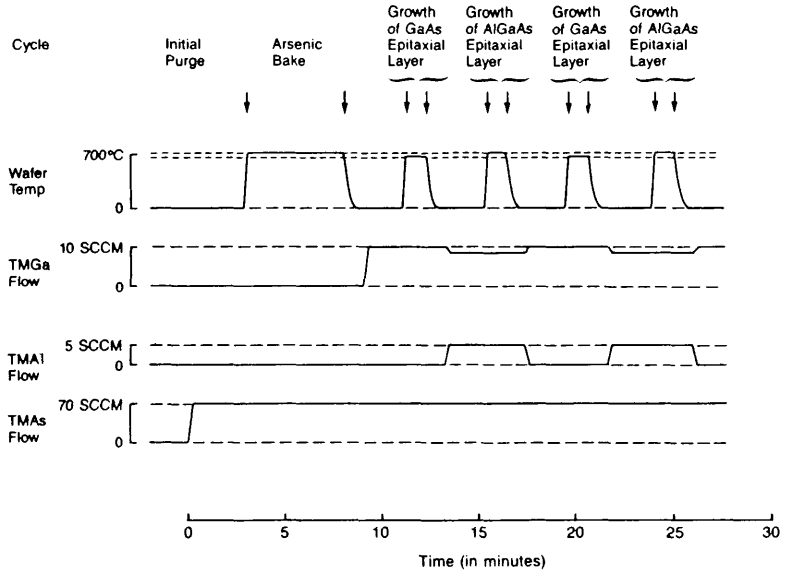


Figure 7. LRP process timing diagram showing how layers are grown by pulsing the wafer temperature in the presence of the correct reactive gases.

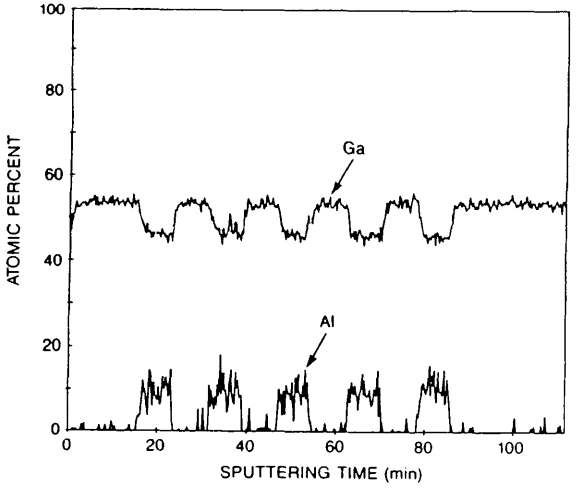


Figure 8. Sputtering Auger profile for sample 135 showing a structure of alternating GaAs/$Al_{.12}Ga_{.88}$ As layers. Total thickness is about 6000 Å. Aluminum scaled by 2 (Charles Evans & Associates, Redwood City, CA).

profile of the resulting epitaxial layers. The GaAs was grown at 670°C and the AlGaAs at 720°C, these temperatures giving the best mobility and surface morphology for single layers of each material. We have grown from 3 to 11 layers of this type with layer thicknesses of 300Å to 2500Å by simply repeating a sequence of rapid thermal steps. The structures have excellent surface morphology and electrical characteristics equivalent to single layers grown by conventional MOCVD in our reactor. Rutherford backscattering and ion channeling analysis shows no evidence of crystal defects at the interfaces. Minimum channeling yields are about 4%, the same as bare GaAs wafers.

The microstructure of the $Al_xGa_{1-x}As$ superlattice was investigated with high-resolution transmission electron microscopy (HRTEM). Direct crystal lattice imaging was performed on the <100> zone axis. As may be seen in Fig. 9, the layers are planar with well defined interfaces and no observed defects. The image contrast at layer interfaces is confined to a two monolayer thickness. Lattice continuity is not disrupted. The origin of the image contrast is not known, but it may be due to carbon contamination or slight interfacial stress. Layer thickness calibrated with (100) lattice fringe spacings are 450Å for the $Al_xGa_{1-x}As$ layers and 340Å for the GaAs.

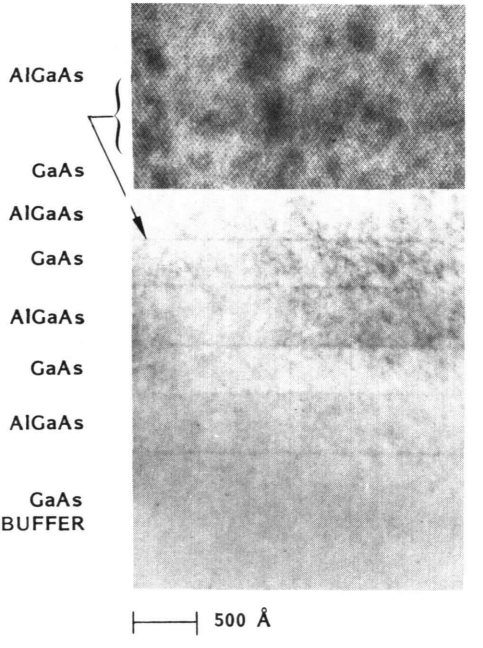


Figure 9. Lattice image Transmission Electron Micrograph of a GaAs/$Al_{.12}Ga_{.88}As$ multilayer structure. The inset shows that layers are abrupt to within 2-3 atomic planes.

SUMMARY

High quality epitaxial films of Si on a silicon substrate have been grown using the LRP technique. Doping abruptness, defect density and foreign atom precipitation are acceptable for demanding VLSI applications. Selective silicon epitaxy has also been achieved using HCl and SiH_2Cl_2 in the gas stream; and epitaxial growth of Si_xGe_{1-x} alloys has also been achieved. MOSFET structures have been fabricated with the critical layers grown in-situ without removing the substrate from the reaction chamber.

GaAs, $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ have also been grown on GaAs from TMAs, TMGa and TMAl precursors. These layers show good crystalline quality but have reached impurity levels that are somewhat higher than desired (mid-10^{16} to 10^{17}). This is currently believed to be due to impurities introduced from the trimethyl source gases.

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