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ELECTRON-BEAM-INDUCED-CURRENT (EBIC) IMAGING OF DEFECTS IN $Si_{1-x}Ge_x$ MULTILAYER STRUCTURES

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ABSTRACT

The electron-beam-induced-current (EBIC) technique has been used to image dislocations and other defects at strained Si: $Si_{1-x}Ge_x$ epitaxial interfaces and in overlying epitaxial layers grown by Limited Reaction Processing. Depending upon the bias conditions and test structure, one can distinguish between interface defects and those in overlying films. We have found that for a low density of misfit dislocations, a high quality (defect-free) overlying epitaxial layer can be grown, but for a high density of dislocations certain line defects propagate upwards in the overlying layers.

INTRODUCTION

The commensurate $Si_{1-x}Ge_x$ strained layer system on silicon substrates has received considerable attention in the last few years as a possible material system for high quality heterojunction devices on silicon substrates. The larger natural lattice constant of the $Si_{1-x}Ge_x$ layers results in misfit dislocations at the interface if the strained layer is thicker than some "critical thickness." [1,2,3] Knowledge of the presence of dislocations is very important since the bandgap of the $Si_{1-x}Ge_x$ depends on the the strain [4], and the dislocations can serve as minority carrier recombination sites. This critical thickness is strongly dependent on germanium fraction x, growth temperature, substrate preparation, and other experimental factors. Transmission electron microscopy (TEM) can be used to detect the presence of dislocations and has excellent resolution, but generally only samples an area of several square microns.

The electron-beam induced current technique monitors the minority carrier charge generated by a scanning electron beam that is collected by a nearby blocking contact (typically a Schottky barrier or a p-n junction.) When the carriers are generated close to a defect, a large number will recombine, and fewer will be collected by the contact. By displaying this collected charge as a function of position, one can thus map out an image of the defect structure [5,6].

The EBIC technique has been previously applied to single $Si_{1-x}Ge_x$ layers grown on silicon substrates to determine critical thickness for various germanium fractions [7]. Our work has focussed on a multilayer structure of Si substrate:$Si_{1-x}Ge_x$:Si as one would use for a narrow gap heterojunction bipolar transistor [8].

SAMPLE GROWTH AND PREPARATION

The samples were grown by a modified version of the Limited Reaction Processing technique [9]. The growth combines the

versatility of gas sources (chemical vapor deposition) with rapid
control of the sample temperature (rapid thermal processing).
The growth chamber itself consists of a 17-cm diamter quartz tube
exhausted by a mechanical roughing pump. A single four-inch
wafer is heated without a susceptor by a bank of
microprocessor-controlled tungsten halogen lamps.

The samples grown for these experiments consisted of a
single layer of $Si_{0.78}Ge_{0.22}$ sandwiched between a silicon (100)
substrate and an epitaxial silicon cap of 1.3 um thickness (fig.
1). Three different samples were grown,each having a different
$Si_{0.78}Ge_{0.22}$ thickness. After sample loading and an initial high
temperature bake in hydrogen for surface cleaning (1200 C, 30 s),
silicon buffer layers were grown at 1000 C and then 900 C (0.4 um
each) at 6.0 torr using dichlorosilane as the source gas in a
hydrogen carrier. The temperature was then changed to 625 C, and
the $Si_{0.78}Ge_{0.22}$ layers were grown using a combination of
dichlorosilane and germane as sources. Growth rates and the
germanium fraction were measured by calibrated SIMS on samples
grown under identical conditions as these just before and after
these samples. The accuracy of the germanium fraction is thought
to be +/- 0.01, and accuracy of the layer thickness +/- 10%. The
three samples were grown with a $Si_{0.78}Ge_{0.22}$ thickness of 0.17 um,
0.34 um, and 0.69 um, respectively. The growth rate of this
layer was approximately 10 nm/min. After these layers, a top cap
of 1.3 um of Si was grown at 800 C at a rate of 40 nm/min. None
of the layers was intentionally doped, but this generally
results in n-type layers in our reactor with doping levels on
the order of $10^{16} - 10^{17}$ cm^{-3}.

EBIC structures were then formed by evaporating Pd dots of
40 nm thickness. This thickness was chosen to be transparent to
high energy (30 KeV) electrons. Simple measurement showed that
the Pd formed a Schottky barrier to the Si, and that the Si was
n-type. Thus the Schottky barrier would collect minority carrier
holes in an EBIC experiment. Capacitance measurements showed the
Schottky barrier depletion width to be about 0.3 um, much less
than the top Si thickness of 1.3 um. Attaching bond wires and
mounting in a header completed the fabrication.

RESULTS

EBIC measurements were performed using an electron energy
of 20 to 30 KeV and a current on the order of 100 nA. Images
from the three samples of varying $Si_{0.78}Ge_{0.22}$ thickness are shown
in figure 2. The sample with the $Si_{0.78}Ge_{0.22}$ thickness of 0.17
um shows no defects. (The few marks on the sample were a result
of processing.) The next thickest sample (0.34 um) showed many
extended defects running in <110> directions, with an average
spacing of about 10 um. Finally, the thickest sample (0.68 um)
showed a larger defect density, with an average spacing on the
order of microns. The defect structures imaged by EBIC were in
one-to-one agreement with surface features seen in the samples
with phase contrast optical microscopy. A few volts reverse bias
yielded no qualitative change in the images. At larger (>5 V)
reverse bias, noise made imaging impractical. A micrograph of
the 0.17 um sample showed no surface features at all, even after
a light defect etch. The thicker samples had an optically
visible cross-hatched pattern (fig. 2d) which is commonly
associated with misfit dislocations. The features were visible
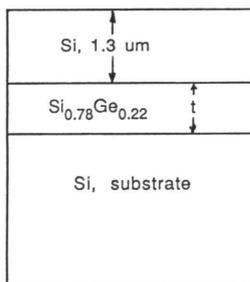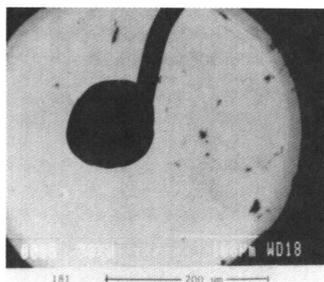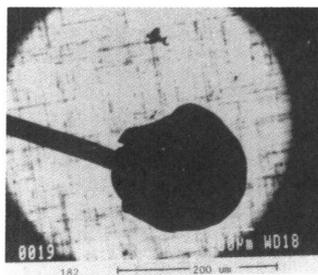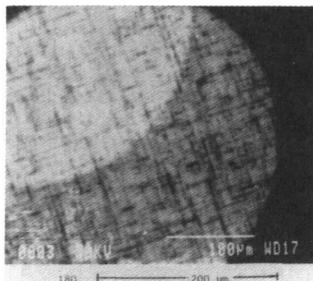without any defect etching, and were measured with a stylus

Fig. 1.   The test structures used in these experiments.
The middle $Si_{0.78}Ge_{0.22}$ layer was 0.17 um, 0.34 um,
and 0.69 um in the three samples, respectively.
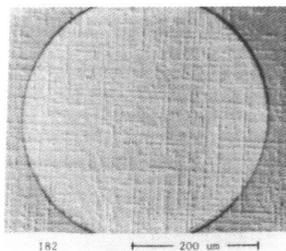

(a)

(b)

(c)

(d)

Fig. 2.   Zero-bias EBIC images for the 0.17 um sample
(a), the 0.34 um sample (b), and the 0.69 um sample
(c).   In (d), an phase contrast optical micrograph
of the 0.34 um sample is shown.

profilometer to be about 50 nm in height.

The data presented so far is consistent with a straightforward interpretation that the 0.17 um layer is thinner than the critical thickness for a x=0.22 Ge fraction, and that the thicker layers were over this critical thickness and hence had dislocations. However, it is generally accepted that the critical thickness for $Si_{0.78}Ge_{0.22}$ on Si, although somewhat dependent on growth conditions, is on the order of 50 nm, much less than necessary to interpret our results.

To investigate this anomaly, we etched away approximately half of the top Si cap (down to ~0.6 um) on an unused piece of the 0.17 sample by careful plasma etching. Schottky barrier structures were then fabricated as before. EBIC measurements with no bias on these structures showed no defects as in fig. 2 (a). A reverse bias was then applied to the Schottky barrier to extend the Schottky barrier depletion region to the $Si_{0.78}Ge_{0.22}$:Si interface. Under such bias conditions, extended line defects (presumably misfit dislocations) were seen, with a spacing on the order of 10 um (fig 3). Plan view TEM measurements performed on the sample also showed line defects, although with a spacing a factor of 10 closer. This discrepancy could be caused by the very varible spacing of dislocations within a sample and the small area sampled by TEM (about 2 square microns in this case), or could result if some dislocations were not electrically active (and hence gave no EBIC signal.) In any case, these measurements confirm that dislocations are present in the structure, and that the critical thickness is less than 0.17 um, consistent with other work reported in the literature.

DISCUSSION

The EBIC technique depends on the recombination at defects affecting the current collected by the Schottky barrier, as is the usual case with minority carriers diffusing in a uniform piece of semiconductor. However, in the strained $Si_{0.78}Ge_{0.22}$:Si system (on Si substrates), a discontinuity on the order of 200 meV is expected in the valence band [4]. Therefore, in our original EBIC structures, any hole at an interface between the SiGe and the Si would tend to get trapped in the narrow gap SiGe alloy. Very few could make it to the Si cap to be collected as an EBIC signal, regardless of the presence of defects at either interface. Simple thermionic emission over a 200 meV barier predicts a reduction of the signal by a factor of over 1000. This would explain the absence of defects in the image of fig 2(a). (See fig 4(a).) When the top Si layer was thinned and the Schottky barrier was reverse biased, the electric field from the surface extends down to the top SiGe:Si interface. With the help of this electric field, apparently holes can now aquire enough energy to get into the top Si to be collected. Thus the pattern becomes sensitive to the presence of defects (fig 4 (b)). From this one can conclude that when performing EBIC on heterojunction structures, for best imaging the minority carrier collector should be placed on the low gap side of the junction so that the flow of minority carriers is not impeded.

Since the initial probing conditons of fig 2 do not sample defects at the interfaces, the defects seen in these tests must now be in the top Si film. To confirm this, the sample of fig.
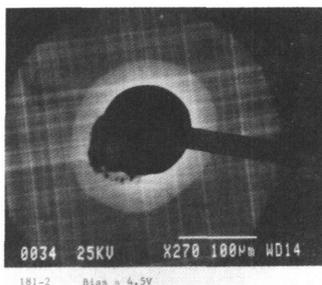
Fig. 3. EBIC image of the 0.17 um sample after thinning and with a bias of 4.5 V.
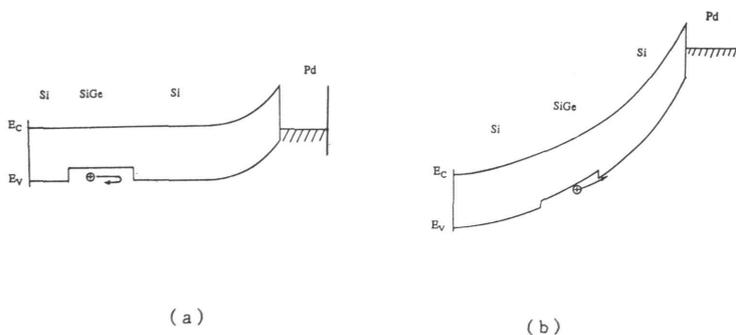

(a)

(b)

Fig. 4. Band diagrams of the samples with no bias (a), and with a 4.5 V reverse bias (b).
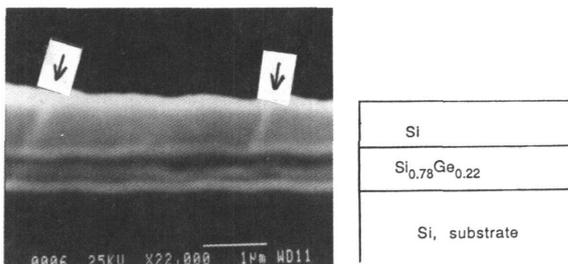

Fig. 5. Cross sectional SEM of the 0.69 um sample after defect etching. Note the defects threading through the top Si film.

2(c) was cleaved and given a brief defect etch. The cross section was then viewed in an SEM (fig 5). The top Si and SiGe regions are clearly visible. Corresponding to each line defect on the top surface, a defect extending from the surface down to the SiGe layer was observed. This defect is apparently that which gave rise to the recombination observed by EBIC in figures 2(b), 2(c). Although the nature of this defect is not known, it can be assumed that it originated at one of the SiGe:Si interfaces because of the misfit dislocations. However, while dislocations were present in the thinnest (and thus presumably all) of the three samples, no defects extended into the top epitaxial Si of the first sample.

Thus, under our growth conditions, the criteria for defects in overlying epitaxial layers is considerably less stringent in terms of critical thickness than that for misfit dislocations at the interface. The absence of a cross-hatched pattern (indicative of no defects in the top epitaxial layer) is not a sufficient condition to infer an absence of misfit dislocations at the heteroepitaxial interfaces. This may be related to the fact that several types of dislocations to relieve strain have been found at Si:SiGe interfaces [1,2,3,7]. Some may lead to overlying defects while others may not.

CONCLUSION

EBIC can be a useful tool for looking at misfit dislocations in heteroepitaxial structures over a large area. However, one must be careful to insure that minority carriers at the heteroepitaxial interfaces may be collected. In $Si_{0.78}Ge_{0.22}$ structures, it appears that a certain amount of strain at interfaces may be accomodated by misfit dislocations without defects propogating upwards into overlying epitaxial layers. This is encouraging for the growth of defect-free "virtual" substrates.

ACKNOWLEDGEMENTS

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