MATERIALS RESEARCH SOCIETY
SYMPOSIA PROCEEDINGS

VOLUME 52

Rapid Thermal Processing

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MRS

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Symposium held December 2-4, 1985, Boston, Massachusetts, U.S.A.

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MRS MATERIALS RESEARCH SOCIETY
Pittsburgh, Pennsylvania

Materials Research Society Symposium B, Boston, MA, Dec. 2-4,1985
Proc. Vol. 52, pp. 305-312

LIMITED REACTION PROCESSING OF SILICON: OXIDATION AND EPITAXY

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ABSTRACT

Limited reaction processing has been used to grow thin, high quality layers of epitaxial silicon, silicon dioxide, and polycrystalline silicon. Multiple layers of these materials were deposited *in - situ* to demonstrate control of layer thicknesses, interface transition regions, and interface cleanliness. MOS and p-n junction structures were fabricated which exhibit electrical characteristics comparable to those of devices produced by conventional techniques.

INTRODUCTION

As integrated circuit dimensions continue to shrink, new processes must be developed to produce ultra-thin layers of semiconductors and insulators as well as highly-controlled doping profiles. A key characteristic of these new processes must be a method of minimizing total thermal exposure, for dopant diffusion and interface broadening must be kept well below the thickness of individual layers. These requirements are complicated by the need for high temperatures to obtain certain material characteristics. For example, dopant activation, crystalline quality of CVD layers, quality of Si/SiO_2 interfaces, silicide resistivity, and glass reflow are all factors which benefit from high temperatures.

Because of the problem of thermal loading, standard furnaces cannot heat and cool wafers quickly enough to keep thermal exposure below a tolerable value. Single wafer rapid thermal processing has emerged as a technique for achieving fast changes in the temperature of a semiconductor substrate.

We introduce a new technique, limited reaction processing (LRP), which employs rapid thermal processing to control thermally driven surface reactions. Radiant heat is used to produce large, yet rapid changes in the temperature of a semiconductor substrate. The substrate temperature, rather than the flux of a reactive gas, is used as a "switch" to turn a CVD or surface reaction on and off. The substrate is hot only while a deposition or surface reaction is occurring, not during purging, gas flow stabilization, and other process steps. Thus, inherently, the thermal exposure of the substrate is minimized, reducing the broadening of interfaces by diffusion and intermixing. Moreover, by changing the ambient gases between high temperature cycles, multiple thin layers of different composition can be grown sequentially without removing the substrate from the processing chamber, thus reducing the possibility of surface contamination. A type of single-layer LRP, rapid thermal oxidation of silicon, has been demonstrated previously [1].

This work focuses on the use of LRP to fabricate multilayer silicon-based structures with excellent interface and electrical qualities. Specifically, LRP has been used to grow layers of undoped and doped epitaxial silicon, thermal silicon dioxide, and polysilicon. The ability of LRP to produce abrupt doping profiles, high quality ultra-thin layers with excellent thickness control, and *in - situ* multilayer structures is demonstrated. MOS and p-n junction devices were fabricated to characterize the electrical properties of LRP layers.

EXPERIMENTAL

The limited reaction processing chamber is shown schematically in Figure 1 [2]. The substrate is rapidly heated by two banks of six air-cooled 1.2 kW tungsten lamps backed by water-cooled reflectors. These lamps irradiate both sides of a two inch diameter silicon substrate mounted on three quartz pins. To calibrate the wafer temperature for a given lamp power vs time program and sample ambient, a W/26% Re vs W/5% Re thermocouple was electron-beam welded to the center of a test

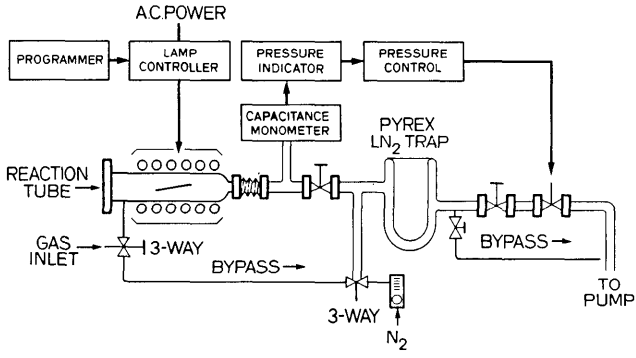

Fig. 1 LRP apparatus.

wafer. Substrates used for the actual growth of films did not have a thermocouple attached. Calibrations were performed often and were very reproducible (run to run variation <20°C). Temperature uniformity was established by growing a thin thermal oxide (10 - 60 nm) and measuring thickness uniformity using ellipsometry. The variation in oxide thickness over a 2.5 x 2.5 cm square centered on a two inch wafer was less than 3%.

EPITAXIAL GROWTH OF SILICON: UNDOPED LAYERS

Materials Properties

As device geometries shrink, many integrated circuit technologies will require very thin (0.2 - 1.5 μm) lightly doped silicon layers on top of heavily doped substrates. Thus, we attempted to grow undoped layers of epitaxial silicon on heavily doped (100) and (111) silicon wafers (less than 0.02 Ω-cm)[1]. Prior to deposition, *in-situ* rapid thermal pre-cleaning was performed. Typically, the wafers were heated in H_2 to 1150 °C for 30-120 seconds. The effectiveness of shorter cleaning steps is being investigated to reduce both dopant evaporation from the substrate and dopant redistribution in the substrate or underlying layers.

Undoped silicon was deposited using SiH_2Cl_2 or SiH_4 at 850 - 1050 °C and 0.5 - 10 torr. Growth rates ranged from 0.1 - 1.0 μm/minute. Low pressures were used to reduce vertical autodoping [2], improve thickness uniformity, and allow single crystal deposition at lower substrate temperatures [3].

Compared to standard epitaxial processing, very short yet well-controlled deposition times can be achieved using LRP, allowing the fabrication of ultra-thin films with abrupt doping profiles at the epitaxial layer/substrate interface. Typical secondary ion mass spectroscopy (SIMS, Charles Evans and Associates) profiles for samples LRP 59 and LRP 64 are shown in Figure 2. The Sb concentration changes two orders of magnitude (10^{16} cm^{-3} to 10^{18} cm^{-3}) over a distance of less than 30 nm. A similar sample deposited by molecular beam epitaxy (MBE) was measured using identical SIMS conditions and shows a transition width (for the same change in Sb concentration) of 15 nm.

The LRP epitaxial films were specular and indistinguishable from polished substrates when viewed under a Nomarsky contrast microscope. Films were deposited between 0.1 μm and 3.0 μm thick. The crystalline quality was studied using Rutherford backscattering channeling spectra. The minimum yields for all samples was between 2.7% and 3.0%, indicating excellent crystalline quality [4]. Further investigations using cross-section transmission electron microscopy are in progress.

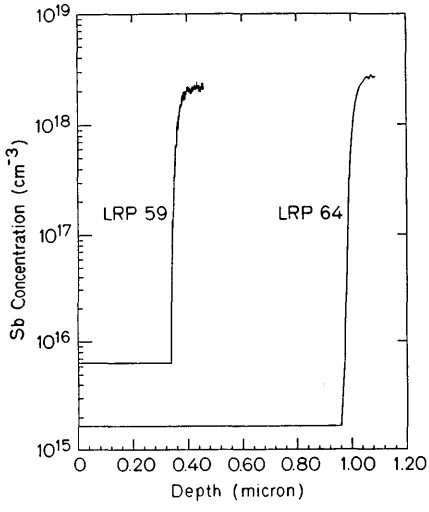

Fig. 2 SIMS profiles of undoped LRP epitaxial silicon deposited on n^+ Sb substrates (Charles Evans and Assoc.).

Electrical Properties

Generation lifetimes and diode properties were measured in undoped (n^-) and lightly boron-doped LRP epitaxial silicon films. Such properties are very sensitive to the quality of semiconductor layers.

Epitaxial films grown for electrical measurements were 2 -3 μm thick with carrier concentrations on the order of 5 x 10^{16} cm^{-3}. Unintentionally doped n-type films were deposited on n^+ Sb substrates, while B_2H_6 was added to the sample ambient to deposit p-type films on p^+ substrates. The minority carrier generation lifetime was measured using the technique of deep depletion recovery of MOS capacitors, described in principle by Zerbst [5]. The capacitors were formed (using conventional furnace processing) by oxidizing the epitaxial layers in a steam ambient at 1000 °C to give an oxide thickness of about 65 nm. A high temperature anneal, metal evaporation, lithography, patterning, and a 450 °C forming gas anneal completed the fabrication of the test structure.

Table I Minority carrier generation lifetimes for LRP epitaxial Si as measured by the MOS deep depletion recovery technique.

Sample	Doping type and Orientation	Doping level (cm^{-3})	Generation Lifetime (μs)
Cz	n-(100)	2 x 10^{15}	49-87
LRP	n-(100)	2.5 x 10^{16}	1.4-4.3
Cz	p-(100)	7 x 10^{16}	144-203
LRP	p-(111)	7 x 10^{16}	14-94

The results of the generation lifetime measurements are shown in Table I. In all cases there was some random variation, but the generation lifetimes in the LRP samples were consistently in the range of microseconds for n-type epitaxial films and tens of microseconds for p-type epitaxial films. The cause of the higher lifetimes observed in p-type films is unknown. While the lifetimes for the LRP films were roughly an order of magnitude lower than those found in the Czochralski control wafers, they nevertheless represent excellent material. Generation lifetimes in the 10 μs range are common for epitaxial silicon used in VLSI processing [6].

The simplest minority carrier device is a p-n junction diode. Planar diodes were fabricated in the LRP epitaxial layers described above by ion implantation and annealing. The depth of the annealed junctions was on the order of 0.2 μm so that the p-n junction and its associated depletion region remained in the epitaxial films.

The n^+-p and p^+-n diodes fabricated had well behaved curve-tracer characteristics and had breakdown voltages consistent with the doping of the epitaxial films (24 V for the p^+-n diodes, 14 V for the n^+-p diodes). Diode quality factors were extracted from the linear portion of diode current-voltage curves. Typical values were 1.05 for the p^+-n diodes and 1.10 for n^+-p diodes. Control diodes in Czochralski substrates had quality factors of 1.00-1.03.

At 5 V reverse-bias, the leakage current measured on p^+-n diodes in the LRP films was 20 nA/cm^2. Using a simple one-dimensional approximation for the depletion region width, a generation lifetime of 4 μs can be calculated to be consistent with this leakage current. This lifetime is within the range of those measured by the MOS deep depletion recovery method.

In summary, the minority carrier properties of silicon epitaxial films grown by limited reaction processing have been investigated. The combination of relatively high lifetimes (1-100 μs) and good diode charactersistics show that the LRP films have potential for use in high quality bipolar transistors.

EPITAXIAL GROWTH OF SILICON: ULTRA-THIN p^+ LAYERS

Materials Properties

Currently, diffusion and ion implantation are two commonly used methods for introducing dopants into semiconductors. VLSI devices, however, will require abrupt doping transitions and ultra-thin, highly-doped layers which may be beyond the capabilities of these techniques. Ultimately, a technology with the interface control of molecular beam epitaxy (MBE) and the doping range of chemical vapor deposition (CVD) will be needed. Limited reaction processing has potential for both of these capabilities. In this section, the fabrication of single crystal silicon structures with ultra-thin, highly-doped regions and abrupt doping profiles is demonstrated.

Multilayer structures consisting of alternating undoped and p^+ regions were fabricated to study layer thickness control and the abruptness of doping profiles. Multiple layers were deposited sequentially *in - situ* by changing the gas composition between high temperature cycles. The p^+ films were deposited under the same conditions as the undoped layers except the carrier gas was changed from H_2 to 5.2 ppm B_2H_6 *in* H_2.

A typical SIMS profile of a sample (LRP 109) with two p^+ regions is shown in Figure 3. The p^+ "pulses", deposited using a 5 second LRP cycle, have a full-width at half-maximum value of 10 nm. Such ultra-thin layers can be fabricated reproducibly. The boron concentration for sample LRP 109 changes four orders of magnitude, from 10^{17} to 10^{21} atoms/cm^3, over a distance of less than 40 nm (10 nm/ decade). For comparison, undoped/p^+/undoped multilayer structures deposited by MBE exhibit boron doping transitions of about 10 nm/decade [7]. These transition values are limited by the depth resolution of SIMS. Clearly, the p^+ multi-pulse sample shown in Figure 3 demonstrates that LRP can produce ultra-thin, highly-doped films of epitaxial silicon with excellent control of layer thicknesses and doping profiles.

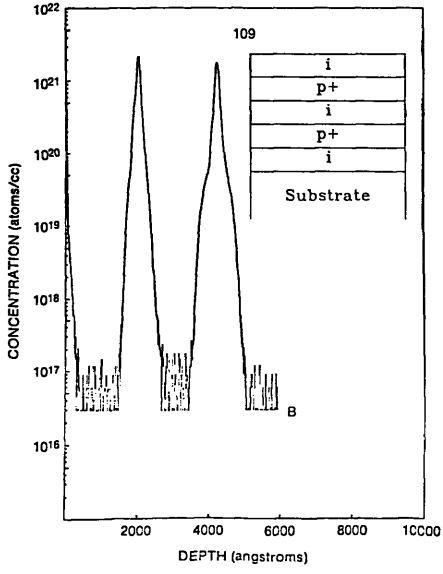

Fig. 3 SIMS profile of an i/p⁺/i/p⁺/i multilayer sample. The first pulse which was deposited shows a slight amount of outdiffusion caused by the thermal cycles of subsequent layers. (Charles Evans and Assoc.)

Electrical Properties

For electrical measurements, p^+ layers (0.1 - 0.6 μm) were deposited on n-type substrates (1 - 10 Ω-cm). Figure 4 shows SIMS and spreading resistance data for sample LRP 82. The spreading resistance curve was scaled by matching its integrated carrier concentration to the value determined by Van der Pauw measurements. The Van der Pauw technique was also used to measure a sheet resistivity of 58 Ω/□ and a hole mobility of 42 cm^2/Vs for sample LRP 82. This value of mobility is comparable to that of bulk material with the same hole concentration [8].

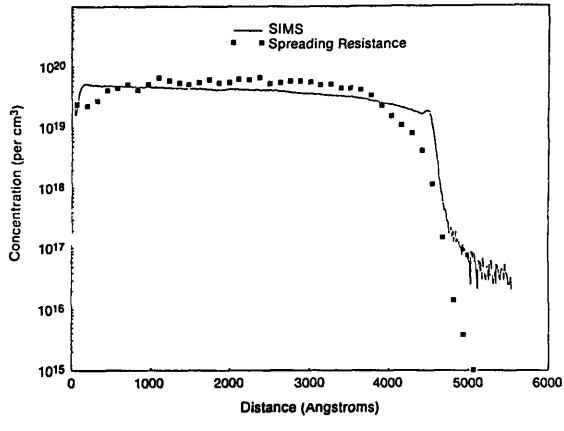

Fig. 4 A comparison of SIMS and spreading resistance (Solecon Labs) profiles for a p^+ LRP epitaxial silicon layer deposited on an n-type substrate.

The highest hole concentrations measured by spreading resistance and Van der Pauw were in the range of 2 x 10^{20} cm^{-3}. For some samples, SIMS indicated significantly higher boron concentrations. Inactive boron is thus present, the nature of which is currently being invesitgated by transmission electron microscopy.

P - n junction test structures were also fabricated. First, a standard field oxide was grown and etched to reveal 600 x 600 μm^2 square regions of bare n-type silicon substrate. P^+ epitaxial silicon was then deposited under the conditions described above, or selectively by adding HCl to the ambient [9]. Figure 5 shows the current-voltage relationship in forward bias of a diode produced by selective epitaxy. The diode quality factor is 1.02, indicating nearly ideal diode behavior. Similar current-voltage curves were found for non-selective depositions. The ability to fabricate a high quality junction between an epitaxial layer and a substrate suggests that the epi/substrate interface has few defects and is not affected by substrate surface contamination.

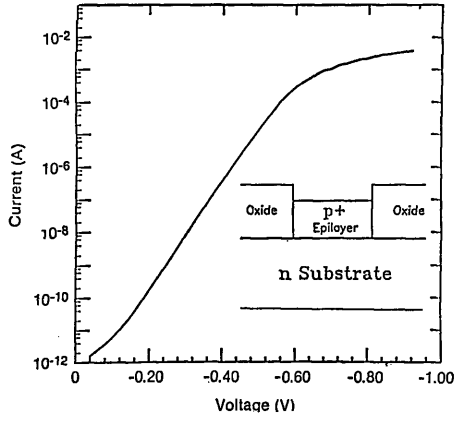

Fig. 5 Diode current-voltage curve for a p^+-n LRP epitaxial layer-substrate junction. The p^+ epitaxial layer was deposited selectively at 925 °C for 30 s. The diode quality factor is 1.02.

The fabrication of ultra-thin regions of single crystal silicon with high doping densities and excellent electrical properties has been demonstrated using LRP. The following paragraphs describe the use of LRP to produce devices consisting of multiple layers of silicon and silicon dioxide.

IN - SITU MULTILAYER DEPOSITION: MOS CAPACITORS

The metal-oxide-silicon (MOS) capacitor structure forms a crucial element in modern integrated cirucit technology. This three-layer sandwich is the key to MOS field-effect transistors (MOSFET's) and is used to store bits of data in dynamic random access memory (D-RAM) circuits. Conventionally, the oxide is grown in one reactor and the wafer is physically transported to a second reactor for doped polysilicon deposition. LRP can be used to fabricate the multilayer MOS structure without removing the wafer from the processing chamber. Such *in - situ* multilayer fabrication might avoid the inevitable chemical and particulate contamination that occurs when wafers are carried from the oxidation furnace to the polysilicon reactor. This contamination could diffuse through the oxide to the sensitive substrate/oxide interface during subsequent high temperature steps.

The wafers used for the experiments were two-inch diameter, phosporus-doped (100) silicon wafers with a resistivity of 3 Ω-cm. The gate oxidation was performed in dry oxygen with 4% HCl at a temperature of 1150°C and a pressure of 500 torr. An LRP cycle of 2 minutes yielded an oxide thickness of 29 nm. A layer of heavily boron-

doped polysilicon was then deposited *in - situ* using silane and diborane in hydrogen at 1.5 torr and 580 °C. A 7 minute LRP cycle yielded a 0.4 μm layer with a sheet resistivity in the range of 50 to 100 Ω/[ ]. Next, the samples received a 1150 °C, 15 second anneal in argon to improve the quality of the silicon/oxide interface [10]. The final processing step was a 375°C forming gas anneal.

The high and low frequency C-V curves are shown in fig. 6, and the interface state density is shown in fig. 7. The midgap interface state density is 5 x 10^9 $cm^{-2}eV^{-1}$ and the fixed charge is 0 ± 1 x 10^{10} cm^{-2}, values comparable to the best conventionally produced silicon/oxide interfaces. Although such an interface charge is unusual, an error in the assumed metal-semiconductor work function difference (0.54 eV [11]) of only 0.03 eV would change the calculated N_f by 2 x 10^{10} cm^{-2}. The effect of mobile ions on N_f, as revealed by bias-temperature stress measurements, was less than 1 x 10^{10} cm^{-2}.

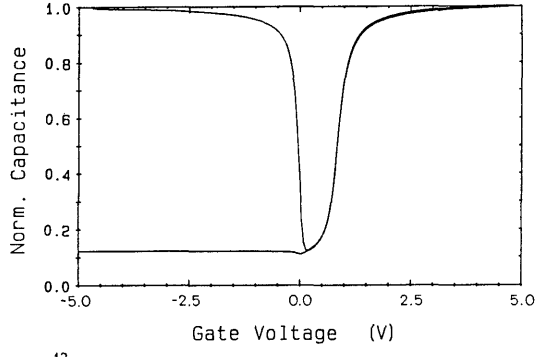

Fig. 6 Typical C-V curves for an *in - situ* MOS capacitor fabricated by LRP. Area = 0.0048 cm^2 C_{max} = 504 pF

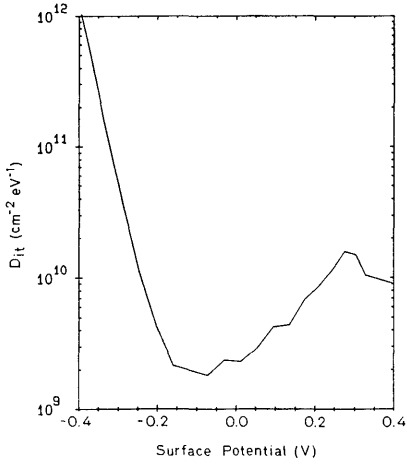

Fig. 7 Interface state density as a function of the bandgap energy for the capacitor in figure 6.

To further probe the oxide quality, tunneling current measurements were performed. Fig. 8 shows the tunneling current in an *in-situ* polysilicon capacitor of area 1.6 x 10^{-3} cm^2. The voltage was scanned five times, but the first four times the scan was stopped just before destructive breakdown. The fact that the curves fall on top of one another indicates good oxide stability. On the fifth scan, the voltage was increased until breakdown. The observed breakdown field of 10 MV/cm is that

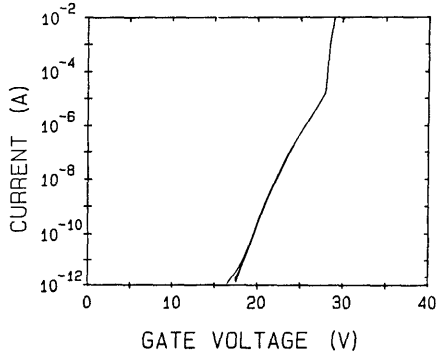

Fig. 8 Tunneling current scans for a typical capacitor. The voltage was scanned four times and then a fifth time to destructive breakdown.

expected for high-quality SiO_2 films.

In summary, the use of limited reaction processing to fabricate *in-situ* multiple layers for MOS capacitors has been demonstrated. The fabricated capacitors exhibit excellent characteristics. The ability to deposit gate electrode layers *in-situ* should provide a useful tool for studying gate electrode-semiconductor work function differences. Larger scale experiments are still needed, however, to evaluate the yield and uniformity implications of *in-situ* multilayer processing.

CONCLUSION

Limited reaction processing allows a high growth temperature for good material qualities, yet minimizes the thermal exposure of the substrate to obtain abrupt interfaces. The *in - situ* fabrication of multiple layers of doped and undoped epitaxial silicon, thermal oxide, and polysilicon with excellent electrical properties has been demonstrated. The control of layer thicknesses is excellent using LRP, even for layers thinner than a few hundred angstroms. The ability to deposit multiple thin layers with sharp interfaces suggests applications as diverse as those ascribed to molecular beam epitaxy.

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