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Limited Reaction Processing: *In-situ* Epitaxial Silicon-Thin Oxide-Polysilicon Layers for MOS Transistors

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Limited reaction processing is a new technique for the *in-situ* growth and deposition of multiple thin high-quality semiconductor and insulator layers. We report here on the *in-situ* growth of epitaxial silicon-thin oxide-doped polysilicon structures and describe the performance of n- and p-channel MOSFET's made using these layers (t_{ox} = 140 Å, L_{eff} = 0.8 μm).

The limited reaction processing system basically consists of a quartz tube connected to a low-pressure pumping apparatus [1]. A gas control system can supply several conventional processing gases such as silane, argon, oxygen, diborane, etc. The tube is surrounded by microprocessor-controlled lamp banks which can bring a wafer inside the tube from room temperature to typical processing temperatures (e.g. 1000 °C) in less than three seconds. With such rapid temperature control, the gas flows are first stabilized with the wafer at room temperature, and the surface reaction is then switched on and off by controlling the wafer temperature. By changing the process gases between high-temperature cycles, multiple individual rapid thermal processing steps, such as silicon epitaxy [1] or oxidation [2], can now be performed sequentially *in situ*, i.e. without disturbing the wafer or breaking the vacuum seal of the system.

To avoid the inevitable interface contamination that occurs when wafers are transported from one reactor to another, an *in-situ* process for MOSFET's was developed. Starting with heavily doped substrates, active area holes were first opened up in a field oxide in a conventional manner. The wafers were then loaded into the LRP apparatus and, following an *in-situ* pre-cleaning step, were subjected to three sequential growth or deposition cycles: (1) silicon epitaxy (t_{si} = 1.5 μm), (2) oxidation (t_{ox} = 140 Å), and (3) doped polysilicon deposition. For device isolation, the epitaxial growth process was adjusted to be selective, i.e. the growth occured only in the oxide holes. Following the high-temperature step for epitaxy, the process gases were changed and a thin gate oxide was grown at 1100 °C. During a third high-temperature step, a layer of heavily doped polysilicon was deposited. The wafers were then removed from the processing chamber, and conventional processing was used to convert the multi-layer MOS structures into both p- and n-channel MOSFET's (minimum L_{eff} = 0.8 μm). The MOSFET's were well-behaved and exhibited excellent threshold uniformity. In general, the advantages of interface cleanliness offered by multi-layer *in-situ* processing could be important for the uniformity and yield requirements demanded by ULSI.

1. C.M. Gronet, K.E. Williams, and J.F. Gibbons, Appl. Phys. Lett. **47**, 721 (1985).
2. J. Nulman, J.P. Krusias, and A. Gat, IEEE Electron Dev. Lett. **EDL-6**, 205 (1985).

interface density of states, dielectric breakdown field, and charge to breakdown of 10^{10} $eV^{-1} \cdot cm^{-2}$, 15 MV/cm and 100 C/cm^2, respectively, for films as thin as 100 Å [2]. In RTO processing, heat is provided by tungsten-halogen lamps and the temperature monitored via a pyrometer. The wafers are introduced at room temperature into a shallow quartz tube, after a short purge with nitrogen, oxygen is introduced into the chamber and the temperature ramped up to typically 1150°C. High-temperature processing times varied between 1 to 300 s. RTO and furnace control processes have been applied to the growth of 250-Å gate oxides on standard production 4K NMOS poly-gate static RAM wafers. The RTO SRAM's showed an access time of 35 ns, a value that meets the high end performance spec of the device. Bias stress experiments resulted in no degradation of the SRAM performance. Typical SRAM transistors were tested on test chips distributed across the wafer. The transistors characteristics for RTO and furnace control oxides were similar. Electrically calculated oxide thickness resulted in a uniformly better than 2 percent across the wafer and from wafer to wafer. This uniformity result matched the ones obtained from ellipsometry measurements. We have also applied this SRAM process to 150-Å gate oxides. The performance of these transistors and the gate dielectrics will be reported. The present device results and the quality of RTO oxides make this a viable technology for the thin oxidation needs by the VLSI technology.

[1] J. Nulman, J. P. Krusius, and A. Gat., "Rapid thermal processing of thin gate dielectrics. Oxidation of silicon," *IEEE Electron Device Lett.*, vol. EDL-6., no. 5, p. 205, May 1985.
[2] J. Nulman, J. Scarpulla, T. Mele, and J. P. Krusius, "Electrical characteristics of thin gate implanted MOS channels grown by rapid thermal processing," in *IEDM Tech. Dig.*, p. 376, Dec. 1985.

IIIB-2 The Fabrication Submicrometer MOSFET's Using Laser Doping—P. G. Carey, K. Bezjian, and T. W. Simon, Stanford Electronics Labs, Stanford University, Stanford, CA 94305, T. Magee and P. Gildea, XMR Inc., Santa Clara, CA 95054.

One of the important objectives in a VLSI process is fabrication of shallow n^+ and p^+ source-drain regions for the n- and p-channel transistors. The conventional implantation processes used to fabricate these junctions require very high implant doses and low energies. These conditions in general give rise to difficulties which serve to complicate a conceptually simple process. The purpose of this work is to describe the successful fabrication of submicron NMOS transistors using gas immersion laser doping (GILD) [1]. The GILD process results in ultra-shallow high concentration n^+ and p^+ profiles.

The GILD apparatus consists of a gas cell, a XeCl (λ = 308 nm) pulsed excimer laser, a highly sophisticated beam homogenizer, and a computer to precisely control and record the process parameters. The GILD step uses the XeCl excimer laser to dope a very shallow region of the Si surface by a melt-regrowth transient. Upon immersion into the gas cell, dopant molecules are adsorbed onto the clean silicon surface. The surface is then exposed to the laser beam and the top 600 to 1000 Å of the Si melts allowing the dopant to diffuse into this region before the recrystallization of this layer (~200 ns). Multiple (2–20) pulses of the laser result in more dopant being incorporated into the layer so that high concentration (1×10^{19} to 2×10^{21} cm^{-3}) shallow (650 to 1000 Å) n^+ and p^+ box-like profiles can be fabricated. This is in direct contrast to low energy ion implantation profiles which exist deeply penetrating channeling tails [2], [3].

The GILD step has been used to dope the source-drain and gate regions of n-channel devices using an otherwise conventional NMOS process. The AsH_3 adsorbs onto the 0.5-μm-thick polysilicon gate (which serves as a channel mask) and the exposed silicon in the source-drain regions. Ten pulses at laser energies of 0.55, 0.60, 0.65, and 0.75 $J \cdot cm^{-2}$ were then used to dope both regions of the device. The entire thickness of the poly melts because it sits on top of the gate oxide which is a poor heat conductor.

The resultant devices have n^+ source-drain junctions from 0.065 to 0.10 μm and low-resistance recrystallized polysilicon gates. Values of R_{sheet} for these shallow junctions range from over 1000 ($\Omega/\square$) to ~110 ($\Omega/\square$) for the n^+ source-drain regions and ~12 ($\Omega/\square$) for the 0.5-μm-thick poly. Values as low as 20–30 ($\Omega/\square$) have been obtained on other GILD junctions using slightly higher energies. SEM cross sections show little or no encroachment of the source-drain regions under the edge of the poly. The I_d versus V_{ds} curves for these devices show flat saturation values (low λ) and there is little V_{t0} shift seen for values of $L_{poly} < 1.0$ μm. A detailed discussion of the processing and measured device results will be given.

[1] P. G. Carey, T. W. Sigmon, R. L. Press, and T. S. Fahlen, "Ultra-shallow high-concentration boron profiles for CMOS processing," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 291–293, 1985.
[2] T. M. Liu and W. G. Oldham, 'Channeling effect of low energy boron implant in (100) silicon," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 59–62, 1983.
[3] J. F. Ziegler and R. F. Lever, "Channeling of ions near the silicon ⟨100⟩ axis," *Appl. Phys. Lett.*, vol. 46, no. 4, pp. 358–360, Mar. 1985.

IIIB-3 Limited Reaction Processing: *In-Situ* Epitaxial Silicon Thin-Oxide Polysilicon Layers for MOS Transistors—J. C. Sturm, C. M. Gronet, and J. F. Gibbons, McCullough 226, Stanford Electronics Labs, Stanford University, Stanford, CA 94305.

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[2] J. Nulman, J. P. Krusias, and A. Gat, *IEEE Electron Device Lett.*, vol. EDL-6, p. 205, 1985.

IIIB-4 Shallow Junction Formation for CMOS VLSI Application Using Tin Preamorphization—B. Molnar and H. B. Dietrich, Naval Research Laboratory, Washington, DC 20375.

In recent years shallow junction formation for CMOS VLSI fabrication has been an active area of research. Significantly shallower junctions have been made through the application of preamorphization and rapid thermal anneal (RTA) techniques. Preamorphization with Ge has proven to be more convenient and reliable than the conventional Si approach and the Hall mobilities for boron implants into this material have been reportedly enhanced [1]. This enhancement has been attributed to the strain compensation provided by the Ge. Tin (Sn) is isoelelectronic with Si and Ge and hence represents an attractive canidate for preamorphization in that amorphization can be accomplished with a lower dose than that required for either Si or Ge and because of the relative covalent radii of Si, Ge, and Sn (1.18, 1.22, and 1.4 Å, respectively). Sn should be more effective in reducing the lattice strain associated with B doping. In fact Sn co-doping has been successfully used to reduce the B related strain in diffused junctions [2]. For these reasons we have undertaken a study of the formation of shallow p^+ and n^+ junctions through the application of Sn preamorphization and RTA techniques.

The critical dose for amorphization has been determined for 200- and 400-keV Sn and the layer thickness has been measured as a function of dose. The regrowth rate for (100) Si amorphized with Sn has been found to be 80 A/min at 550°C. RBS and TEM have been used to determine the quality of the regrown layer. Channeling measurements show that the Sn is close to 100-percent substitutional. TEM micrographs show a band of dislocation loops at the initial amorphous crystalline interface but high-quality material between this region and the surface. Electrical measurements on the regrown layer show that there are no shallow or compensating deep levels associated with the implanted Sn. Spreading resistance profiles of low-energy B and P implants have been compared to those obtained for control implants without the preamporphization to quantify the effects of the Sn implantation and the RTA techniques. The preamorphization eliminates tailing and reduces the junction depths by as much as a factor of two. Hall data for the layers formed in the Sn preamorphized material have been compared to that for control samples. For Sn concentrations of less than 10^{19}/cc no increase in p-type mobilities (measured to be on the order of 40 $cm^2/V \cdot s$ for the 10^{20}/cc B concentrations investigated) have been observed. Diodes have been fabricated to measure the leakage current associated with the various approaches to shallow junction formation. These data will also be presented.

[1] J. Liu, J. J. Wortman, and B. B. Fair, DRC 85 IIB-6.
[2] T. H. Yen *et al.*, *J. Electrochem. Soc.*, vol. 116, p. 73, 1969.

IIIB-5 Recessed Silo—A Submicrometer VLSI Isolation Technology—John Hui, Paul Vande Voorde, and John Moll, Hewlett-Packard Laboratory, 3500 Deer Creek Road, Palo Alto CA 94304.

A new VLSI device isolation technology, recessed sealed interface local oxidation (recessed SILO) has been developed. This process provides a completely planar silicon surface suitable for VLSI photolithography and etching. The process is bird's beak free, low in crystal and gate oxide defect density, and can be scaled into the submicrometer regime.

The structure is fabricated by forming a thin layer of oxide on silicon, followed by deposition of 10 nm of LPCVD nitride, 40 nm of LPCVD oxide, and 150 nm of LPCVD nitride. The wafer is then patterned by photolithography. Anisotropic plasma etch is done to etch through the entire nitride/oxide/nitride/oxide layers. The silicon is recess etched 100 to 150 nm. Boron field implantation is done. 600 nm of field oxide is then grown at 950°C in steam. The nitride/oxide/nitride/oxide layers are then etched away which removes about 100 nm of field oxide.

The recessed SILO process differs from the original SILO process in two major areas [1]. First of all, the silicon is recess etched 100 nm to 150 nm to allow the field oxide to be fully sunk into the silicon and provides a completely planar surface. The second aspect is that, instead of sealing off the silicon/silicon dioxide interface with thermal nitride, a thin layer of oxide is formed between the silicon and the LPCVD nitride. This thin layer of oxide allows the oxidation profile to relax into a gentle shape which is essential for defect free isolation [2]. A small bird's beak is formed but it is etched away during the removal of the nitride/oxide/nitride/oxide layers. The final oxide isolation structure is bird's beak free and planar. Secco etch of the silicon wafers after processing shows very low crystal defect density. The diode reverse bias leakage current of Recessed SILO is found to be comparable to that of LOCOS technology. The gate oxide defect density of recessed SILO technology is found to be comparable to that of LOCOS technology and is much better than the original SILO technology with the thermal nitride. The recessed SILO technology is less susceptible to the field oxide thinning effect in submicrometer isolation spacing than technologies like SWAMI because there is no bias into the isolation region [2]. For a field oxide thickness of 550 nm, the process can be scaled down to about 0.5 μm compared to about 0.8 μm for SWAMI. Compared to conventional LOCOS process, the recessed SILO process has only one extra LPCVD nitride deposition step and one oxide formation step and is a lot simplier than other VLSI isolation processes reported.

[1] J. Hui *et al.*, "Electrical properties of MOS devices made with SILO technology," in *IEDM Tech. Dig.*, pp. 220–223, Dec. 1982.
[2] J. Hui *et al.* "Scaling limitations of submicron local oxidation technology," in *IEDM Tech. Dig.*, pp. 392–395, Dec. 1985.

IIIB-6 The Dependence of MOSFET Output Resistance on Drain Doping Profiles—Fu-Chieh Hsu, Integrated Device Technology, Inc., 3236 Scott Blvd., Santa Clara, CA 95052.

The theory and model for the behavior of the output resistance in short-channel MOSFET's with different drain structures are studied based on experimental data and PISCES [1] simulations.

Using MOSFET's to implement analog circuitry is getting increasing interest due to its higher packing density and ease to integrate both digital and analog functions/systems on a monolithic chip than using bipolar junction transistors. The MOSFET in general, however, suffers from poor matching, low transconductance and low attainable gain per stage resulted from its low output resistance. The low attainable gain per stage is particularly severe for many analog applications in very short-channel devices which otherwise promise higher transconductance, higher cutoff frequency and higher packing density.

In search for a better way to optimize the device characteristics for analog applications, several MOSFET structures were fabricated and simulated to study the behavior of their corresponding output resistances. These structures include the conventional, double-diffused drain (DD), lightly-doped drain (LDD) and pocketed drain (PD) devices. It is shown that the traditional channel-length modulation (CLM) models [2], [3] that were commonly used to describe the behavior of the drain output resistance are inadequate and sometimes misleading in projecting device characteristics for