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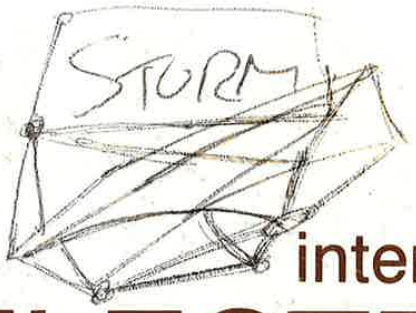

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Ultra-High Speed CMOS Circuits in Thin SIMOX Films

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ABSTRACT

CMOS dual-modulus prescaler circuits were built in very thin SIMOX films. They operate at 6.2 GHz, the highest speed ever reported for a digital CMOS circuit and 50% faster than the control circuits built in bulk Si. The high speed is obtained by taking advantage of the intrinsic properties of the SOI structure combined with the symmetric CMOS technology that simultaneously optimizes the characteristics of both the p and n-channel transistors.

INTRODUCTION

Combining the SOI and CMOS technologies offers improved circuit performance, along with simpler device processing. There is a substantial increase in speed in the SOI structure, particularly when the transistors operate in the fully depleted mode. The source/drain capacitance is negligible, and the conductor line capacitance is reduced because of the thick underlying oxide, i.e. the composite of field and isolation oxides. Furthermore , the CMOS device fabrication process in SOI is compatible with and simpler than the bulk CMOS process, in particular in the formation of shallow source and drain junctions.

The compatibility of SOI and CMOS technologies was originally demonstrated in thick (~0.5μm) Si films. This, however, does not take full advantage of the SOI potential. The circuits fabricated in thick films do not perform at speeds much higher than the bulk [1,2], in addition, the devices show a "kink" behavior due to the floating body effects.

More recently the feasibility of the SOI/CMOS technology has been demonstrated in very thin (~1000Å) Si films, and operation of individual devices and small scale circuits have been reported [3 - 5]. In thin films the "kink" effect does not exist, and ring oscillator speeds of about 30 ps have been achieved [4,5].

We have taken advantage of the high quality Si films on SIMOX wafers obtained by annealing at near Si melting temperature, and those of symmetric CMOS technology to achieve a 50% increase in the speed of dual-modulus prescalers.

EXPERIMENT

The SOI structure was formed by implanting 4-inch n-type (100) wafers with 1.7×10^{18} oxygen ions at 200 keV while holding the substrate temperature at 615 °C. The wafers were then coated with 0.5μm of LPCVD oxide and annealed for 30 min. in a lamp furnace. Wafers were heated from the back side up to their melting temperature so that the optical properties of Si would provide an intrinsic feedback necessary to keep the device side precisely at 1405°C [6]. After annealing, the structure consisted of 2400Å of crystalline Si with some dislocations but no oxide precipitates, on 3500Å of synthesized SiO_2, with atomically abrupt interfaces. Subsequently, the Si overlayer was thinned by oxidation to about 1200Å to obtain films that are fully depleted in the transistor channel regions.

Device fabrication processes were optimized for bulk Si and not for SOI structures. Lateral isolation was achieved by local oxidation through the Si film thickness. Gate oxide thickness was 125 Å, and $CoSi_2$ was used in the source, drain, and gate areas.[7] No additional implant aimed at the Si/buried oxide interface was used. The final device structure is shown in Fig. 1.

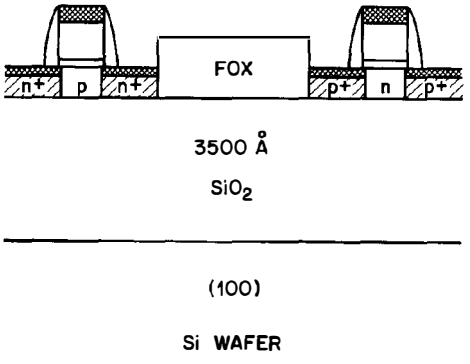

Fig. 1 Schematic structures of n- and p-channel transistors on SOI.

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The prescalers, designed as dual modulus divide-by-128 or 129 counters, consisted of a high speed divide-by-4 or 5 counter, and a lower speed divide-by-32 counter [8]. The block diagram of the prescaler is shown in Fig. 2. The speed of this prescaler is determined by the divide-by-4/5 counter, which uses two NAND gates and three edge-triggered D-type flip-flops clocked synchronously by the high-frequency input signal. To reduce the capacitive loading, 0.75μm wide aluminum lines and 0.5μm metal salicide runners were used.

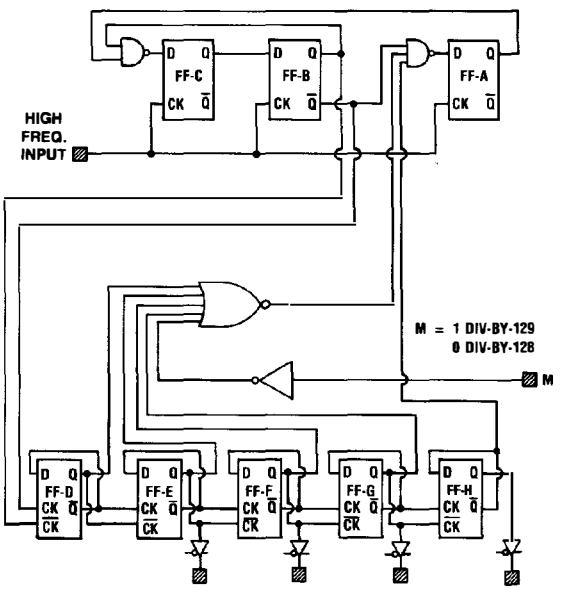


Fig. 2 CMOS prescaler functional block diagram.

RESULTS AND DISCUSSIONS

Current-voltage characteristics of both n- and p-channel transistors for design gate length of 0.62μm, and effective channel length 0.42μm, are shown in Fig. 3. The kink effect, typical of SOS and SOI devices, is absent because the thin Si film is fully depleted. These traces were obtained using a back-gate bias , V_{bg}, of -6V. We found that -4 to -6V back-gate bias was needed to turn off the finite leakage at low gate voltages. The application of V_{bg}, in addition, helped make the V_{th} of n- and p-channel devices nearly symmetric. The threshold voltages for n-and p-channel devices with several different L_{eff}, as a function of backgate bias are shown in Figs. 4 and 5.

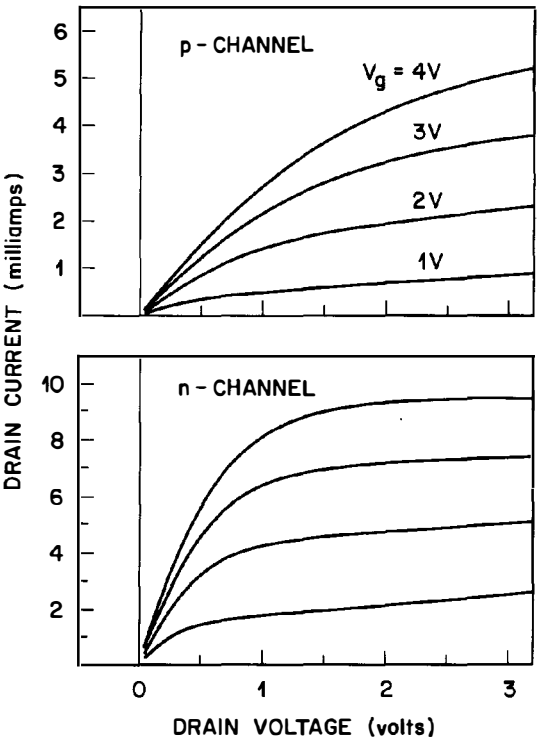


Fig. 3 Drain current vs. voltage characteristics of 0.62 μm (L_{eff}=0.42μm) n- and p-channel transistors with -6V back-gate bias.

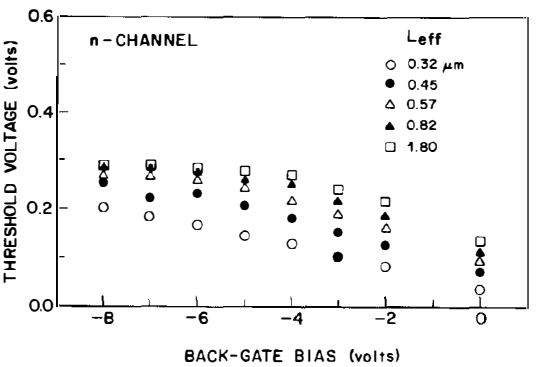


Fig. 4 Threshold voltage of n-channel devices as a function of back-gate bias.

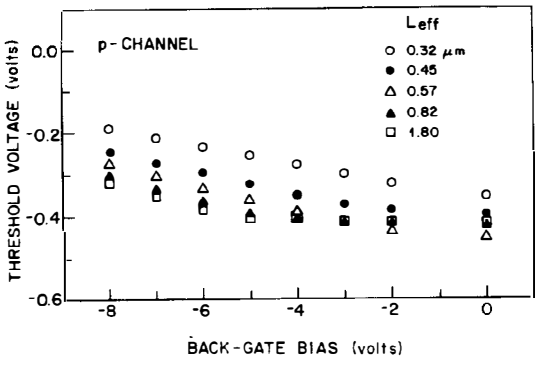


Fig. 5 Threshold voltage of p-channel devices as a function of back-gate bias.

The threshold voltages for -6V bias on the substrate were 0.24V and -0.30V, and the mobilities were 420 $cm^2/V{\cdot}s$. and 100 $cm^2/V{\cdot}s$ in n- and p-channel transistors respectively. Figure 6 illustrates the subthreshold characteristics of 0.62, 1 and 2μm n-channel transistors with the subthreshold swings indicated on the figure.

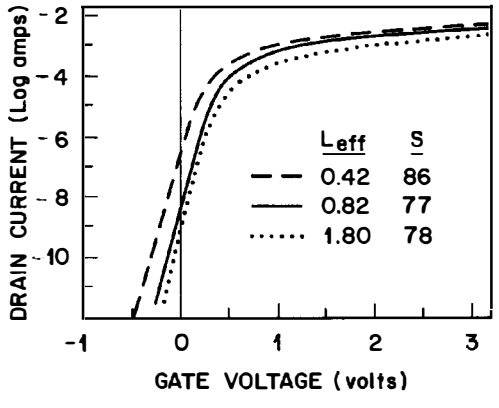


Fig. 6 Subthreshold behavior of 3 transistors with design gate lengths of 0.62 μm, 1.0μm and 2.0μm. V_{ds} = 0.01 V. The L_{eff} is given in μm, and S, the subthreshold swing, in mV/decade.

The ring oscillator delays per stage measured in 49 stage ring oscillators for the SOI and the bulk monitors are shown in Fig. 7. The delays in the circuits on SOI are ~40% lower for all channel lengths.

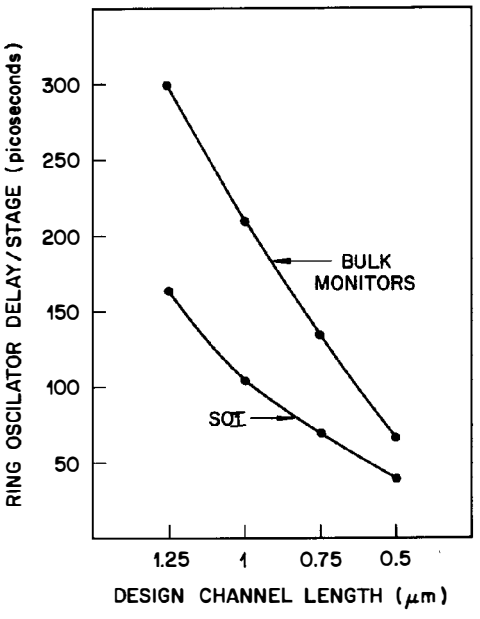


Fig. 7 The ring oscillator delays as a function of gate length for both SOI and the bulk monitors.

The minimum delays as a function of Vdd between 1 and 5 volts are shown in Fig. 8. Note that even at a small Vdd of 2V the delay is only 50ps, and it drops to 34 ps for Vdd = 5V.

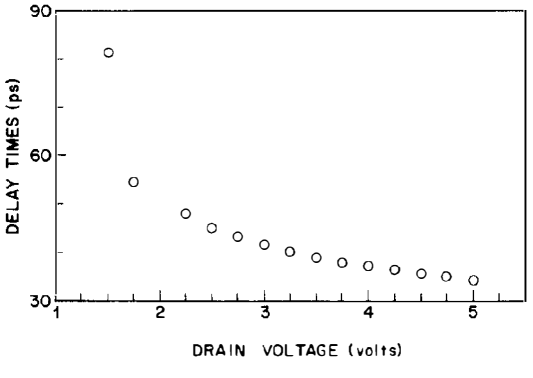
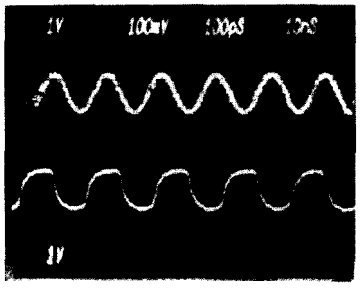


Fig. 8 Ring oscillator delay times as a function of drain voltage.

The best SOI prescaler was found to be functional at 6.2 GHz (Fig. 9) consuming 210 mW of power at Vdd of 3.5V. The effective gate length of the transistors is approximately 0.4μm. Back-gate bias between -4 and -6.5V with respect to the V_{ss} was applied so that a threshold voltage of about 0.2V was obtained for both p and n channel transistors.



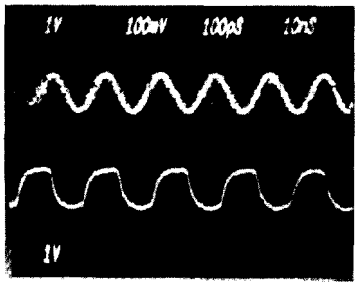


Fig. 9 Oscilloscope traces for the input and output signals for the SOI prescaler: (a) divide-by-128, and (b) divide-by-129.

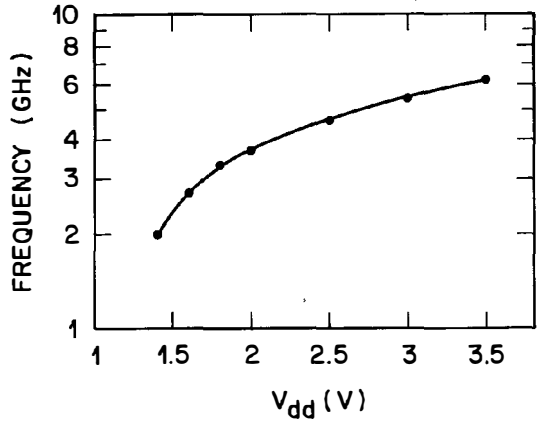


Fig. 10 Maximum operation frequency of the SOI prescaler as a function of the supply voltage.

Maximum operation frequency was dependent upon the supply voltage (Vdd), and varied by about 1.6 GHz per volt of Vdd (see fig. 10). One partially operational prescaler (÷ 64) had a toggle frequency of 7 GHz.

It is noteworthy that the prescaler is still functional at 2 GHz with the supply voltage as low as 1.4V dissipating only 11 mW of power. The speed of this SOI prescaler at 6.2 GHz is substantially higher than those of similar prescalers that have been published to date (generally ranging from 2.5 GHz to 4.6 GHz, see Ref. 8). This speed, in addition, is 2.5 times higher than the fastest reported Ga-As and Bipolar ÷ 128/129 counters.

ACKNOWLEDGEMENTS

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