Extended Abstracts of the 15th Conference on Solid State Devices and Materials, Tokyo, 1983, pp. 1-2

Invited

Circuit Simulation of Three-Dimensional Device in Beam-Recrystallized Polysilicon Films

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ABSTRACT

A set of folding and rotation operations is used to transform planar MOSFET device configurations into three-dimensional structures in beam recrystallized polysilicon films. Circuit simulation techniques are used to judge packing density, speed, and yield of each configuration in an integrated circuit layout. The implications of this analysis are explored to estimate the potential of three dimensional integration.

In 1979, Lee et al. (1) fabricated the first MOSFETs in laser-recrystallized polysilicon films and made a variety of measurements showing that these films were worthy of further study as an alternative to SOS technology. Shortly afterwards Lam et al., in collaboration with the Stanford group (2), fabricated 11-13 stage ring oscillators in laser recrystallized films with a minimum propagation delay of 44 ns per stage compared to a propagation delay of 36 ns per stage for the same circuit made on a single crystal substrate. Since then a substantial number of papers have been published on this subject (3, and references cited therein), leading to a number of techniques for improving the recrystallization process itself. Devices capable of integration into large area liquid crystal display decoders have been demonstrated(4). In addition, the possibility of three-dimensional integration has been established by Gibbons and Lee (5), who made a stacked CMOS structure with a common gate interposed between the two surfaces on which enhancement mode MOSFET action was desired. More recently, Gibbons et al. (6), described stacked MOSFETs that were fabricated in a single recrystallized film in which the devices utilized separate gates to obtain independent enhancement mode behavior on each surface of the recrystallized film.

From a topological point of view, both of these stacked devices can be visualized as arising from a series of folding and rotation operations, using the equivalent planar (single surface) device as a primitive. Several examples will be given to illustrate the procedure.

Using the procedure, several different implementations of a CMOS shift register (bulk, SOI, (SPICE) has been employed to compare these technologies.

Each configuration is described in terms of its packing density, speed and manufacturing yield. For a gate having area A, propagation delay $\bar{t}_D$ and requiring M separate masking operations for fabrication, each with a yield y, a figure a merit

$$\mu = (y)^M/(2A\,\bar{t}_D)$$

can be calculated. This figure of merit is calculated for the different implementations of the shift register and used to judge the efficacy of the various implementation possiblities.

The results of this analysis suggest that, in the near term, memory applications are more likely candidates for commercialization than logic, except for special cases. This and other general conclusions will be developed and presented.

References

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