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LIMITED REACTION PROCESSING AND THE GROWTH OF IN-SITU MULTI-LAYER STRUCTURES

James C. Sturm
Department of Electrical Engineering
Princeton University
Princeton, New Jersey 08544

Limited Reaction Processing (LRP) is a new surface modification technique for the fabrication of thin, high-quality layers of semiconductors and insulators. The central feature of LRP is the use of radiant heating to produce large, yet rapid changes in the temperature of a wafer both accurately and reproducibly, enabling precise control of thermally driven surface reactions. The system essentially consists of a quartz single-wafer processing chamber surrounded by microprocessor-controlled lamp banks. The chamber is connected to a low-pressure pumping apparatus and a gas control system which can supply several conventional processing gases. The temperature control available with LRP allows the substrate temperature to be used as a "switch" to control thermally-driven surface reactions such as epitaxial growth or oxidation, much as a physical shutter is used in an MBE machine.

Because the wafer can be brought by the lamp heating from room temperature to typical processing temperatures (e.g. 1000 C) in times on the order of a second, LRP allows for high-temperature processing but still minimizes the thermal exposure of the substrate. For example, silicon epitaxial samples grown by LRP have doping profiles (as measured by SIMS) virtually identical to those grown by MBE, but also have electrical properties similar to those of virgin single crystal silicon substates.

In addition to the advantages of precise thermal control, by changing the process gases between high temperature cycles, multiple layers of different composition can be grown in-situ, i.e., without removing the wafer or breaking the vacuum seal of the system. Specific multilayer structures that have been investigated are doping superlattices, Si:Si/Ge strained layer superlattices, epitaxial silicon-oxide-doped polysilicon structures, and p-n junction structures. In most cases, electrical measurements have shown excellent interface properties. In-situ multilayer processing has the potential to avoid the inevitable particulate and chemical contamination that occur when wafers are transported from one reactor to another. Such considerations could be important for the uniformity and yield requirements of ULSI.

The silicon-oxide-doped polysilicon system forms the heart of modern MOS structures. Two level structures (oxide, doped polysilicon) were grown in situ for capacitor studies, and three level structures (selective epitaxial silicon, oxide, doped polysilicon) were fabricated for subsequent processing into MOS transistors. The resulting capacitors and sub-micron transistors both exhibit excellent characteristics, although the scale of experiments was too small to test for uniformity effects.

P-n junctions have been grown at both the substrate-epi and epi-epi interrupted growth interfaces. Placing junction depletion regions at these interfaces is a stringent test of their electrical quality. Cleaning procedures to remove interfacial contaminants have led to such junctions grown by multiple pulses with nearly ideal characteristics in forward bias ($n=1.05$) and low leakage currents. The extension of this work to all-epitaxial bipolar structures will also be presented.