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Laser-Solid Interactions and Transient Thermal Processing of Materials

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BEAM PROCESSING OF SILICON WITH A SCANNING CW Hg LAMP

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ABSTRACT

A scanning arc lamp annealing system has been built using a 3" long mercury arc lamp with an elliptical reflector. The reflector focuses the light into a high intensity narrow line source. Silicon wafers implanted with 100 KeV $^{75}As^{+}$ to $1x10^{15}$ cm^{-2} have been uniformly annealed with a single scan, resulting in complete activation and negligible redistribution of the implanted species. Using a scan rate of 1cm/s, entire 3" wafers have been annealed in less than 10 seconds with this system. The system has also been used to recrystallize thin films of polysilicon deposited on thermally grown silicon dioxide. The recrystallized films contain grains that are typically 0.5-1 mm in width and several centimeters long. Surface texture measurements show the crystallites to be almost entirely (100) in the plane of the film with the orthogonal <100> direction closely paralleling the scan direction. MOSFETs were fabricated in these films with surface mobilities 66% of ones fabricated in single crystal silicon. An epitaxial layer with the same crystallographic features as the recrystallized film was grown on the film itself.

INTRODUCTION

Over the past few years a considerable amount of research has been directed towards developing alternative heat treatment techniques for application to semiconductor processing. The most thoroughly investigated of these has been the use of pulsed and cw laser and electron beams [1]. Work performed using these sources has provided new insights into the mechanisms of thermally induced processes such as solid phase and liquid phase epitaxial growth and thin film recrystallization. In particular, some of the earliest work demonstrated that ion implantation damaged silicon could be annealed with a scanned cw laser such that there was complete electrical activation of the implanted species and virtually no impurity redistribution [2]. In addition, laser recrystallization of fine grain or amorphous films on insulating substrates was found to significantly improve the electronic properties of the film itself [3]. Once these processes were observed and understood, work began to identify alternative beam sources for producing these effects. In this paper we describe the results of using a high pressure Hg arc lamp system for large area annealing of ion implanted crystalline silicon and zone recrystallization of silicon thin films on insulating substrates. We also present data obtained from MOSFETs fabricated in the zone recrystallized film as well as describe the crystallographic features of an epitaxial layer grown on the film itself.

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ANNEALING SYSTEM

We have built an arc lamp annealing system which consists of a 3 inch long high pressure mercury lamp, an elliptically shaped reflector and a variable speed translation hot stage. In previous work xenon and krypton lamps were used. We chose to use a mercury lamp primarily for the following two reasons. First, the spectral distribution of this lamp is most heavily weighted in the uv range. Consequently, the mean absorption depth for this source is much shallower than that for the other lamps.

The second reason the mercury lamp was chosen over the other available lamps is due to the narrow capillary used for containing the discharge. For example, a typical 3" krypton lamp has a 5 mm capillary whereas the mercury lamp uses a 2 mm capillary. The tighter confinement results in a narrower imaged beam, and thus yields a higher intensity at the sample surface for a given lamp power.

The light from the lamp is focused into a narrow (< 5mm wide) ribbon by a 4" long reflector with an elliptical cross section. By using this shape of reflector to collect and focus the light, we can create an intense linear heat source and still maintain a reasonable working distance between the sample and the lamp. The reflector in our system has major and minor axes of 10cm and 8.6 cm respectively. This configuration gives a magnification factor of about 3.2 and a working distance of about 26mm between the edge of the reflector and the focal plane.

The samples are placed on a heated sample stage, over which the lamp can be translated at speeds up to 10cm/s. A schematic representation of the arc lamp annealing system is shown in Fig. 1.

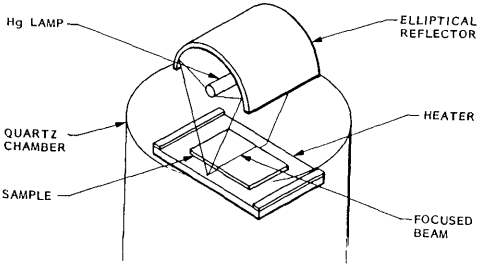

Fig. 1. Schematic representation of scanning cw arc lamp annealing system.

ARC LAMP ANNEALING OF ION IMPLANTED CRYSTALLINE SILICON

Arc lamp annealing of ion implanted silicon has several distinct advantages over other techniques, in particular laser annealing. First, because the light is incoherent, interference effects which result from the interaction of monochromatic light and the dielectric layers on the semiconductor material are eliminated. These effects can lead to nonuniform heating of the irradiated material if not eliminated. Second, the effective processing area for an arc lamp is orders of magnitude greater than that for a laser. For example, an entire silicon wafer can be arc lamp annealed in about 10 seconds, whereas a cw laser takes several tens of minutes to process the same amount of material. This single scan-large area processing also eliminates the periodic nonuniformities observed in raster scanned laser annealed materials. Finally, an arc lamp is significantly less expensive than a laser and is much more efficient to operate.

In the following section, we describe the results of using an arc lamp to anneal ion implanted silicon. We demonstrate that while it has the above advantages over laser annealing, it also provides the benefits of beam annealing over conventional furnace annealing. Specifically it results in high quality, solid phase epitaxial regrowth with complete activation of the implant species and no dopant redistribution.

Annealing experiments were carried out using 2 and 3 inch 1-8 Ω-cm p-type (100) silicon wafers which were implanted with $^{75}As^{+}$ at 100keV to 1 x $10^{15}cm^{-2}$. It was found that several combinations of arc lamp power, scan rate and substrate temperature could be used to achieve a wafer temperature sufficient for good annealing, ~ 1000°C. In general, scan rates from 5mm/s to 1cm/s, substrate temperatures of 400°C to 600°C and arc lamp input power of 1kW/inch to 1.5kW/inch gave good results.

Because of the length of the arc lamp, an entire wafer can be annealed in a single scan. Figure 2 is a photograph of a 3" wafer in which the scan was stopped at the center of the wafer. Because of the difference in reflectivities between single crystal and amorphous silicon, the demarcation between the annealed and unannealed regions is readily seen. Transmission electron microscope (TEM) diffraction patterns made from samples taken from the unannealed and annealed regions clearly indicate the amorphous and completely recrystallized nature of the regions, respectively. (The picture is somewhat distorted due to the angle at which the photo was taken.)

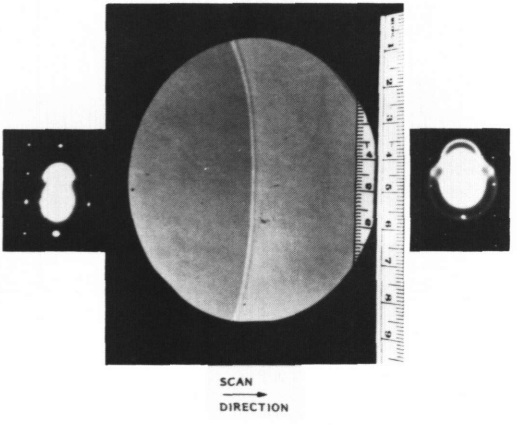

Fig. 2. Photograph of partially annealed silicon wafer, and TEM diffraction patterns from the annealed and unannealed regions.

The recrystallized layer was also analyzed by Rutherford Backscattering Spectroscopy (RBS) and directly compared to a sample which was thermally annealed at 850°C for 30 minutes followed by a 10 second 1000°C anneal. Figure 3 shows the backscattering spectra from an as-implanted, arc lamp annealed and thermally annealed sample. As shown, there is no detectable difference between the quality of the regrown material annealed by the scanned arc lamp and the thermally processed sample.

Carrier concentration and mobility of the arc lamp annealed material as a function of depth were determined by means of differential sheet resistivity and Hall effect together with an anodic oxidation stripping technique. These

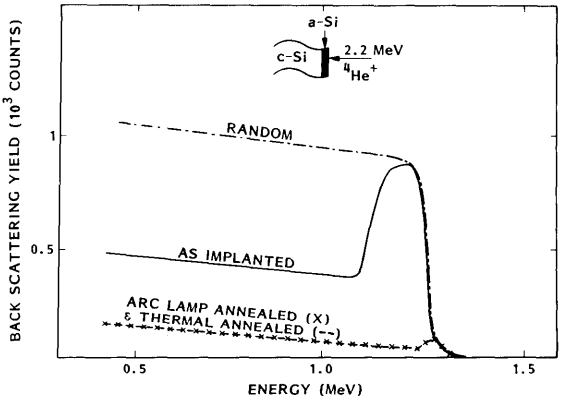

Fig. 3. Rutherford backscattering spectra from as-implanted, arc lamp annealed and thermally annealed samples.

results are shown in Fig. 4, along with the as-implanted profile calculated using LSS theory and published bulk silicon mobilities for the respective impurity concentrations. As shown, no measurable dopant redistribution occurred during the annealing process and the free carrier mobility in the annealed region is as good as found in bulk silicon.

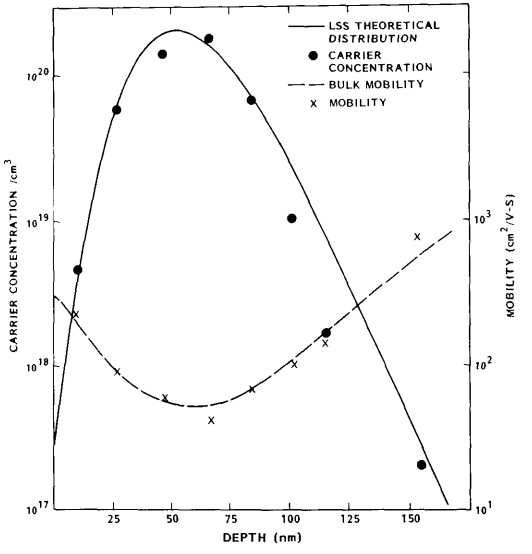

Fig. 4. Carrier concentration and mobility versus depth from an arc lamp annealed sample.

To assess the uniformity of the anneal, four point probe sheet resistivity measurements were made on a wafer which was completely annealed in a single scan. The variation across the wafer from side to side and top to bottom (with respect to the scanning beam) showed no significant variation in either direction, indicating a very uniform annealing of the implanted wafer. These data are shown in Fig. 5.

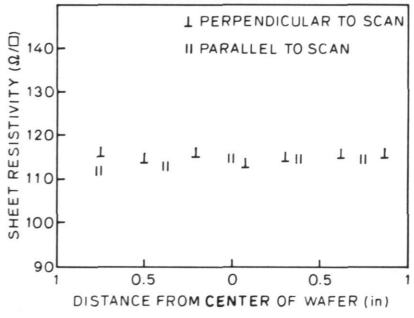

Fig. 5. Sheet resistivity profiles across an arc lamp annealed wafer.

High resolution transmission electron microscopy (TEM) was used to compare the residual dislocation density in arc lamp annealed material to material which was furnace annealed at 1000°C for 1 hour in N_2.

In Fig. 6 we compare the results of a sample which was annealed using 1 kW/inch lamp power, a scan rate of 7 mm/s and a substrate temperature of 450°C, to one which was thermally annealed. As shown the residual dislocation density is approximately the same in both cases.

Deep level transient spectroscopy has also been performed on these samples and compared to furnace annealed as well as other beam (e.g., laser and electron) annealed samples [4]. These results indicate that the arc lamp annealed material has approximately an order of magnitude lower defect density and does not contain the principle defect species identified in the other beam processed material.

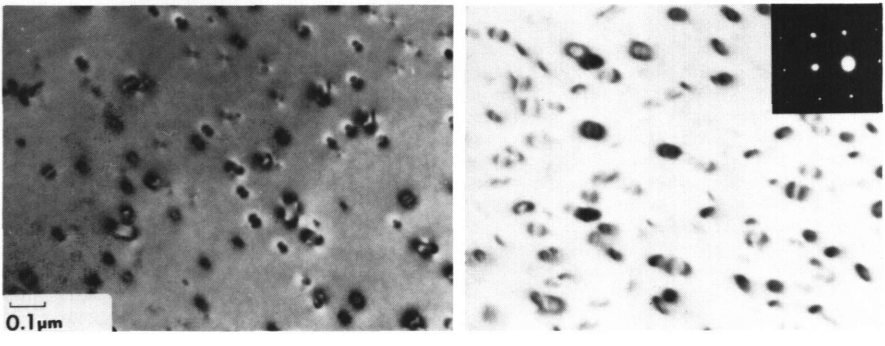

Fig. 6. Bright field TEM micrographs of (a) furnace annealed (1000°C, 1 hr.) and (b) arc lamp annealed samples.

In summary, arc lamp processing of ion implanted silicon provides fast, high quality annealing of the damaged material, complete dopant activation and no redistribution of the dopant species.

RECRYSTALLIZATION OF THIN POLYSILICON FILMS ON SiO_2

Fabrication of device worthy silicon thin films on insulating substrates has been an active area of research for many years. One of the most successful approaches for obtaining this material is by recrystallizing as-deposited fine grain or amorphous films into large grain or single crystal material.

Over 30 years ago zone melting was shown to be an effective grain enlarging recrystallization technique for thin films [5]. In that work, a platinum wire was used to zone melt and recrystallize films of luminescent material on insulating substrates. By 1966 several researchers had grown large grain germanium thin films using an electron beam for the zone melting process [6-9]. More recently, lasers [10,11] and graphite strip heaters have been used for zone melting of silicon films [12-14].

In this section we show that a scanned, high pressure mercury lamp can be used for zone melting and recrystallization of silicon thin films on insulating substrates.

The samples used for these experiments were thermally oxidized single crystal silicon wafers upon which polycrystalline silicon films had been deposited using low pressure chemical vapor deposition (LPCVD). The thermal oxide was 1 μm thick and the deposited silicon film was 600 nm thick. Finally, the films were encapsulated with 1 μm-2 μm of CVD SiO_2.

Three parameters controlling the zone melting process were investigated; arc lamp power, starting substrate temperature and zone scan rate. Although a variety of combinations of these parameters could be used to achieve a molten zone in the deposited film, the following general observations were made.

If the scan rate was too fast and/or the lamp power-substrate temperature combination was too low, partial melting of the film and/or severe agglomeration would occur. If the starting substrate temperature was too low, the substrate would be highly damaged after the recrystallization process, exhibiting a large number of slip lines. If the combination of substrate temperature and lamp power was too high, melting of the underlying single crystal substrate would occur. Finally, within the operating region of a stable molten zone, an increase in scan rate was found to increase the spacing between the subgrain boundaries.

Our best results to date were obtained using a lamp power of 1 kW/inch, a substrate temperature of 1150° C and a scan rate of 3 mm/s. The following results were obtained under these experimental conditions.

The zone recrystallized films using our system exhibited features similar to those found in zone recrystallized films using other techniques. The film consisted of very large grains, typically 0.5 mm to 1 mm in width and up to several centimeters long. These large grains were obtained without using any intentional seeding techniques. Such techniques have been shown to eliminate large angle grain boundaries and yield a film composed entirely of low angle grain boundaries [12]. The individual grains were composed of many subgrains, with subgrain boundaries typically from 50 μm to 100 μm apart. Figure 7 is an optical photomicrograph of a section of recrystallized film which has been Secco [15] etched to delineate the subgrain boundaries. In Fig. 8 we show a scanning electron micrograph which was taken under channeling contrast conditions. This figure clearly indicates that the surface normals of the regions separated by the subgrain boundaries have slightly different orientations.

Because of the large grain size in the recrystallized films, conventional crystallographic techniques for evaluating the structure of the films are very time consuming and complex. This is because the incident beam, i.e., electron

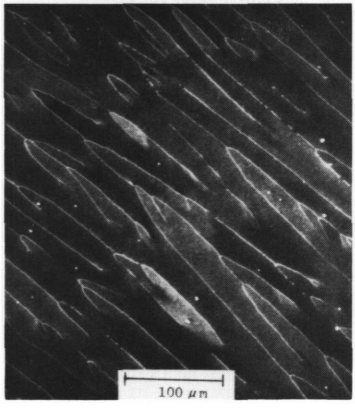

Fig. 7. Photomicrograph of zone re-recrystallized film which has been Secco etched to delineate the sub-grain boundaries.

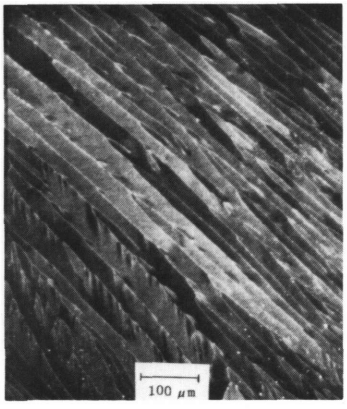

Fig. 8. Scanning electron micrograph of zone recrystallized film taken under channeling contrast conditions.

or X-ray, is smaller than or on the order of the average grain size of the material. Consequently the data obtained from a single diffraction pattern is representative of at most a few grains. Thus in order to obtain any statistically meaningful information about the crystallographic composition of the film, many patterns over a large area of the film must be taken and analyzed.

Geis et al. have described a technique for observing the orientation and size of large grains in zone recrystallized films by using an anisotropic etch in combination with a square array of etch pits [16]. We have used this approach to evaluate our zone recrystallized film. Using conventional photolithographic techniques, round holes on 50 μm centers were fabricated in the SiO_2 encapsulant after the underlying material was zone recrystallized. The samples were then immersed in a 50% by weight solution of KOH in DI H_2O at 80° C for 6 - 8 minutes. This solution preferentially etches in the <110> direction [22]. Consequently the symmetry and alignment of the etch pits can be related to the crystallographic nature and in-plane orientation of the grains being etched.

Figure 9 is a photomicrograph of a recrystallized film which has been preferentially etched in the manner described above. The first feature to note is that the etch pits are square, indicating a <100> surface texture of the film. We have also observed hexagonally shaped etch pits in some of our films which indicates a <111> texture. However, this texture was found only in some very localized areas and on just a few samples. All the material we have recrystallized has exhibited predominantly a <100> texture.

The second feature to notice is that the etch pit diagonals closely parallel the zone scan direction, indicating a <100> texture in the growth direction. Also shown in Fig. 9 is a grain boundary as evidenced by the misalignment of the etch pits on either side.

DEFECTS IN ZONE RECRYSTALLIZED FILM

The principal defects we have observed in the zone recrystallized film and/or substrates are: (1) slip and warpage, (2) substrate melt through, (3) protrusions, (4) voids and (5) agglomeration or dewetting.

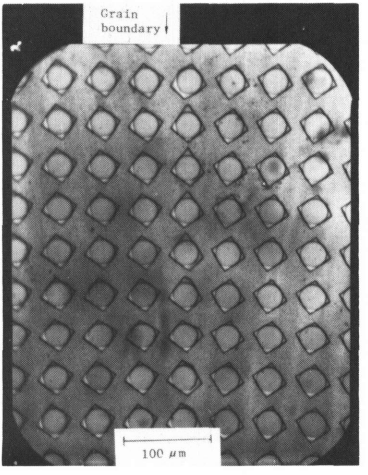

Fig. 9. Photomicrograph of zone recrystallized film illustrating misalignment of etch pits due to the presence of a grain boundary.

Slip and warpage damage to the single crystal silicon substrate are a result of the large thermal stresses the substrate sees during the processing. In general, higher substrate temperatures and very uniform substrate heating reduce or eliminate these problems.

When the molten zone (or an area of it) becomes too hot, melting of the crystalline substrate beneath it can occur. Under these conditions the thermal oxide can rupture resulting in a large 'melt through' pit, where the surface film and substrate have fused together. This is shown in Fig. 10(d).

If the film to be recrystallized contains impurities, they can segregate to the sub-boundaries during the solidification process. This segregation will depress the melting tmeperature of the film in that region. Consequently, it will solidify after the zone front has passed that region and the neighboring film has solidified. Since silicon has a positive expansion coefficient upon solidification, these small molten areas which are constrained by the surrounding solid silicon must expand upward, resulting in small protrusions at the surface of the film. Figure 10(b) illustrates this case. Note how the protrusions all lie along the low angle grain boundaries. In general, clean material, reduced scan speeds and steep thermal gradients will prevent this defect.

We have also observed small areas in the zone recrystallized film where the film has thinned out and exposed the underlying thermal oxide. These 'voids' are believed to be a result of some local contamination at the interface between the oxide and the deposited film. Figure 10(c) is a photomicrograph of this defect.

The last defect, agglomeration and dewetting is a gross feature which generally renders the film useless. This is the case when the film balls up or gathers into separate unattached regions, as shown in Fig. 10(a). The driving force for this reaction is the minimizing of free energy by reducing the surface to volume ratio of the film. The encapsulation layer is intended to minimize or eliminate this effect. Some investigators have found that two layer encapsulants (18) are more effective than the single layer SiO_2. We have observed, however, that some deposited films are less prone to agglomeration than others and can be relatively insensitive to the encapsulant. In either case, this problem is perhaps the most demanding and the solution must be understood and universally reproducible if this process is to become a useful technique.

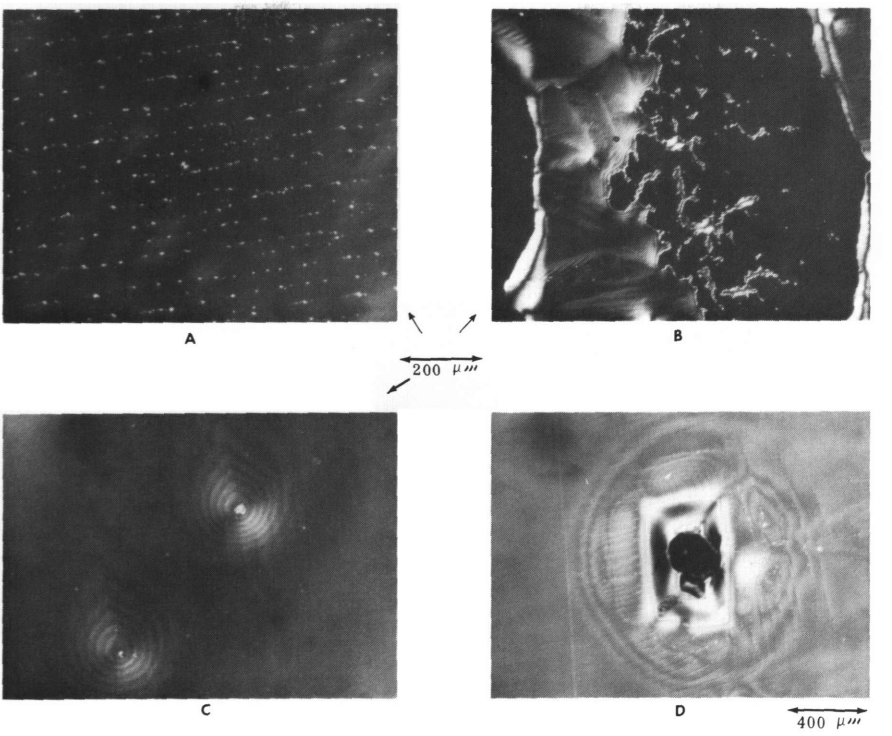

Fig. 10. Defects in zone recrystallized films (a) agglomeration, (b) protrusions, (c) voids, and (d) substrate melt through.

MOSFETS IN ZONE RECRYSTALLIZED FILM

In order to investigate the electronic properties of the zone recrystallized films, n-channel metal-oxide-semiconductor field-effect-transistors were fabricated using an aluminum gate process. The transistors had channel lengths of 10 μm, 20 μm and 50 μm with all channel widths being 200 μm. The transistors were fabricated such that there were channels running both parallel and perpendicular to the low angle grain boundaries. In this way the effect of the low angle boundary orientation on the channel mobility could be assessed. Channel implants of 1.5×10^{11} cm^{-2} boron and phosphorus were used for the enhancement and depletion mode devices, respectively. The implants were thermally annealed under such conditions as to insure a uniform dopant distribution through the film thickness, yielding a net impurity concentration of 2×10^{15} cm^{-3}. The gate oxide thickness was 1000 Å and all devices were isolated by an island etch.

A circular bulk resistor pattern was also included to evaluate bulk properties of the film. Resistivity data obtained from these devices indicate that there was complete activation of the phosphorus implant and single crystal bulk mobilities in the film. Surface mobility data were obtained by analyzing transistor IV characteristics from a curve tracer. In Table I we summarize the surface mobility data obtained from the MOSFETs. As shown, the average

TABLE I
Summary of N-channel MOSFET surface mobilities (cm^2/V-S)

Channel Length + Direction	Arc Lamp Recrystallized		Single Crystal Control Enhancement
	Enhancement	Depletion	
50 μm parallel	436	334	537
50 μm perpendicular	418	399	
20 μm parallel	--	432	573
20 μm perpendicular	382	415	
10 μm parallel	345	332	591
10 μm perpendicular	335	357	

Conclusions: no sub-boundary orientation effects on surface mobility.

surface mobilities for the enhancement and depletion mode devices in the zone recrystallized film ranged from 335 cm^2/V-s to 436 cm^2/V-s. No systematic variation due to low angle grain boundary orientation or channel length was observed. Included in Table I are the surface mobilities of enhancement mode devices simultaneously fabricated in single crystal material. The average mobility for these devices is 567 cm^2/V-s. Thus the transistors fabricated in the recrystallized film had surface mobilities approximately 66% of those fabricated in single crystal material.

EPITAXIAL LAYERS ON ZONE RECRYSTALLIZED FILM

Although 0.5 μm silicon films can be used for MOSFET devices, thicker films are desirable for bipolar applications. In light of this need, a 14 μm epitaxial layer was grown on a 0.5 μm zone recrystallized film. The sample preparation and zone recrystallization were performed as described in the previous section. After processing, the 2 μm SiO_2 encapsulation layer was removed from the sample. The sample was then cleaned and placed in a standard conventional epitaxial reactor.

It was found that the epitaxial layer replicated and enhanced the surface features of the zone recrystallized film. In particular, the low angle grain boundaries were clearly evident in the topography of the epitaxial layer. Figure 11 is a Nomarski photomicrograph of the surface of the film illustrating these features. Diffraction patterns of epitaxial layers grown on as-deposited as well as zone recrystallized material were taken using a Read camera. These patterns, shown in Fig. 12, clearly indicate that while the layer grown on the as-deposited film is fine grained with no preferred orientation, the layer grown on the recrystallized film is large grained and highly oriented. In order to evaluate the macroscopic crystallographic features of the epitaxial layer, the preferential etch pit method previously described was used. These results are presented in Fig. 13. As shown, there are no facets in the etch pits formed in the layer grown on the as-deposited film. However the etch pit pattern in the layer grown on the recrystallized film clearly indicates a (100) film orientation. The photomicrograph shown in the lower portion of Fig. 13 was taken using light scattered off the sample surface. All the etch pits within a single grain will have their facets aligned. This alignment however will vary from grain to grain. Thus this technique can be used to

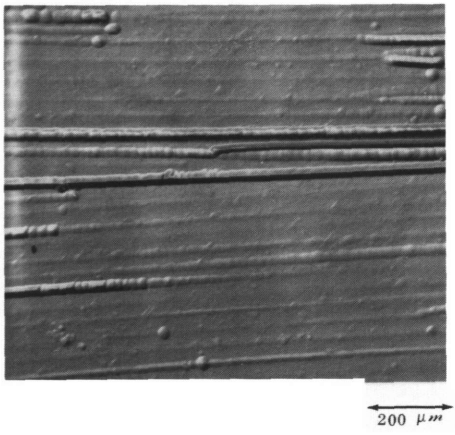

Fig. 11. Nomarski photomicrograph of surface of epitaxial layer grown on zone recrystallized film.

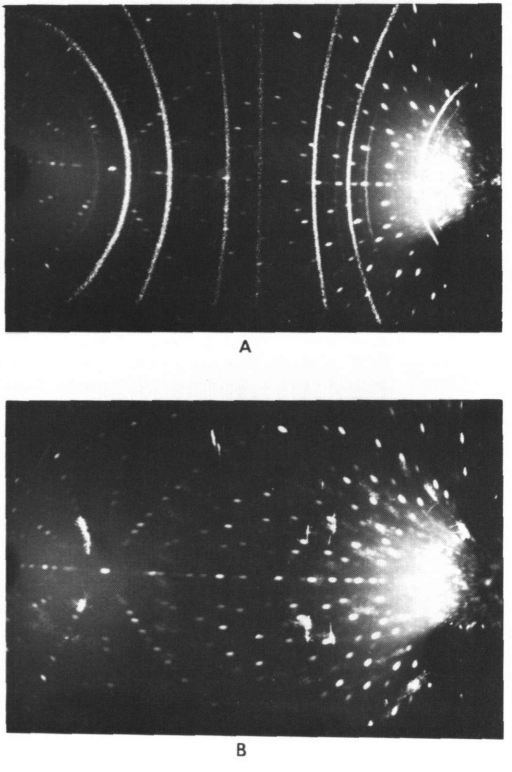

Fig. 12. READ camera diffraction patterns from (a) epi on as-deposited film, (b) epi on zone recrystallized film.

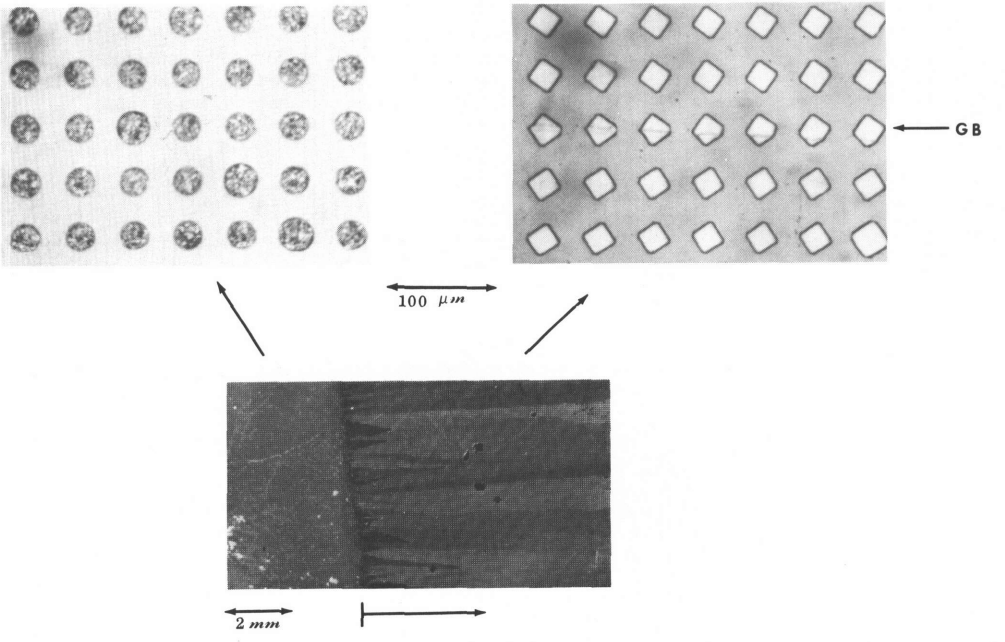

Fig. 13. Etch pits and scattered light photo of epi on zone recrystallized film.

delineate and observe the grains in the film. As shown, the grains in the epitaxial layer tend to be 0.5 mm to 1 mm in width, as was observed in the zone recrystallized films.

In summary, an epitaxial layer which replicates the surface and crystallographic features of a zone recrystallized thin film substrate have been grown. Work in progress includes evaluating the electronic properties of these epitaxial layers.

SUMMARY

We have built a scanning Hg arc lamp system which can be used for thermal processing of semiconductor materials. The Hg lamp was chosen over other available high intensity sources due principally to its large near UV spectral content which results in better optical coupling with the silicon being processed. The scanning Hg arc lamp system was used to anneal ion implanted silicon and to zone recrystallize silicon thin films on insulating substrates. The annealing experiments have demonstrated that Hg lamp irradiation can produce a high quality diffusionless anneal in less than 15 seconds. The recrystallization experiments have demonstrated that large grain, highly oriented thin films of silicon on amorphous substrates can be produced using this system.

The recrystallized film had a (100) in plane orientation and exhibited a <100> texture in the direction of the zone scan. Enhancement and depletion mode MOSFETs were fabricated in the zone recrystallized film. The electron surface mobilities were greater than 60% of those measured in devices fabricated in single crystal silicon, demonstrating that the electronic properties of the film are suitable for device applications. Finally, a 14 μm epitaxial layer was grown on a zone recrystallized film. This layer contained the same crystallographic features as the zone recrystallized film used as a substrate and has potential for bipolar device applications.

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