FED-73

PROCEEDINGS OF 7TH SYMPOSIUM ON FUTURE ELECTRON DEVICES

次世代産業基盤技術

—第7回新機能素子技術シンポジウム—

予　稿　集

NOVEMBER 1-2 1988
JYOSUI KAIKAN
HITOTSUBASHI, TOKYO, JAPAN

昭和63年11月1日(火)～2日(水)
一ツ橋　如水会館

SPONSORED BY
THE RESEARCH & DEVELOPMENT ASSOCIATION FOR FUTURE ELECTRON DEVICES
THE JAPAN INDUSTRIAL TECHNOLOGY ASSOCIATION

SUPPORTED BY
THE AGENCY OF INDUSTRIAL SCIENCE AND TECHNOLOGY, MITI

主　催　財団法人 新機能素子研究開発協会
　　　　財団法人 日本産業技術振興協会
後　援　通商産業省工業技術院

7TH SYMPOSIUM ON FUTURE ELECTRON DEVICES
November 1-2, 1988 Tokyo, Japan pp. 179-184

DEVICE PHYSICS AND PERFORMANCE ADVANTAGES OF THIN SOI MOSFETs FOR FUTURE VLSI (INVITED)

J. C. STURM
Princeton University

ABSTRACT

Enhanced transconductance has been observed in fully depleted silicon-on-insulator (SOI) MOSFET's compared to otherwise similar bulk structures. The cause of the effect is the reduced vertical electric fields in fully-depleted SOI. In this paper, the role of the underlying oxide thickness and the drain saturation voltage are examined. Channel length scaling is also examined. It is found that with all other variables held constant, entering the regime of velocity saturation will reduce the current enhancement. However, lightly doped films offer the possibility of maintaining the increased transconductance in the submicron regime.

INTRODUCTION

The traditional advantages of silicon-on-insulator technology have been low substrate nodal capacitances, device isolation, and radiation hardness. Over the last few years, however, many additional advantages of SOI for the scaling of VLSI MOSFET's have been discovered. These effects include short-channel threshold voltage stability and improved subthreshold slopes [1,2]. These improvements generally require ultra-thin SOI films (~0.1 um). Recently, a new advantage of improved transconductance in these ultra-thin films has been described [3]. This paper will review this effect and then further examime the behavior of drain saturation voltage and the dependence of transconductance enhancement on the underlying oxide thickness. Finally, the behaviour of the effect as channel lengths are scaled to the micron range will be explored.

SUBSTRATE ELECTRIC FIELDS AND DRAIN CURRENT

In the MOS structure, the electric field supplied by the gate voltage must support both the charge in the channel and the ionized dopant in the underlying substrate depletion region (substrate charge). In a bulk FET, as one moves from the source to the drain end of the channel this substrate charge grows as the channel-substrate depletion region grows. Hence at the drain end of the device the gate electrode supports more substrate charge than it does at the source end. Since this substrate charge gives rise to a vertical electric field, the effect can be graphically exhibited by plotting the vertical electric field versus depth at both ends of the device. This is done in fig. 1 using the PISCES-IIB two-dimensional simulator [4] for a "long-channel" device with a gate oxide thickness of 20 nm and a uniform substrate doping of 4 x 10^{16} cm^{-3}, and an operating condition of V_g-V_t = 3.0 V and V_{ds} = 2.5 V. The sharp drop in vertical electric field near the Si-SiO_2 interface (x=0) represents the inversion layer of mobile carriers. Its absence at the drain end of the device indicates the onset of saturation. Note that the substrate field just under the inversion layer is twice as large at the drain end of the device compared to the source end. This rise in substrate charge as the channel-substrate voltage grows is precisely what causes the body effect.

The case can be quite different in a silicon-on-insulator FET. If the film is fully depleted when the device is on, all acceptors (in an n-channel device) in the SOI film will already be ionized at the

7TH SYMPOSIUM ON FUTURE ELECTRON DEVICES
November 1-2, 1988 Tokyo, Japan pp. 179-184

threshold condition. Thus any additional vertical field lines under the channel must terminate underneath the underlying oxide at the substrate. If this oxide is thick, the field in the oxide is effectively zero for finite voltages across it [3]. Hence the vertical electric field should be pinned to zero at the bottom $Si-SiO_2$ interface. This condition is simulated in fig. 1b. for a SOI device with the same channel doping, gate oxide thickness, and voltage conditions as the earlier bulk device. The SOI film thickness is only 80 nm, and the underlying oxide is 2 um. With such a thin SOI thickness, the silicon film is fully depleted when the device is on in steady state for a grounded substrate. Since the substrate electric field does not grow from source to drain, the SOI device will have more electric field from the gate available to terminate on channel carriers. More carriers in the channel should lead to enhanced current and hence enhanced transconductance.

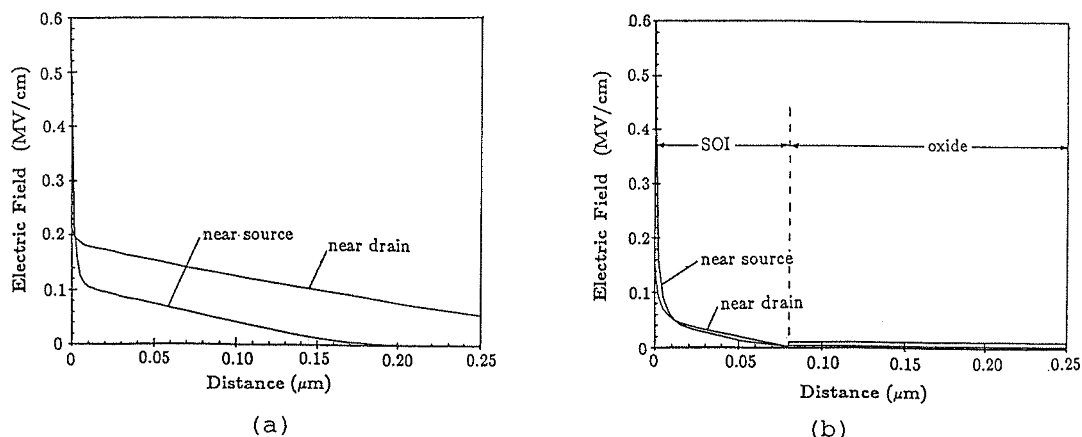

Fig. 1. Vertical electric field in a long-channel MOS transistor near the source and drain ends of the device for (a) a bulk device and (b) a device in an 80-nm SOI film on a 2-um oxide. ($N_A = 4 \times 10^{16}$ cm^{-3}, gate oxide thickness = 20 nm, $V_s = V_{subs} = 0$, $V_d = 2.5$ V, $V_g-V_t = 3.0$V.)

A second physical phenomenon affecting current is the confinement of carriers against the $Si-SiO_2$ interface by the vertical electric fields. As the vertical field (and hence confinement) is increased, the surface mobility is known to decrease due to increased surface and phonon scattering. Thus, fully depleted SOI films should also have the advantage of increased mobility over their bulk counterparts. This advantage is distinct from the first advantage mentioned earlier which describes only the number of carriers in the channel. The details of these mechanisms are more fully described in [3]. A transconductance improvement of roughly 40% was predicted for the geometries described earlier.

As an experiment, FET's were fabricated in 100 nm SOI films (created by the SIMOX process) and simultaneously in bulk films. The gate oxide thickness was 25 nm and the bulk channel and SOI film doping was 1×10^{17} cm^{-3}, close to the conditions described for the earlier simulations. The buried oxide thickness was estimated at 350 nm. Data shown in fig. 2 for 20um/8um devices shows about a 30% increase in transconductance. This is somewhat less than predicted, but the SIMOX films were annealed at only 1250 C, lower than is commonly used for optimal SIMOX annealing [5,6]. Further, the underlying oxide was not as thick as that used for the simulations. The effect of this oxide thickness will be described in the next section.

7TH SYMPOSIUM ON FUTURE ELECTRON DEVICES
November 1-2, 1988 Tokyo, Japan pp. 179-184

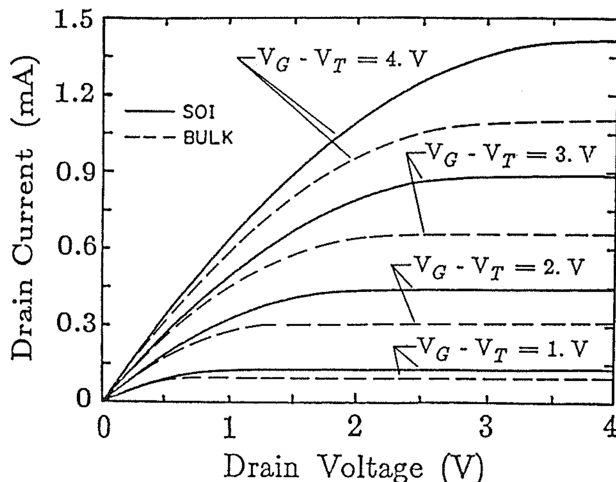

Fig. 2. Curve-tracer characteristics (data) for bulk and 100-nm SOI MOSFET's. The bulk threshold voltage is 0.7 V and the SOI threshold is 0.2 V. Sources and substrates were grounded in both cases.

EFFECT OF UNDERLYING OXIDE THICKNESS

In deriving the original expressions for the fully depleted SOI MOSFET [3], it was assumed that the underlying oxide was infinitely thick to force electric fields in it to zero. It is thus important to investigate how practical cases of thinner oxides will affect the current enhancement. We will assume n-channel FET's with worst case boundary conditions underneath the underlying oxide: an n-type or heavily doped p-type substrate so that there is little potential drop in the underlying substrate. Since the SOI film is fully depleted, we may define an effective capacitance C_{sub} representing the coupling between the top inversion channel and the underlying substrate. C_{sub} is the series capacitance of the SOI film and the underlying substrate,

$$C_{sub} = \frac{1}{\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{SOI}}{\epsilon_{Si}}} \quad (1)$$

where t_{ox} is the underlying oxide thickness and t_{SOI} is the SOI thickness. In the gradual channel approximation, we can then write the basic condition for the inversion layer charge density (Q_I) as a function of channel voltage (V_{chan}) as

$$Q_I = (V_g - V_t - V_{chan})C_{gate} - V_{chan} \cdot C_{sub} \quad (2)$$

V_t is the threshold voltage defined for $V_{chan} = 0$, C_{gate} is the gate oxide capacitance, and V_g is the gate voltage. The drain saturation condition occurs when $Q_I = 0$, and the drain saturation voltage $V_{DS,SAT}$ then is

$$V_{DS,SAT} = (V_g - V_t)\frac{C_{gate}}{C_{sub} + C_{gate}} \quad (3)$$

Thus when the substrate is infinitely thick ($C_{sub} = 0$), $V_{DS,SAT} = V_g - V_t$ as the ideal case. Using (2) and the gradual channel approximation, one can easily show

7TH SYMPOSIUM ON FUTURE ELECTRON DEVICES
November 1-2, 1988 Tokyo, Japan pp. 179-184

$$I = \frac{W}{L} \mu \left[C_{gate}(V_g - V_T)V_{ds} - (C_{gate} + C_{sub}) \frac{V_{ds}^2}{2}\right] \quad (4)$$

Substituting (3) into (4) then yields the drain saturation current,

$$I_{DS,SAT} = \frac{W}{2L} \mu \, C_{gate}(V_g - V_t)^2 \left(\frac{C_{gate}}{C_{gate} + C_{sub}}\right) \quad (5)$$

From (5) one may easily calculate $I_{DS,SAT}$ as a function of underlying oxide thickness. For example, for a 25 nm gate oxide and a 100 nm SOI thickness, an underlying insulator thickness of 350 nm will give a drain saturation current which is 94% of the maximum value. This may partially explain why the transconductance enhancement in fig. 2 is somewhat less than predicted for a 2 um underlying oxide thickness which would give a saturation current of about 99% of the maximum value according to (5).

DRAIN SATURATION VOLTAGE

It is readily apparent from the data in fig. 2 that the drain saturation voltages of the SOI transistor are considerably larger than those of the bulk transistor. This is understood in terms of the reduced vertical fields as shown in fig. 1. By extrapolating dI_d/dV_{ds} to zero, one can accurately extract $V_{DS,SAT}$ from the curve-tracer characteristics. These results are shown in fig. 3. Although the drain saturation voltages of the SOI transistor are over 20% larger than those of the bulk, they are not quite equal to the ideal V_g-V_t. For example, at V_g-V_t = 4.0 V, $V_{DS,SAT}$ = 3.7 V. This difference can be explained by the finite thickness of the underlying oxide as described in the previous section. Using (3) and an underlying oxide thickness of 350 nm, one would expect $V_{DS,SAT}$ = 3.75 V, in excellent agreement with the data.

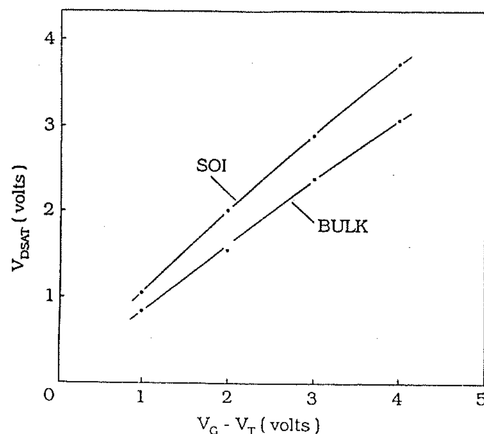

Fig. 3. Drain saturation voltage as a function of V_g-V_t, extracted from the data of fig. 2.

The increased drain saturation voltage is emphasized separately from increased transconductance since it may lead to reduced hot electron effects. Classically, high-field pinch-off regions occur only for $V_{DS} > V_{DS,SAT}$. Hence an increased $V_{DS,SAT}$ may lead to reduced high-field regions and reduced hot electron effects. Indeed, there has been one report of reduced hot electron degradation in n-channel fully-depleted SOI FET's compared to bulk structures [7]. Further work in this area is needed.

CHANNEL LENGTH SCALING

All simulations and data presented up to this point have been for long-channel structures. Excessive contact resistance prevented any useful measurement of micron-scale transistors on the same run as the long-channel FET's described earlier. Hence two-dimensional simulations using PISCES-IIB were performed. The test parameters used were a 20 nm gate oxide and a 5 x 10^{16} cm^{-3} channel doping for both the SOI and bulk transistors. The SOI underlying oxide was 1 um, and the SOI thickness was 0.14 um, which corresponds to the fully depleted condition. Low-field mobilities of 500 cm^2/Vs were used for both devices, and velocity saturation was incorporated through a tangential field-dependent mobility. The perpendicular field dependence of mobility described earlier was not accounted for because of the difficulty in incorporating such effects into a 2-D simulator. The results are shown in fig. 4 in the form of the ratio of the SOI saturation current to the bulk saturation current for equal bias conditions as a function of channel length. It can be seen that in the 1-um range, the SOI transconductance enhancement is decreased for large drain voltages. By turning off the tangential field-dependent mobility, it was confirmed that this reduction was due to velocity saturation effects. Hence velocity saturation will tend to limit the usefulness of the transconductance enhancement mechanisms for short-channel devices for VLSI if the SOI devices are made with the same channel doping as the bulk devices.

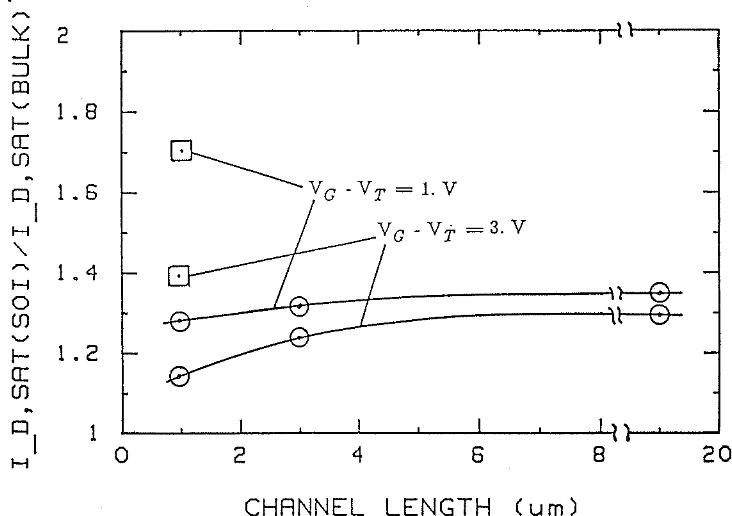

Fig. 4. SOI transconductance enhancement for two different bias conditions as a function of channel length. The simulation parameters are given in the text. Circles correspond to a SOI channel doping of 5 x 10^{16} cm^{-3} and the squares correspond to a channel doping of 1 x 10^{15} cm^{-3}

In the micron or submicron range, bulk FET's require a considerable channel doping to avoid punchthrough or drain-induced barrier lowering. In a thin SOI film (<100 nm) however, the gate strongly controls the potential distribution in the SOI film. For example, it is easily confirmed by simulation that a 1-um n-channel device in a 100-nm SOI film with only 1 x 10^{16} cm^{-3} acceptor doping is easily turned off with V_{ds} = 5 V. The advantage of lightly doped films is the enhanced electron mobility due to the reduced surface electron confinement described in the beginning of this paper. Although this effect is not easily quantified when the device is two-dimensional, we may make a rough estimate of the magnitude of the effect by using the peak low-field surface mobilities from Sun and Plummer [8]. Their data shows approximately a mobility of ~860 cm^2/Vs for N_A = 1 x 10^{15} cm^{-3} and a mobility of ~575 for N_A = 5 x 10^{16} cm^{-3}. Applying these mobilities to

the simulator for a channel length of 1 um, one finds a 54% current enhancement for the lightly-doped SOI over bulk for $V_g-V_t = 1$ V and a 30% increase for $V_g-V_t = 3$ V (fig. 4). Thus by using lightly doped films, SOI FET's should retain their transconductance enhancement advantages over bulk even at short channel lengths.

Using light doping in the SOI films should also enable one to avoid transient current overshoot effects which can occur during switching of fully depleted SOI FET's [9]. These transients are due to holes which are displaced from the SOI body during the turn-on of the FET. Light doping in the SOI film removes the source of most of the holes. However, undoped or lightly doped SOI films make the threshold voltage almost independent of film thickness. While this is useful from a manufacturing point of view if the film thickness is not well controlled, it requires one to use the gate work function to adjust the threshold voltage. p^+ polysilicon gates for n-channel devices (and vice versa) may be required.

SUMMARY

Current enhancement mechanisms in ultra-thin silicon-on-insulator MOSFET's have been explored. Reduced substrate electric fields lead to more electrons in the channel, increased surface mobilities, and increased drain saturation voltages. The magnitude of these effects depends on an adequate underlying oxide thickness. Finally, submicron scaling of SOI transistors will be most advantageous when lightly doped thin films are used. In addition to circuit and manufacturing advantages, they offer the greatest opportunity for increased transconductance.

ACKNOWLEDGEMENTS

The authors would like to thank J.P. Colinge for supplying the transistor samples. The work was made possible by support from the New Jersey Commission on Science and Technology, NSF (PYI), and IBM, and by donations from Rucker and Kolls, Olympus, Sloan Corp., and Hewlett Packard.

REFERENCES

1. J.-P. Colinge, presented at the 1987 IEEE SOS/SOI Workshop, Durango CO, October, 1987.
2. J.-P. Colinge, IEEE Electron Dev. Lett., EDL-7, 247 (1986).
3. J.C. Sturm, K. Tokunaga, and J.-P. Colinge, IEEE Electron Dev. Lett., EDL-9, 460 (1988).
4. M.R. Pinto, C.S. Rafferty, and R.W. Dutton, Stanford Electron. Lab., Stanford, CA, (1984).
5. C. Jassaud, J. Margail, J. Stoemenos, and M. Bruel, Proc. Symp. Mat. Res. Soc., 107, 17 (1988).
6. B.-Y. Mao, M. Matloubian, C.-E. Chen, R. Sundaresan, and C. Slawinski, IEEE Electron Dev. Lett., EDL-8, 306 (1987).
7. J.-P. Colinge, IEEE Trans. Elec. Dev, EDL-34, 2173 (1987).
8. S.C. Sun and J.D. Plummer, IEEE Trans. Elec. Dev., ED-27, 1497 (1980).
9. M. Yoshimi, T. Wada, K. Kato, and H. Tango, Tech. Dig. IEDM, 640 (1987).