MATERIALS RESEARCH SOCIETY
SYMPOSIA PROCEEDINGS

VOLUME 53

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Symposium held December 3-6, 1985, Boston, Massachusetts, U.S.A.

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MATERIALS RESEARCH SOCIETY
Pittsburgh, Pennsylvania

Materials Research Society Symposium C, Boston, MA, Dec. 3-6, 1985

A SEEDED CHANNEL APPROACH TO SILICON-ON-INSULATOR TECHNOLOGY

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ABSTRACT

A seeded channel approach was developed to avoid the short comings of the conventional SOI structure such as grain or sub-grain boundaries in the channel region, floating substrate effects, etc. In this approach, the gate of each FET is located above its own seed window to insure that single crystalline material is obtained for the channel region. The source and drain regions, however, are located in the recrystallized silicon over SiO_2 for improved isolation and minimizing junction capacitance. Recrystallization was obtained in 4" silicon wafers by using an Ar laser and a computer controlled X-Y stage with heated substrate holder. Problems encountered in laser recrystallization, such as, reflectivity variations over seed and SOI regions, surface ripples, pittings, etc., were eliminated by optimizing the thin film thickness of the isolation oxide, polysilicon, and the capping oxide. This technology was used successfully to fabricate FET devices using a standard production n-MOS process. Good device characteristics were obtained using 400Å gate oxide and channel length ranging from 1um to 50um. The measured electron mobility in the channel region is, however still lower than the ideal bulk values.

INTRODUCTION

The silicon on insulator (SOI) structure offers important advantages over the normal bulk devices, particularly for CMOS circuit, in terms of high packing density, reduced junction capacitance and latch-up prevention. Even though extensive studies have been made to recrystallize silicon on top of SiO_2, it is still impossible to obtain grain boundary and sub-boundary free material to fabricate narrow channel devices over a large chip area for VLSI applications. A common technique used to overcome this problem has been the use of seed window which provides direct contact to the single crystal substrate to improve the quality of the recrysatllized SOI material[1,2,3]. However, grain boundary free material is still limited to the immediate surrounding, i.e., tens of microns, of the seed window. Furthermore, the lack of substrate contact in completely dielectric isolation devices causes a "kink" in the I-V characteristics similar to the floating body effect in bulk devices[4] and can affect high speed device performance.

We have developed a seeded channel SOI device structure to overcome the above problems. In the seeded channel approach, the gate is placed directly above a seed window in the underlying oxide while the source and drain are left on the SOI region. This is illustrated in Fig. 1. Because the oxide opening provides a seed region during the recrystallization process, the silicon quality in the channel region should be free of any grain boundaries. Only a minimal lateral overgrowth from the seed window is needed to assure the integrity of device characteristics. Defects in the recrystallized silicon some distance away from the seed window will not

significantly affect the device performance. The floating body effect, or "kink" effect, should also be eliminated by using this structure since the channel region is in direct contact with the substrate. It is the purpose of this paper to demonstrate that the seeded channel approach can be used for SOI device fabrication without the need of any changes in device layout and good device charcateristics can be obtained by the usual scanning laser recrystallization process.

EXPERIMENTAL PROCEDURE

A standard production process was used to fabricate test devices. The gate oxide is 40nm and channel length of test devices ranges from 1um to 50um. The starting materials were <100> 50Ω-cm p-type silicon wafers. A 400nm thermal oxide was grown by local oxidation process to form seed windows. The seed window mask is simply the active channel region, therefore, the seed window mask can be created by the areas common to the diffusion mask and poly gate mask data base in the conventional self-aligned silicon gate process. No new layout is required for this step, it is illustrated in Fig. 2. LPCVD polysilicon and oxide capping layer were then deposited before laser recrystallization. After recrystallization the oxide capping layer was stripped then a standard mask set for n-MOS 256K EPROM chip were used to fabricate test transistors. Care was taken to align the transistors directly over the seed windows. Both enhancement and depletion transistors as well as devices without threshold implant were fabricated. Control devices were fabricated simultaneously using the same starting materials and mask set. In this way, direct and quantitative comparisions of device characteristics can be obtained. The fabrication process is summarized in Table 1.

LASER RECRYSTALLIZATION

A CW argon laser is used as a power source for recrystallization. The beam is controlled by a shutter and is shaped by lenses into a 150 x 20um ellipse when focused onto the wafer surface. The 4" device wafer is placed on a heated substrate holder (450°C) and scanned under the laser spot by a computer controlled X-Y stage. The scan speed is approximately 10cm/sec and the step distance between scan lines is 100um, therefore, a 50um overlap of the scanned spots. The laser power is adjusted to achieve optimum recrystallization over substantially the entire 4" wafer surface.

Because of variations in the underlying structure, it is more difficult to obtain uniform recrystallization of polysilicon in the seed window area and over the SOI region simultaneously as compared to the standard SOI structure. Since the reflectivity of bare silicon is very high (30 to 40%) the capping oxide layer thickness is chosen to be 1/4 wavelength, i.e., 90nm to minimize surface reflection in the seed region. The reflectivity in the SOI region is a function of buried oxide and poly thickness as well as the capping oxide thickness. The difference in reflectivity between the seed and SOI regions has a pronounced effect on the quality and uniformity of recrystallized material. The best recrystallization result is obtained by matching the reflectivity of the seeded area to the SOI area. To study the effect of reflectivity on laser recrystallization, structures of different buried oxide/poly thickness and capping layer combinations were fabricated. Various problems such as blasting of the capping layer over SOI region, seeded area not melting, surface ripples etc. were observed on different combinations of thin film stack. We have also carried out computer simmulations of this multilayer reflection problem. We have found that due

to the periodic dependance of the reflectivity on the underlying poly and oxide thickness we can adjust the reflectivity of the SOI region by optimizing the thickness of these films. The results of the computer simmulation studies are summarized in Fig. 3.

Other than the thickness control, we have found the mechanical properties of the capping layer also has a pronounced effect on the uniformity of recrystallized material. As deposited LPCVD oxide is mechanically too weak to prevent "blasting" of the capping layer in the overheated regions. Due to the large thermal diffusivity difference of oxide and silicon, there is a significant difference in the vertical thermal gradient between the seeded region and the SOI. This temperature difference sets up a lateral thermal gradient causing heat to flow laterally. This lateral heat flow causes a distinct peak and trough in temperature profile at boundaries of SOI and seed regions. "Blasting" will occur when the vapor pressure of molten silicon in the over heated region exceeds the mechanical strength of capping layer. In the blasted area the capping layer as well as the molten silicon are removed from the surface leaving only the underlying oxide. To overcome this problem, densification is needed after CVD deposition to improve mechanical integrity before laser anneal. Annealing at 920°C in N_2 gives a capping layer that is much more blasting resistant. However, the recrystallized material exhibited pronounced surface ripples. The ripples have an amplitude of 500 - 2500Å and a pitch of approximately 25um. These ripples represent the thickness variations of the recrystallized film and could be caused by the excessive stress in the densified CVD oxide film. A series of annealing experiments were carried out to optimize the densification temperature to prevent blasting and ripple formation. An annealing cycle of 2 hrs at 800°C was found to be satisfactory. The optimized substrate preparation conditions for laser recrystallization is summarized in Table 2. The resulting recrystallized material after Seeco dislocation etch is shown in Fig. 4 indicating defect free material around the seed window. Fig. 5 is a cross-sectional TEM micrograph showing relatively defect free material around the seed window.

DEVICE CHARACTERISTICS

The transistors fabricated with this seeded channel approach exhibited well behaved I-V characteristics. This is illustrated in Fig. 6. As expected, no "kink" effect was observed because the channel region is in contact with the substrate. The threshold voltages of the experimental enhancement (1.2V) and depletion transistors (-2.5V) is about 0.2 volt more positive than that of control devices. This is caused at least in part by the excessive p-type doping in the recrystallized region (2×10^{15}) than the original substrate (2×10^{14}). This excessive p-type doping is believed due to the presence of dopant material in the CVD deposited poly and capping layer. The carrier concentration of the recrystallized silicon was determined by spreading resistance measurements. The leakage current of these transistors are also well behaved as illustrated in Fig. 7. Fig. 7 gives a subthreshold slope of 120mV per decade of current. This is somewhat higher value than the standard control device which is approximately 105mV/decade.

Junction breakdown and junction leakage were also measured. These values are comparable to that of control devices, although a significantly larger number of SOI transistors exhibited large S/D junction leakage current than that of standard control transistors. The cause of poor junction leakage is unknown but likely due to the poor backside interface with the buried oxide. The surface mobilities as determined from long channel length (50um) enhancement devices were about 20% lower than that of

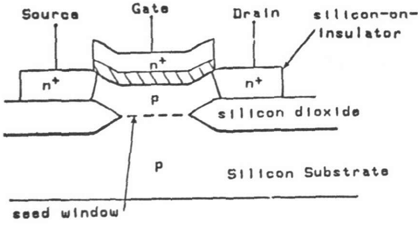


Fig. 1 Cross section of a seeded channel SOI transistor.

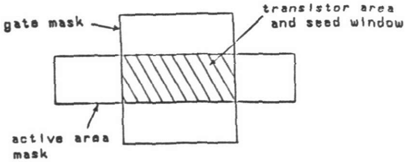


Fig. 2 Seed window mask is formed by the composit of stanard diffusion and poly gate structures.

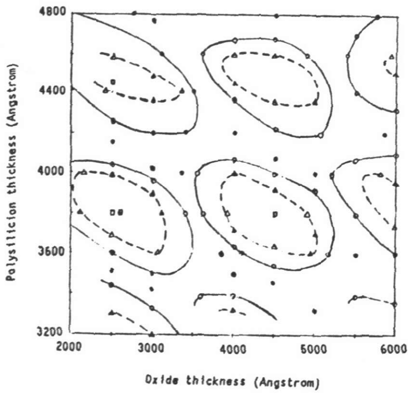


Fig. 3 Computer simulation of surface reflectivity of SOI structures with different polysilicon and oxide thickness. LTO thickness is 900 Angstrom. • <5% ; o (———) 10% ; ▲ (- - - -) 20% ; ▫ 30%

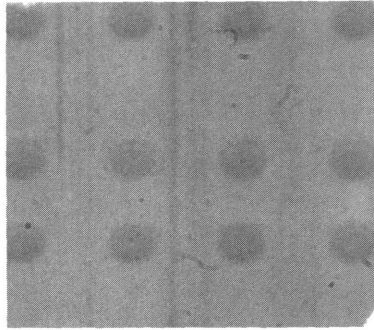


Fig. 4 Photomicrograph of laser recrystallized silicon after Secco dislocation etch.

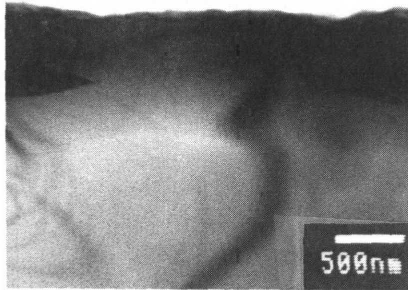


Fig. 5 Cross-sectional TEM micrography of laser recrystallized silicon showing defect free material around a seed window.

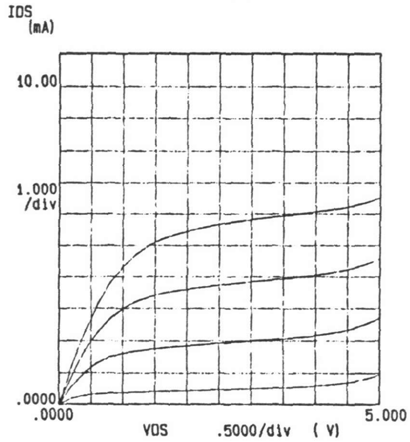
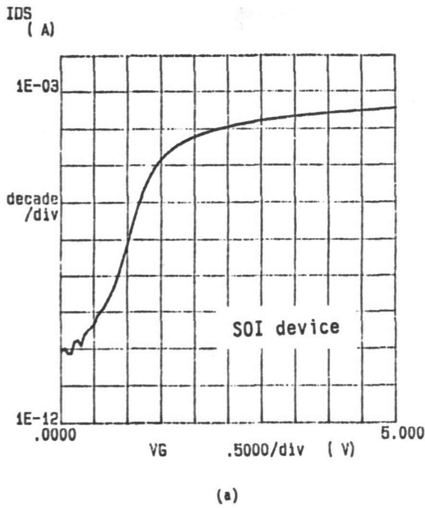


Fig. 6 I-V characteristics of an enhancement SOI transistor with W = 50um L = 2um (Le $\simeq$ 0.8um).



(a)

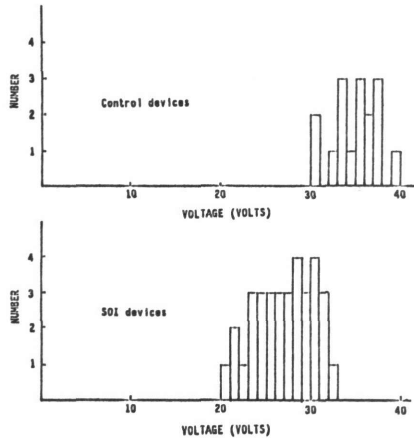
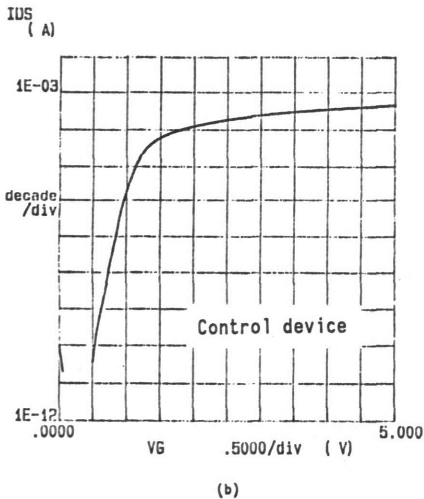


Fig. 8 Gate oxide breakdown voltage distribution of SOI devices and control devices.



(b)

Fig. 7 Subthreshold conduction characteristics of (a) SOI enhancement transistor and (b) control enhancement transistor. Both transistors have drawn W = 50um and drawn L = 3um.

Table I

PROCESS FLOW

38-63 OHM-CM <100> P TYPE SILICON
*SEED WINDOW PATTERN LOCOS OXIDE
*CVD POLYSILICON
*LPCVD CAPPING OXIDE
*ANNEALING
*LASER SCAN
*CAPPING OXIDE STRIPPING
LOCOS ISOLATION
DEPLETION IMPLANT ARSENIC
GROW 400A GATE OXIDE
ENHANCEMENT IMPLANT BORON
POLYSILICON GATE
SOURCE/DRAIN IMPLANT ARSENIC
PYROGLASS
CONTACT OPEN
METAL
PASSIVATION

NOTE: THOSE STEPS MARKED WITH * ARE USED FOR PREPARING SOI WAFERS

Table II

OPTIMIZED CONDITIONS FOR LASER RECRYSTALLIZATION

3500A LOCOS OXIDE
4200A CVD POLYSILICON
900A LPCVD OXIDE
TWO HOURS 800C ANNEAL IN NITROGEN GAS
150UM X 20UM BEAM SPOT SIZE
50UM OVERLAP
NO TILTING OF BEAM SPOT W.R.T. SCAN DIRECTION

control devices. This difference is too large to attribute to doping concentration differences in the channel regions. The fact that the channel region for the SOI devices is not perfectly flat and the recrystallized material has a grainy surface as compared to the original control wafer surface may also contribute to the degradation of the mobility. The gate oxide breakdown voltages of the SOI devices were compared with the control devices as shown in Fig. 8. The SOI devices have lower gate oxide breakdown voltages. The cause for this is also uncertain but could also be due in part the rougher surface condition of the recrystallized material.

SUMMARY

A seeded channel structure has been developed to fabricate SOI transistors that retain the advantages of SOI and bulk transistor characteristics. Good device characteristics were obtained using a standard mask set and process flow. Although laser recrystallization is more difficult to obtain due to the difference in thin film structures between the seeded and SOI regions. By carefully optimizing the property and thickness of these films good materials can be obtained. This structure should be easily adoptable to all existing MOS designs and technology since no new designs are required.

ACKNOWLEDGEMENT

The authors wish to thank for the wafer processing support from Intel's Fab 1 facility and the Intel Research Council for providing the funding to modify the laser recrystallization equipment at Stanford University.

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