THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

ELECTRON DEVICES SOCIETY

50th Annual Device Research Conference

June 22 - 24, 1992
Massachusetts Institute of Technology
Cambridge, MA

DIGEST

Conference Chair:	Sam Shichijo
Program Chair:	Tom Jackson
Publicity Chair:	Joe Campbell
Past Chair:	Larry Coldren
Local Arrangements Chair:	Leslie Kolodziejski
Treasurer:	Lu Kasprzak

Program Committee

Peter Asbeck
Dave Bloom
Paul Chow
Emmanuel Crabbé
Chris Harder
Hideki Hasegawa
John Hayes
Takashi Ito
Umesh Mishra
Dennis Rathman
Mark Reed
Chuck Rogers
Jim Rosenberg
Jim Sturm
Henryk Temkin
Kang Wang
I-Wei Wu

Sponsored by

The IEEE Electron Devices Society

A Novel Double Base Heterojunction Bipolar Transistor for Low Temperature Bipolar Logic

Erwin J. Prinz, Xiaodong Xiao, Peter V. Schwartz, and James C. Sturm
Dept. of Electrical Engineering, Princeton University, Princeton, N.J. 08544, (609)258-6624

Future low temperature applications of electronic devices demand low power consumption which could be achieved by increased functionality of each transistor. Here we report a novel Double-Base Heterojunction Bipolar Transistor (DB–HBT) in the Si/SiGe material system which can operate with high gain in a single-transistor NAND gate at 77K. The device structure is similar to that of a Si/SiGe/Si HBT, except for an intrinsic Si layer inserted into the p-SiGe base. The intrinsic Si layer is used to electrically isolate the two SiGe base layers of an n-Si/p-SiGe/i-Si/p-SiGe/n-Si DB–HBT, because the valence band discontinuity at the SiGe/Si heterojunction acts as a barrier for holes. A key point is that the Si layer introduces only a very small barrier in the conduction band because most of the bandgap difference between unstrained Si and strained SiGe occurs as a valence band offset, ΔE_V.

If a bias is applied between the two p-SiGe base layers, holes are injected by thermionic emission over the valence band discontinuity at the Si/SiGe heterojunction. The magnitude of this current precludes independent base operation of the device at room temperature. At 77 K, however, thermionic emission is sufficiently suppressed to provide isolation between the two base layers. The voltages applied between each of the base layers and the emitter shape the *conduction* band barrier seen by the electrons. Only if *both* bases are forward biased can electrons travel over the base potential barrier from emitter to collector. ("ON" state). If the voltage of either base contact is below the turn-on voltage of the n-Si/p-SiGe junction, no electron current flows ("OFF" state). Operated with a load resistor this device therefore performs the logic NAND function.

The device structure was grown using Rapid Thermal Chemical Vapor Deposition. After the n-Si collector growth at 1000°C, the temperature was kept below 700°C to minimize boron diffusion into the Si barrier while growing the 200Å-thin p-$Si_{0.70}Ge_{0.30}$ bases, the 200Å-thin intrinsic Si barrier, and the n-Si emitter. Four-terminal devices (emitter, base 1, base 2, and collector) were fabricated in a triple-mesa process. The two p-SiGe base layers were contacted by selective chemical etching [1, 2] and the collector by plasma-etching.

At room temperature the intrinsic Si-barrier has no isolating effect and the device works as a single base HBT with an ideality factor of 1.3 for the base current and 1.0 for the collector current and a common-emitter current gain of about 200. At 77 K the device has a maximum current gain of about 100 when operating with both base contacts externally shorted together. Unlike at room temperature, however, the thermionic emission across the p-SiGe/i-Si/p-SiGe barrier is suppressed and the two bases are independent with leakage currents below 5 μA for relative base voltages of less than 0.5 V in a device with a base mesa area of $184 \times 184\ \mu m^2$. Since the voltages applied at *both* base layers shape the *conduction* band, the collector current injected from the emitter can be controlled independently with either base contact. Only if the voltage on both bases exceeds about 0.8 V does the collector current turn on. It increases with a slope of less than 17 mV/decade which is close to the ideal value of 15.3 mV/decade at 77 K. Using a load resistor of 1 kΩ, switching is demonstrated in a NAND-gate using a single DB–HBT where the two inputs are the base terminals and the output is at the collector terminal.

In summary, a novel DB-HBT device has been demonstrated at 77 K, with high gain and nearly ideal switching behavior in a single-transistor NAND-gate. We acknowledge support of the Office of Naval Research and the National Science Foundation.

[1] P. Narozny *et al.*, IEEE Trans. on Electron Dev., Vol. 36, p. 2363, 1989.
[2] A.H. Krist *et al.*, Appl. Phys. Lett., Vol. 58, p. 1899, 1991.

Good idea — use mult gates to control Ec vs x => ie study velocity field charact through fT by varying VB1 vs VB2?

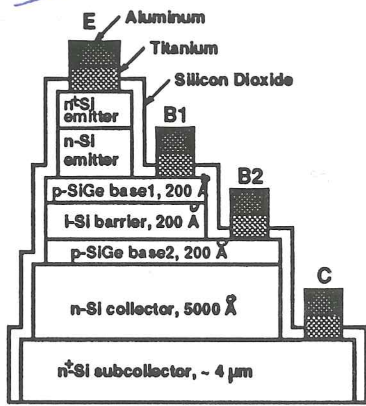

Fig. 1: Device structure of Double-Base Heterojunction Bipolar Transistor (DB–HBT).

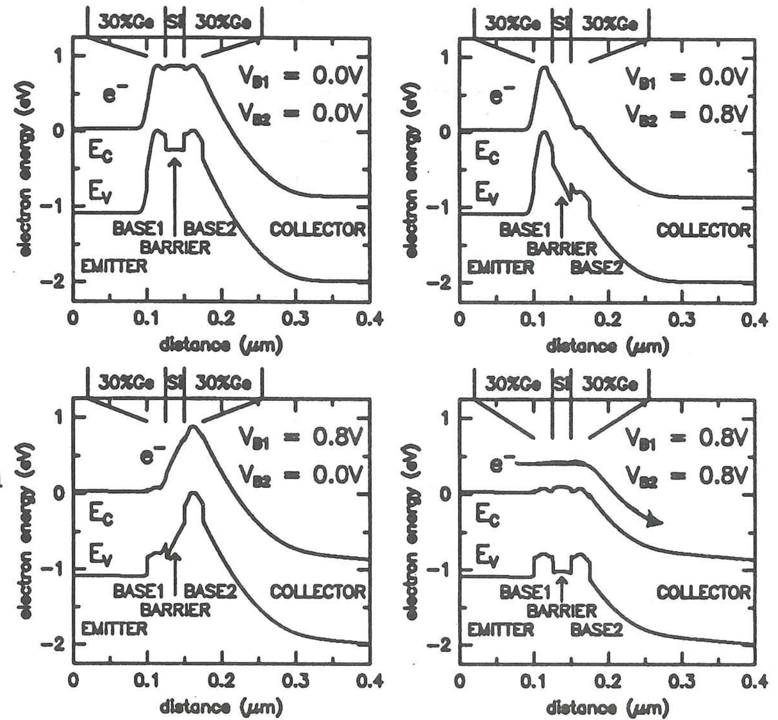

Fig. 2: Calculated band diagrams of DB–HBT for various base voltage inputs.

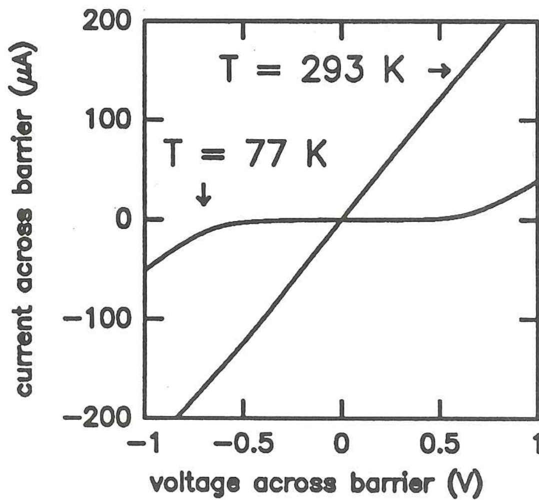

Fig. 3: Measured current-voltage characteristics of p-SiGe/i-Si/p-SiGe barrier at room temperature and at 77 K. Note the low leakage current for voltages below 0.5 V at 77 K where thermionic emission is effectively suppressed.

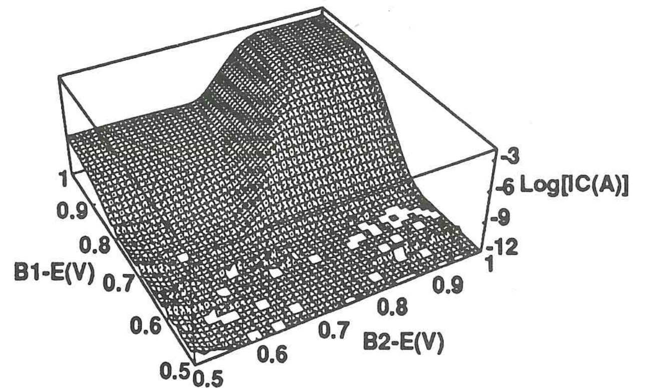

Fig. 4: Measured collector current plotted logarithmically vs. voltage applied at base 1 and base 2. Note the sharp turn-on when *both* inputs are above about 0.8 V.

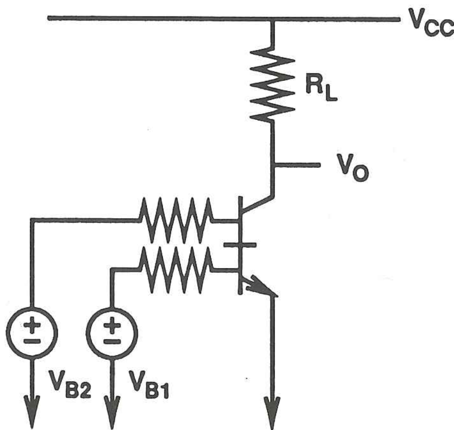

Fig. 5: Circuit diagram for single-transistor NAND-gate. If both inputs are high (see Fig. 2) the current across the load resistor R_L lowers the output voltage V_O.

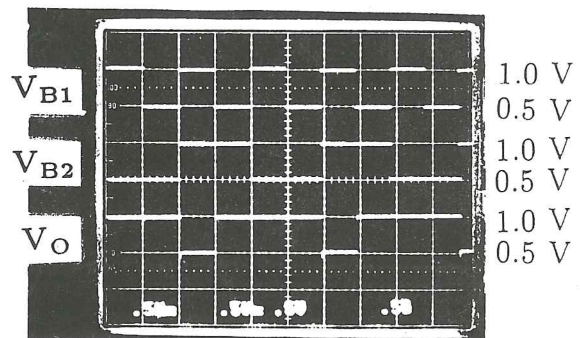

Fig. 6: Measured switching behavior of the circuit of Fig. 5. Both the input and output voltage levels are between 0.5 V (transistor ON) and 1.0 V (transistor OFF).

was on hand. It took an appreciation of the merits of the lattice-matched (Al,Ga)As system, and of a suitable LPE technology, to make the device work. The presentation of this breakthrough by Panish and Hayashi at the 1970 DRC was one of the great moments in the history of the Conference. With (Al,Ga)As LPE technology on hand, Woodall *et al.* in 1972 reported the first truly successful HBTs, another DRC highlight.

In the mid-1970's, MBE came on stream, shortly followed by OMVPE. These technologies had the ability to grow *very* abrupt heterointerfaces, which, in the hands of Dingle *et al.* and Esaki *et al.*, led to quantum wells and superlattices. Superlattices soon led to the concept of modulation doping, which, in turn, led to the 1980 development of the HEMT by Hiyamizu *et al.* The last of the major device families had "gone hetero," starting a decade of "Heterostructures for Everything"—including specifically silicon. The realization of HBT's in the (Si,Ge) alloy system by Bean and others must be rated as a development of significance comparable to that of the laser.

We are now over two years into the 1990's, and there is already a major new breakthrough: The first II–VI blue-green diode laser, to some *the* highlight of the 1991 DRC. It looks like the heterojunction device field is going to remain a lively one, and the DRC is going to remain the dominant conference for "going public" with new breakthroughs in this field.

IIA-1 53 GHz-f_{max} Si/SiGe Heterojunction Bipolar Transistors—A. Gruhle, H. Kibbel, and E. Kasper, Daimler-Benz AG, Research Center, Wilhelm-Runge-Strasse 11, D-7900 Ulm, Germany (+49)0731/505-2038.

The Si/SiGe/Si heterojunction bipolar transistor offers the possibility of a thin and at the same time highly doped base. The low base resistance is particularly important for increasing the f_{max} limit. Despite excellent reported transit frequencies of up to 75 GHz the base sheet resistance of several kilo-ohms per square has so far limited f_{max} to 40 GHz [1]. Base dopant out-diffusion during the necessary poly-emitter anneal cycles has been the obstacle for a further improvement.

We report Si/SiGe HBT's with a base sheet resistance of only 680 Ω/□ leading to a measured f_{max} of 53 GHz. This is the highest frequency for power amplification reported for any three-terminal silicon-based device. The complete layer structure was grown by MBE including the single-crystal emitter with no need for a poly-drive-in anneal. The low thermal budget prevents the diffusion of boron out of the 30-nm-thick (25% Ge) base with a peak of 6×10^{19} cm^{-3} concentration. The 300-nm-thick collector was Sb doped at 2×10^{17} cm^{-3}, emitter thickness was 150 nm at 6×10^{18} cm^{-3} with an n^+ cap layer.

Devices were built on high-resistivity substrates with As-implanted and diffused buried layers. A double-mesa structure using a self-aligned base metallization with respect to the emitters was employed. Air bridges and the p^--substrate reduced parasitic capacitances of the contact pads.

On-wafer high-frequency measurements from 0.5 to 26 GHz showed transit frequencies between 40 and 50 GHz for devices with 1–3 μm wide emitter fingers. The reduced base sheet resistance compared to earlier devices [2] led to a maximum available gain at 26 GHz for a 1 × 16 μm device of 6.3 dB corresponding to a record f_{max} = 53 GHz. Bias values were $V_{CB} = 4.5$ V and $I_C = 20$ mA. Devices with 3-μm emitter still had f_{max} the values above 40 GHz. This is because of the low base sheet resistance which permits relaxed design rules for high-frequency devices in contrast to the submicrometer emitters of state-of-the-art Si bipolar transistors.

[1] J. H. Comfort *et al.*, "Single-crystal emitter cap for epitaxial Si- and SiGe-base transistors," in *Proc. IEDM Tech. Dig.*, 1991, p. 857.
[2] A. Gruhle *et al.*, "MBE-grown Si/SiGe HBT's with high β, f_t, and f_{max}," *IEEE Electronic Device Lett.*, vol. 13, pp. 206–208, Apr. 1992.

IIA-2 A Novel Double-Base Heterojunction Bipolar Transistor for Low-Temperature Bipolar Logic—Erwin J. Prinz, Xiaodong Xiao, Peter V. Schwartz, and James C. Sturm, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 (609) 258-6624.

Future low-temperature applications of electronic devices demand low power consumption which could be achieved by increased functionality of each transistor. Here we report a novel Double-Base Heterojunction Bipolar Transistor (DB–HBT) in the Si/SiGe material system which can operate with high gain in a single-transistor NAND gate at 77 K. The device structure is similar to that of a Si/SiGe/Si HBT, except for an intrinsic Si layer inserted into the p-SiGe base. The intrinsic Si layer is used to electrically isolate the two SiGe base layers of an n-Si/p-SiGe/i-Si/p-SiGe/n-Si DB–HBT, because the valence-band discontinuity at the SiGe/Si heterojunction acts as a barrier for holes. A key point is that the Si layer introduces only a very small barrier in the conduction band because most of the bandgap difference between unstrained Si and strained SiGe occurs as a valence band offset ΔE_V.

If a bias is applied between the two p-SiGe base layers, holes are injected by thermionic emission over the valence-band discontinuity at the Si/SiGe heterojunction. The magnitude of this current precludes independent base operation of the device at room temperature. At 77 K, however, thermionic emission is sufficiently suppressed to provide isolation between the two base layers. The voltages applied between each of the base layers and the emitter shape the *conduction* band barrier seen by the electrons. Only if *both* bases are forward-biased can electrons travel over the base potential barrier from emitter to collector ("ON" state). If the voltage of either base con-

tact is below the turn-on voltage of the n-Si/p-SiGe junction, no electron current flows (''OFF'' state). Operated with a load resistor this device therefore performs the logic NAND function.

The device structure was grown using Rapid Thermal Chemical Vapor Deposition. After the n-Si collector growth at 1000°C, the temperature was kept below 700°C to minimize boron diffusion into the Si barrier while growing the 200-Å-thin p-$Si_{0.70}Ge_{0.30}$ bases, the 200-Å-thin intrinsic Si barrier, and the n-Si emitter. Four-terminal devices (emitter, base 1, base 2, and collector) were fabricated in a triple-mesa process. The two p-SiGe base layers were contacted by selective chemical etching [1], [2] and the collector by plasma etching.

At room temperature, the intrinsic Si barrier has no isolating effect and the device works as a single-base HBT with an ideality factor of 1.3 for the base current and 1.0 for the collector current and a common-emitter current gain of about 200. At 77 K the device has a maximum current gain of about 100 when operating with both base contacts externally shorted together. Unlike at room temperature, however, the thermionic emission across the p-SiGe/i-Si/p-SiGe barrier is suppressed and the two bases are independent with leakage currents below 5 μA for relative base voltages of less than 0.5 V in a device with a base mesa area of 184 × 184 μm^2. Since the voltages applied at *both* base layers shape the *conduction* band, the collector current injected from the emitter can be controlled independently with either base contact. Only if the voltage on both bases exceeds about 0.8 V does the collector current turn on. It increases with a slope of less than 17 mV/decade which is close to the ideal value of 15.3 mV/decade at 77 K. Using a load resistor of 1 kΩ, switching is demonstrated in a NAND gate using a single DB-HBT where the two inputs are the base terminals and the output is at the collector terminal.

In summary, a novel DB-HBT device has been demonstrated at 77 K, with high gain and nearly ideal switching behavior in a single-transistor NAND gate.

This work was supported by Office of Naval Research and the National Science Foundation.

[1] P. Narozny *et al.*, *IEEE Trans. Electron Devices*, vol. 36, p. 2363, 1989.
[2] A. H. Krist *et al.*, *Appl. Phys. Lett.*, vol. 58, p. 1899, 1991.

IIA-3 p^+ Polysilicon Emitters for Sub-0.5 μm High-Performance p-n-p

J. Warnock, J. Y. C. Sun, and S. Bhattacharya* IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 (914) 945-3000.

Introduction

Recent advances in high-performance p-n-p design have been motivated by the promise of low-power high-performance complementary bipolar and/or BiCMOS circuits. Self-aligned p-n-p devices have been demonstrated [1] with cutoff frequencies above 35 GHz; the present challenge is to scale the device dimension down into the sub-half-micrometer regime to further improve the power-delay tradeoff. The issues associated with p-n-p emitter scaling in this regime have not been investigated to date, and initial indications are that emitter size effects are likely to be more severe than in the n-p-n case, due to the lower solubility of B and its reduced diffusion speed in polysilicon [2] as compared to As. However, any sacrifice on E-B junction depth will degrade the p-n-p device performance.

Emitter–Base Profile Design

Arsenic is chosen as the base dopant in this work since it can be implanted at very short depth and it hardly diffuses under typical p^+ emitter drive-in conditions. Thus for a given collector profile, the base width is determined only by the As implantation energy (and associated straggle). The energy required for the implant will depend directly on the emitter process, being higher for deeper emitter diffusions. Optimization of the p-n-p polysilicon emitter process is therefore the most critical part of the p-n-p device design.

Experimental

Self-aligned double-polysilicon p-n-p transistors with emitter width down to 0.15 μm were fabricated in a simplified three-mask process. After forming a semi-rox isolation, the extrinsic base poly and dielectrics are deposited. The emitter opening and extrinsic base are patterned simultaneously with one mask. The emitter poly is deposited after base and sidewall formation. The use of *in situ*-doped polysilicon for the p-n-p emitter [3] was not tried in these experiments, since it may induce more complexity into an integrated complementary bipolar or BiCMOS process. After implanting and annealing, poly and metal are patterned together. Finally, the exposed extrinsic base dielectric is etched to allow contact directly to the extrinsic base poly. The device parameters were then studied as a function of the emitter poly thickness (100 versus 150 nm), annealing cycle (850°C 5-min + 990°C 5-s rapid thermal anneal (RTA), or RTA only), and interfacial oxide (either 1.7 or 2.3 × 10^{15} cm^{-3}, from SIMS measurements).

Device Characteristics

Device characteristics were first compared for two different poly emitter thicknesses and several emitter sizes (furnace + RTA anneals). For dimensions below 0.4 μm, a significant nonideality is seen in the base current of the 150-nm emitter poly devices, resulting in a beta which falls rapidly with decreasing emitter size. Also, the reverse E-B leakage jumps by two orders of magnitude in this regime. This is evidence of inadequate doping of the poly at the periphery of the device. Also evident is a sudden increase in emitter resistance as the emitter becomes ''plugged,'' i.e., when emitter width is less than twice the poly thickness. For the 100-nm poly device, charac-