4th International Meeting on Silicon Molecular Beam Epitaxy, at Materials Research Society Symposium B, Anaheim, CA, Apr. 29 - May 3, 1991

REDUCTION OF p^+-n^+ JUNCTION TUNNELING CURRENT FOR BASE CURRENT IMPROVEMENT IN Si/SiGe/Si HETEROJUNCTION BIPOLAR TRANSISTORS

Ž. MATUTINOVIĆ-KRSTELJ, E. J. PRINZ, P. V. SCHWARTZ AND J. C. STURM,
Princeton University, Department of Electrical Engineering, Princeton, NJ 08544

ABSTRACT

A reduction of parasitic tunneling current by three orders of magnitude in epitaxial p^+-n^+ junctions grown by Rapid Thermal Chemical Vapor Deposition (RTCVD) compared to previously published ion implantation results is reported. These results are very important for the reduction of base current in scaled homojunction and Si/SiGe/Si heterojunction bipolar transistors. High reduction in tunneling currents allows higher limits to transistor base and emitter dopings. Significant tunneling was observed when the doping levels at the lighter doped side of the junction were of the order of $1\times10^{19}cm^{-3}$ for both Si/Si and SiGe/Si devices. These results were confirmed by I-V measurements performed at different temperatures. Since the tunneling current is mediated by midgap states at the junction, these results demonstrate the high quality of the epitaxial interface.

INTRODUCTION

Heavily doped layers are desired for optimum performance of homojunction (BJT's) and heterojunction bipolar transistors (HBT's). Increased base doping is required to avoid punchthrough when scaling these devices and is also desired for low base resistances and high Early voltages. High emitter dopings are desired for increased emitter efficiencies and low series resistances. However, it has been shown that the forward current of heavily doped silicon junctions at low bias levels is dominated by a parasitic tunneling current [1-5]. This is not band-to-band tunneling, but rather the tunneling of both electrons and holes to midgap states at the p-n interface where they recombine. A schematic diagram of ideal and tunneling currents at a heavily doped p^+-n^+ junction is shown in Fig.1. An increase in the doping of the lighter doped side of the base-emitter junction reduces the width of the space charge region increasing the tunneling probability. After a certain doping level (>10^{18} cm^{-3} according to [1]) is exceeded, the tunneling barrier becomes very narrow and causes non-negligible tunneling to midgap states. Since the hole and electron currents to midgap states must be equal, the current is limited by the side of the junction with lighter doping where the tunneling barrier is wider. Therefore the tunneling current is expected to increase with the doping on the lighter doped side. This tunneling current becomes a significant component of the transistor base current, especially at low forward biases.

In this paper, a significant reduction of tunneling current is reported in epitaxial p^+-n^+ junctions grown by RTCVD compared to the previously reported ion implantation results [1]. The implications of these results for HBT performance are also shown. Since it is desirable for Si/SiGe/Si HBT's to contain high base dopings (e.g. 10^{19} cm^{-3} [6] or more) the tunneling base current component becomes especially important. This is illustrated in Fig.2 where it is shown how the tunneling current is predicted to limit the current gain in a Si/$Si_{0.85}Ge_{0.15}$/Si HBT with a base doping of $N_B=5\times10^{19}cm^{-3}$ as the emitter doping is increased. In the absence of tunneling, the gain would follow the ideal curve shown in the figure. (At higher emitter doping levels, the ideal curve bends due to the silicon bandgap narrowing.) With tunneling, the gain curves are predicted to drop rapidly after a certain doping level is reached since tunneling causes a significant increase in the base current.

EXPERIMENTAL RESULTS AND DISCUSSION

Epitaxial p^+-n^+ (i.e. like a base-emitter) Si/Si and $Si_{0.85}Ge_{0.15}$/Si diodes were fabricated by RTCVD. Thick silicon (phosphorous doped) n^+ layers (3-13 μm) were grown on n-type substrates. The growth temperature varied from 850°C to 1000°C for different samples. The dopings ranged from $1\times10^{17}cm^{-3}$ to $1\times10^{19}cm^{-3}$. After the relatively high temperature step, the growth was stopped for 30 seconds and the temperature was lowered. P-type (boron doped) layers were then grown at low temperature to prevent outdiffusion and provide an abrupt junction. On some of the samples, a thin p^+ (30nm) $Si_{0.85}Ge_{0.15}$ strained epitaxial layer was grown at 625°C (doped $5\times10^{19}cm^{-3}$). This provided a n^+-Si/p^+-SiGe junction. Thin epitaxial p^+ silicon layers (50nm), doped $5\times10^{19}cm^{-3}$, were then grown at 700°C on all of the samples. The dopings were confirmed by spreading resistance and C-V measurements. The junctions were isolated by a simple mesa process.

Room temperature forward bias I-V curves are shown in Fig.3. The tunneling effect is clearly evident in the heavily doped devices at low

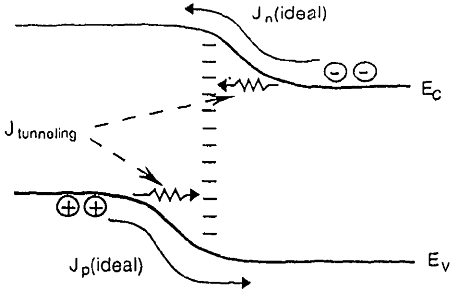


Fig.1. Schematic band diagram of ideal and tunneling currents at heavily doped p^+-n^+ junction

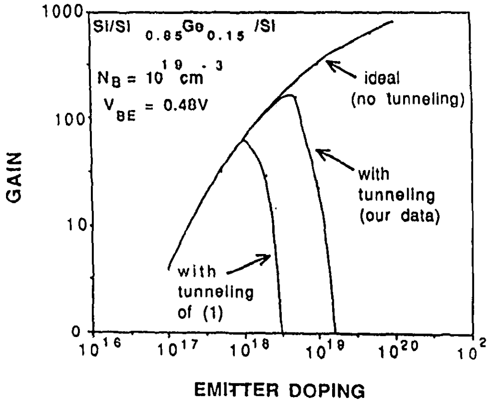


Fig.2. Calculated effects of the tunneling current on the gain of $Si/Si_{0.85}Ge_{0.15}/Si$ HBT's as the emitter doping is increased. Both curves based on the data of [1] and our data are given for comparison, as well as the ideal curve (no tunneling).

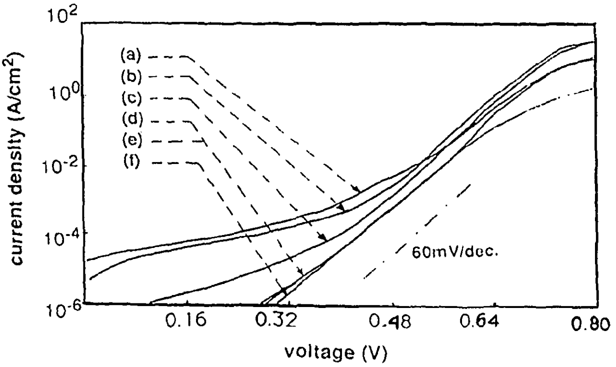


Fig.3 Room temperature forward bias I-V curves of several devices with the following n-type dopings:(a)$1x10^{19}cm^{-3}$(Si/SiGe), (b)$9x10^{18}cm^{-3}$(Si/Si), (c)$7x10^{18}cm^{-3}$(Si/Si), (d) $3x10^{18}cm^{-3}$ (Si/Si), (e) $1.5x10^{18}cm^{-3}$ (Si/Si and Si/SiGe),(f)$1.3x10^{17}cm^{-3}$ (Si/Si).

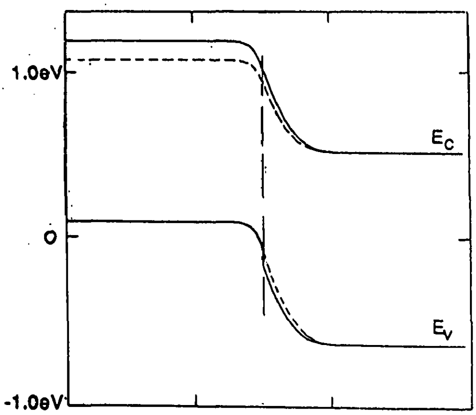
bias levels as the large "n>2" current. The current increases with the doping on the lighter doped side, as expected. This is not the typical space charge recombination current ($1<n<2$), which would increase at low doping levels with larger space-charge regions. I-V curves among the devices with the same area and doping were similar, and measurements on several different area devices ($1.4\times10^{-2}cm^{2}$--$9.5\times10^{-5}cm^{2}$) confirmed that the peripheral current components were negligible. Significant tunneling was observed at doping levels of the order of $1\times10^{19}cm^{-3}$ for both Si/Si and SiGe/Si devices.

Further evidence that these large currents at low biases are indeed tunneling is provided by temperature-dependent I-V measurements (175K - 350K). Since the injected currents are vastly reduced at lower temperatures and the tunneling currents are fairly insensitive to temperature, the effect of tunneling is even more significant at low temperatures. The observed concave shape of the current vs. temperature curve of heavily doped devices is consistent with the expected shape of excess tunneling current curves [4,5].

Calculations of band diagrams showed a slightly lower tunneling barrier (of the order of 100meV) for electrons in the $Si_{0.85}Ge_{0.15}/Si$ devices compared to the Si/Si devices for the same n-doping densities (Fig.4). This predicts slightly higher currents (~3 times) of SiGe/Si junctions. However, due to the resolution of the measurement, no significant difference in the behavior of Si/Si and SiGe/Si devices at the same doping levels was observed.

In Fig.5a, the current density at the forward bias of 0.32V is plotted as a function of doping. Also plotted are calculated values of the ideal diode current, which is dominated by electron injection into the p^{+}-Si layer. The ideal current should be the same in all devices since the total electron barrier is the same for both Si/Si and SiGe/Si devices. Previous results for tunneling limits in ion implanted p^{+}-n^{+} junctions [1] are also shown for comparison to the tunneling current lines fitting our data. At low doping levels, or high biases, ideal current dominates over tunneling. At lower bias levels tunneling causes an increase of several orders of magnitude in the current of heavily doped devices. A similar plot at V=0.48V is shown in Fig.5b. Also plotted are some typical base current densities extracted from Gummel plots of several published HBT and BJT results [7-12]. These reported base currents, of course, consist of several components besides tunneling, but tunneling is a fundamental lower limit to this number. It is interesting to note that except for devices also fabricated by another CVD epitaxial base technology (UHVCVD) [9], all base currents lie substantially above our results and even above the ion implantation results [1].

Fig.4 Band diagram of a forwardly biased junction (V=0.48V):
a) p^+-$Si_{0.85}Ge_{0.15}/n^+$-Si (solid)
b) p^+-Si/n^+-Si (dashed)
$N_A = 5\times10^{19}cm^{-3}$
$N_D = 10^{19}cm^{-3}$



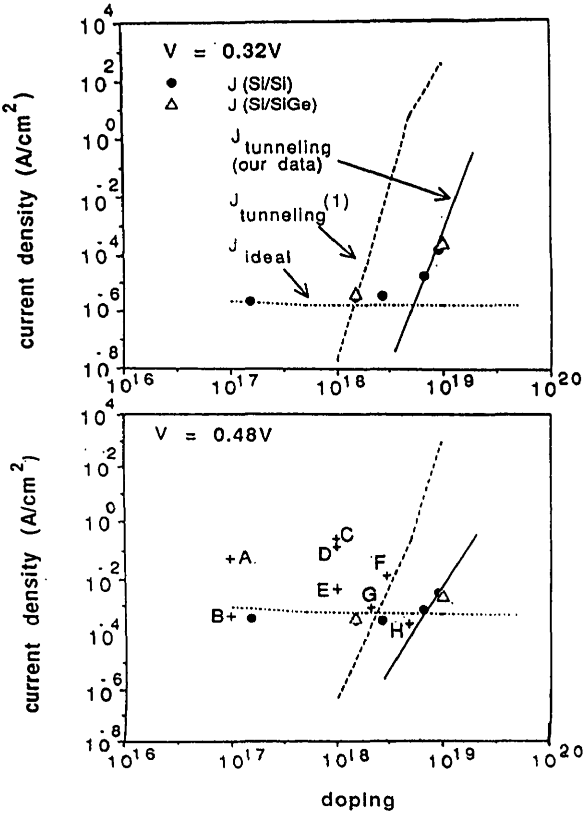


Fig.5 Current density vs. n-type doping for:
(a) V=0.32V;
(b) V=0.48V.
Also shown are the following data points:
A) SiGe HBT grown by LRP [11]
B) SiGe HBT grown by RTCVD (in our lab)
C) SiGe HBT grown by MBE [8]
D) SiGe HBT grown by MBE [7]
E) Si BJT grown by MBE [7]
F) SiGe HBT grown by UHV/CVD [10]
G) Si BJT [12]
H) SiGe HBT grown by UHV/CVD [9]

SUMMARY

For identical n-type doping levels, the tunneling currents in our devices are approximately three orders of magnitude lower than those of the ion implanted devices previously reported [1]. The reduction in parasitic tunneling current that we observed predicts that higher emitter dopings can be used, as well as predicts an increase in the peak transistor gain (Fig.2). The low tunneling current allows high gain to be maintained to higher base doping levels, enabling reduced base resistances and increased Early voltages. Since the tunneling current is mediated by midgap states at the junction, the vast reduction in tunneling currents of the devices fabricated by RTCVD implies a commensurate reduction of density of defects at the interface.

ACKNOWLEDGMENTS

This work was funded by ONR (N00014-90-J-1316) and NSF (ECS-86157227). The assistance of S.A. Schwarz of Bellcore for SIMS is greatly appreciated.

REFERENCES

1. J.A. Del Alamo and R.M. Swanson, IEEE El. Dev. Lett., 7, 629, (1986).
2. J. M. C. Stork and R. D. Isaak, IEEE Trans. El. Dev., 30, 1527 (1983).
3. E.Hackbarth and D.Duan-Lee Tang, IEEE Trans.El.Dev, 35, 2108 (1988).
4. G.P.Li, E. Hackbarth and T.-C. Chen, IEEE Trans. El. Dev. 35, 89 (1988).
5. A.G.Chynoweth, W.L.Feldmann, R.A.Logan, Phys.Rev., 121, 684 (1961).
6. C.A. King, J.L. Hoyt, J.F. Gibbons, IEEE Trans. El. Dev. 36, 2093 (1989).
7. G. L. Patton, S. S. Iyer, S. L. Delage, S. Tiwari and J. M. C. Stork, IEEE El. Dev. Lett., 9, 165, (1988).
8. P. Narozny, H. Dämbkes, H. Kibbel and E. Kasper, IEEE Trans. El. Dev. 36, 2363, (1989).
9. G.L.Patton, J.H.Comfort, B.S.Meyerson, E.F.Crabbé, G.J.Scilla, E.D. de Frésart, J.M.C.Stork, J.Y.-C. Sun, D.L.Harame and J.N. Burghartz, IEEE El. Dev. Lett., 11, 171, (1990).
10. D.L.Harame, J.M.C.Stork, B.S.Meyerson, E.F.Crabbé, G.J.Scilla, E de Frésart, A.E.Megdanis, C.L.Stanis, G.L.Patton, J.H.Comfort, A.A.Bright, J.B.Johnson and S.S.Furkay, IEDM Tech. Dig., 2.7.1, (1990).
11. T.I.Kamins, K.Nauka, J.B. Krueger, J.L.Hoyt, C.A.King, D.B.Noble, C.M.Gronet and J.F.Gibbons, IEEE El.Dev.Lett., 10, 503, (1989).
12. J.Warnock, J.D.Cressler, K.A.Jenkins, T.-C. Chen, J.Y.-C.Sun and D.D.Tang, IEEE El.Dev.Lett, 11, 475, (1990)