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Artificial Intelligence Meets Large-Scale Sensing:

using Large-Area Electronics (LAE) to enable intelligent spaces

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***Abstract*—The tremendous value artificial intelligence (AI) is showing across a broad range of applications is driving it from cyber-systems to systems pervading every aspect of our lives. But real-world data challenges the efficiency and robustness with which AI systems of today can perform, due to the highly dynamic and noisy scenarios they face. While algorithmic solutions are required, this paper also explores technological solutions based on large-scale sensing. Specifically, Large-Area Electronics (LAE) is a technology that can make large-scale, form-fitting sensors possible for broad deployment in our lives. System-design principles, architectural approaches, supporting circuits, and underlying technological concerns surrounding LAE and its use in emerging systems for intelligent sensing are explored.**

Keywords—Artificial intelligence; flexible electronics; Internet of Things; large-area electronics; machine learning.

I. Introduction

The field of artificial intelligence (AI), fueled by algorithms from machine learning, has made astounding progress in just the last few years. With machines demonstrating capabilities at or surpassing the level of humans in specific cognitive tasks (e.g., [1]), technology is redefining its relationship with people and society. This potential is motivating AI to extend beyond cyber-systems, to systems pervading all aspects of our work and social environments. But, early demonstrations of such systems show that the intricate, dynamic, noisy, and statistically non-stationary environments of the real world raise immense challenges [2,3]. To address these, the AI community is focused on algorithms that learn and adapt efficiently, i.e., within the number of experiences (training examples) needed by humans, and models that are robust, i.e., to the incompleteness, noise, and logical perturbations exhibited by real-world processes and data.

This paper examines how *new sensing technologies* can critically enable such algorithmic directions, especially for human-interactive systems. We focus on sensing technologies that can be associated with (a large number of) physical objects, which humans naturally interact with. The insight driving this is that the ways humans interact with objects in their environments say something about the activities they are engaged in and the underlying intentions they have.

Associating functionality with physical objects on a large scale has clear connections with the Internet of Things (IoT), which is a confluence of technologies the electronics community has been pursuing broadly. This paper takes a more specific perspective on IoT, focusing on a particular technology to enable large-scale, form-fitting sensing, namely Large-Area Electronics (LAE), and the algorithmic transformations it enables for the particular function of efficient and robust estimation of the state of an environment, including its human actors.

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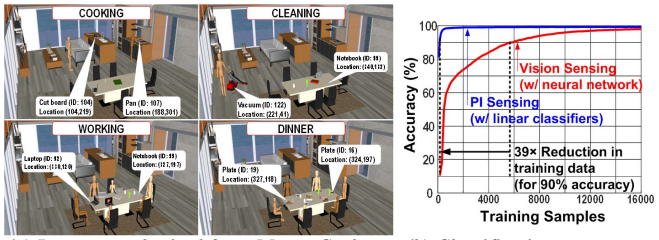
II. Physically-Integrated (PI) Sensing

Before delving into LAE, this section examines the impact on AI algorithms of associating sensor data with physical objects. We note a distinction between *physically-integrated* (PI) sensing, where embedded signals are directly coupled with sensors, and *remote* sensing, where embedded signals are not directly coupled with sensors. Remote sensing, such as vision, raises the challenge that as objects in a field of view change, what embedded signal is being sensed must first be detected Deep learning [4] has shown great success with this, where first low-level detection in space is performed by striding convolutional kernels (correlation filters), and then detection of progressively higher-level semantics is performed through composition via layers. Given the large space of possible embedded signals, and their compositions, deep-learning models require correspondingly many degrees of freedom, and proportionately large amounts of training data. This ultimately inhibits the ability to learn and adapt quickly in dynamic and/or interactive scenarios.

On the other hand, PI sensing potentially avoids the need for such ground-up learning and detection, because the embedded signal being sensed is *invariant*. This enforces structure in the sensed data. But, importantly, the structure also has *semantic relevance*: i.e., sensor data is tied to specific physical objects, and the ways physical objects are used is tied to human activities and intentions. The hope is that such semantically-relevant structure enhances *generalization of learning*, leading to models that can be trained more rapidly (in terms of examples needed) and perform more robustly (to practical perturbations and noise in the physical processes and sensed data).

While understanding and exploiting this structure is the subject of on-going research, jointly on algorithms and sensing technologies, we present some illustrative results. Fig. 1a shows example images from a smart-home environment. These are synthesized via 3D modeling and rendering, performing Monte Carlo sampling of human and object positions from predefined



(a) Images synthesized from Monte Carlo sampling. *(b) Classification accuracy versus training samples.*

Figure 1. Comparison of vision and PI sensing in smart home.

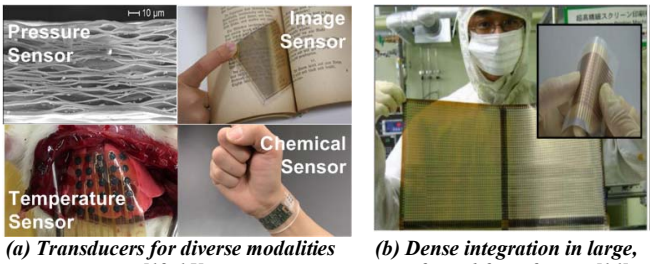
distributions for 10 different human-activity classes: breakfast, dinner, work, clean, cook, exercise, play toys (kids), play games (adults), recreation, no activity. This enables assessment of both vision sensing and PI sensing (e.g., emulating IoT), since occurring objects and positions are known by construction. Fig. 1b shows the classification accuracy versus number of training examples, using an ensemble of simple linear classifiers applied to PI sensing (with 126 object sensors), and an AlexNet-style [5] deep neural network applied to vision sensing (with 400×400 pixels). As seen, PI sensing enables rapid convergence and high final accuracy.

As mentioned, algorithmic research is progressing in a number of directions from here. For example, it is unlikely a sensor will be attached to every object. This raises questions around the completeness, accuracy, reliability, and modality requirements of PI sensing, and how these are impacted when *combined* with vision and other forms of remote sensing. Further, such requirements must be assessed for the range of inference problems encountered in interactive systems, including state estimation (as above) and state-action estimation (as in optimal control).

But, in addition to algorithmic questions, PI sensing raises critical technological challenges. First, *sensors must now be deployed on a large scale*, i.e., potentially on all objects humans interact with and over the physical dimensions those interactions span. However, such deployment must not be obtrusive to the natural interactions with the objects and the information signals such interactions generate. Second, continuous inference must now be performed over a large number and physical distribution of sensors, *necessitating low-energy localized computation*. While much work has recently been done to address such computation (e.g., [6-8]), we focus below on a potential platform technology for the required large-scale, distributed sensing, namely Large-Area Electronics (LAE).

III. Large-Area Electronics (LAE)

LAE is based on low-temperature processing (<200°C) of thin films. This enables materials deposition methods on substrates that can be large (square meters), thin (<5μm), and highly conformal. Today, the dominant applications for LAE technology are photovoltaics, flat-panel displays, and X-ray imagers. Flat-panel displays, in particular, are moving towards the integration of LED pixels on sheets as large as 10m^2, which are also flexible [9]. However, the LAE research community has recognized that low-temperature processing can enable broad sensing applications, going well beyond these initial applications. Low temperature affords compatibility with diverse materials, which can lead to a wide range of transducers for sensing, actuation, and other forms of energy harvesting. Combined with the large and conformal form factors possible, LAE thus holds distinct potential as a platform technology for interfacing electronics with the physical world [10,11]. To provide some examples, Fig. 2a shows various types of sensors and transducers that have been demonstrated, based on the integration of a range of materials [12-15]. Further, Fig. 2b shows the sort of form factor achievable, in this case integrating pressure sensors, based on PDMS with graphite nanoparticles to form a piezo-resistive rubber, with 2.54mm pitch in a flexible sheet on the order of a square meter [16].



(a) Transducers for diverse modalities [12-15]

(b) Dense integration in large, conformal form factors [16]

Figure 2. Recent demonstrations of LAE sensing capabilities.

However, sensing devices alone are not enough for enabling the broad embedded sensing applications that have begun to be envisioned. Such applications raise the need for a range of specific functionalities surrounding sensing. For instance, this includes sensor instrumentation/acquisition, computation, power management, and communication. The subsections below examine the realization of such functionality, on the technological, circuits, and systems levels.

A. LAE Technology

Electronic devices can be achieved over large areas in two ways: (1) direct deposition/processing of underlying materials on the eventual substrate; or (2) transferring fabricated devices from materials deposited/processed on a separate substrate. The second approach has most prominently been based on isolating micron-thick crystalline silicon layers, for instance by chemical etching of underlying ion-implanted SiO_2 layers [17]. While this can result in high performance devices, and has been exploited in emerging flexible systems for embedded sensing [18], the large number of transfer steps required limits scalability, particularly over large area. On the other hand, direct deposition/processing over large area and on flexible substrates imposes thermal limits, which in turn restricts the materials and methods, due to the processing equipment required, temperature limits on substrates such as plastics, stresses due to differential thermal expansion of materials, etc. Given the large investments involved in technology manufacturing, displays, in particular, have thus been an essential driver for such LAE technologies.

Displays, in fact, involve integration of multiple different LAE technologies, typically laminated together to achieve the range of required functionality (light emission, pixel control, touch sensing, etc.). This can also provide a model for integrating the range of functionality needed in broader sensing systems. A particularly critical functionality in displays is pixel control/accessing, via a thin-film-transistor (TFT) active matrix. Semiconductor properties, such as mobility, tend to be impaired by low-temperature processing, making TFTs an important area of focus.

The dominant semiconductor technology used for TFTs has been hydrogenated amorphous silicon (a-Si:H), and processing methods thus far have been derived from those of conventional CMOS ICs. Research activities have recently moved in two directions. First, efforts to reduce cost (indeed relevant for broader sensing applications) from the roughly \$100/m^2 required for today's displays has motivated additive, rather than subtractive processing methods. This has led to

research on organic TFTs [19,20]. Second, efforts have focused on increasing TFT performance through use of higher mobility semiconductors processed at low temperature. Most notably, this has motivated a transition to metal-oxide semiconductors [21,22], with n-channel TFTs achieving electron mobilities μ_e in the range of 10cm^2/Vs, compared to 1cm^2/Vs for a-Si:H. We point out that all TFT technologies discussed thus far present only unipolar capability; in fact, only polysilicon offers a complementary TFT technology, with mobilities in the range of 100cm^2/Vs, but requires significantly more complex processing, only adopted for very high-resolution displays. Table II summarizes the characteristics of a-Si:H [23] and zinc-oxide (ZnO) [24] TFTs fabricated in our lab for circuits and systems research. For reference, comparison with silicon-CMOS transistors is provided, showing large performance disparity, even with state-of-the-art TFT technologies.

Table I. Comparison of LAE TFTs and silicon MOSFET transistors.

	a-Si TFT	ZnO TFT	Si CMOS (130nm)
Mobility (μ_e/μ_h)	μ_e: 2 cm^2/Vs μ_h: 0.05 cm^2/Vs	μ_e: 12 cm^2/Vs μ_h: <1 cm^2/Vs	μ_e: 1000 cm^2/Vs μ_h: 500 cm^2/Vs
$t_{dielectric}$	280nm	40nm	2.2nm
V_{DD}	20V	6V	1.2 V
C_{GD}/$_{GS}$	3.3 fF/µm	9.9 fF/µm	0.34 fF/µm
f_T	1MHz	15MHz	150 GHz

B. *LAE Circuits*

The potential of LAE for broad embedded-sensing applications has recently fostered research in TFT circuits, directed at the diverse functionality required in such application. But, displays have once again served as an essential driver of TFT circuit design. Initially, this included circuits for pixel-control as well as circuits for row/column drivers and scanners [25,26]. More recently, the integration of increased sensing functionality within displays has driven research in areas such as in-pixel touch sensing [27] and finger-print sensing [28].

As mentioned, looking forward to the broader embedded-sensing applications potentially enabled by LAE has stimulated research taking TFT circuits beyond display-integrated functions, to components for diverse sensing-oriented functions. These have included instrumentation amplifiers [29-32], ADCs [33-37], power converters [38,39], wired communication transceivers [40,41], wireless communication transceivers [42], and even digital processing [43,44], some of which are shown in Fig. 3. Importantly, the limitations raised by TFT technologies and the sensing applications of interest have motivated specialized ways of thinking about circuit-level implementations. For instance, the ADC in [37] employs a simple time/frequency-based conversion architecture, potentially suitable for RFID readout. Other work has explored alternate logic styles to enable digital circuits in the absence of complementary TFT technology [45]. Related work has gone further to introduce readily-integrated device-level modifications in the TFTs, to enhance the performance of such logic styles [46]. Thus, we are seeing that a technological based initially driven by displays and X-ray imagers is beginning to support a broader class of embedded-sensing applications, and that these applications themselves are now beginning to drive device-level design. How this evolves into ecosystems for impacting new commercial markets remains to be seen, but it is showing some initial movement towards new products. As an example, standards-compliant RFID tags, based on such logic circuits and TFT designs, have recently begun to emerge [44].

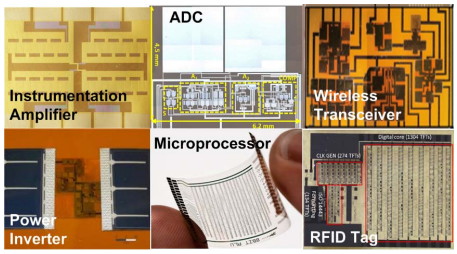


Figure 3. Recent demonstrations of TFT circuits [28,37,38,42-44].

C. *LAE Systems*

While recent research on TFT circuits shows a transformation in way of thinking about LAE technology more broadly than its traditional applications, such circuits remain limited in the functionality they can provide. In particular, the characteristic of low-temperature processing, which enables diverse and expansive arrays of sensors in LAE, also degrades the properties of semiconductor materials, making the performance and energy efficiency of TFTs orders-of-magnitude lower than that of transistors available in silicon-CMOS technologies. For instance, Table I shows that TFT f_T's and f_{MAX}'s may be 3-5 orders of magnitude lower. Thus, it is unlikely that TFTs will enable the range of functionality required in embedded-sensing applications on a scale proportionate with the level of sensing made possible in LAE. To extensively exploit the sensing capabilities of LAE at the system level, research is now turning to *hybrid systems*, which combine LAE, for sensing, with silicon CMOS, for other functionality required in systems [47].

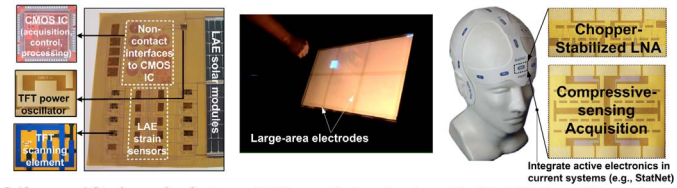
As discussed in the next section, hybrid systems can enable structured ways of thinking about LAE on the system level, and help to focus on specific challenges. For instance, such structure helps to identify and characterize foundational circuit and technological needs, providing specific directions for research in LAE systems. Beyond this, but of equal importance to the ultimate adoption of LAE systems, such structure also enables activities and investments to proceed around the manufacturing capability needed [48], even while architectures for differentiated applications are being researched.

IV. Hybrid Systems for PI Sensing

On a high level, hybrid systems, by bringing together two technologies with very different characteristics, enable complementary aspects to be addressed within the range of system functions required. This is illustrated in Table II, where, for instance, we see the following: (1) for power management, LAE enables physically-large energy harvesters, capable of providing significant power, while silicon CMOS enables efficient circuity for power conversion and regulation; (2) for communication, LAE enables long interconnects in wired communication and large antennas in wireless communication, while silicon CMOS enables efficient transceivers; and (3) for sensing, LAE enables diverse and expansive arrays of sensors, while silicon CMOS enables large scale computation over the sensor data. Along these lines, several hybrid-systems have been demonstrated, some of which are illustrated in Fig. 4:

Table II. Complementary strengths of LAE and silicon CMOS.

	Large-Area Electronics (LAE)	Silicon CMOS
Power management	• (Large) energy harvesting	• Power conversion, regulation
Communication	• Long, low-loss interconnects • Large antennas (efficient radiation)	• Wired transceivers for on sheet • Wireless transceivers for off sheet
Sensing/Computation	• Many diverse, distributed sensors	• >1B high-performance logic gates



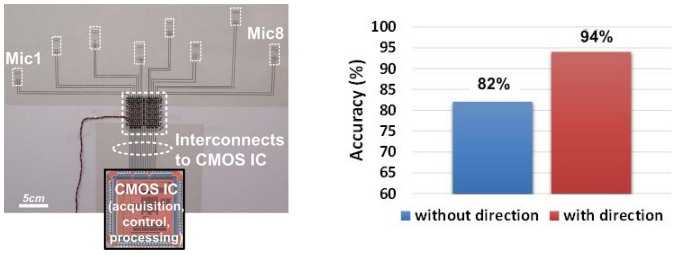
Self-powered Strain-sensing System for Structural Monitoring | 3D Human Gesture Sensing based on Capacitance | Flexible EEG Acquisition and Feature Extraction Array

Figure 4. Examples of hybrid systems [49,50,29].

- **Strain-sensing sheet for structural monitoring [49].** Strain correlates strongly with stress, which determines when structural failure occurs in materials. However, stain sensing requires high spatial resolution, necessitating large scale sensing in the case of civil infrastructure, such as bridges and buildings. This system employs LAE, for photovoltaic energy harvesters, piezo-resistive strain gauges, control/accessing circuitry, and long-range interconnects, along with silicon CMOS, for instrumentation, power conversion/regulation, and data communication.
- **Capacitive proximity and gesture sensing [50,51].** Typical capacitive touch sensing suffers from limited range due to electric field fringing from sensing electrodes to surrounding features. This system employs LAE, for long row/column [50] or pixel [51] electrodes, local pixel-modulated oscillators [51], and an actively-driven electric-field shield, along with silicon CMOS, for frequency de-modulation and data conversion.
- **Large-aperture phased-array acoustic sensing [52].** Exploiting the finite speed of sound, spatially-distributed acoustic sensors can form a phased array, enabling simultaneous sensing of multiple audio sources at different locations within an environment. This system employs LAE, for distributed thin-film piezoelectric microphone patches, local amplification, and control/accessing circuitry, along with silicon CMOS, for instrumentation, data conversion, and signal processing.
- **Conformal EEG sensing and processing [29].** Electroencephalogram (EEG) sensing requires typically 20, and possibly over 100, electrode channels distributed around the scalp. The recent emergence of flexible electrode arrays addresses patient comfort as well as challenges with electrode preparation and positioning, but requires a potentially large number of cables to external acquisition circuity. This system employs LAE, for electrode-localized low-noise amplifiers, compressive-sensing sampling, and channel-scanning circuits, along with silicon CMOS, for signal reconstruction, feature computation, and seizure classification.
- **Two-dimensional large-area force sensing [53].** Force/pressure sensing has applications ranging from patient bedsore avoidance to object-position detection. This system employs LAE, for piezo-resistive force sensors and amplitude-modulated frequency-hopping oscillator circuits, along with silicon CMOS, for instrumentation, signal demodulation, and two-dimensional signal reconstruction.

With such system demonstrations, research has been able to progress in two directions. First, on the applications level, in addition to controlled simulation over large datasets (as in Fig. 1), research demonstrations like this have enabled experimental exploration of PI sensing. For instance, Fig. 5a shows a hybrid system for activity detection based on large-aperture phased-array acoustic sensing [52] deployed in a laboratory. Fig. 5b shows the performance of sound classification, based on a dataset of 10 environmental sounds [54], replayed through speakers positioned in a room, to represent the locations of various sources (clock tick, rain fall through open window, etc.). As seen, the performance achieved by adding a directionality feature (available from a microphone phased array) to conventional audio features [mel-frequency cepstral coefficients (MFCC)] substantially enhances performance, by exploiting the discriminative value of source locations.

Second, on the circuits and architectures level, such systems have illuminated the key bottlenecks limiting hybrid systems, as well as possible approaches for addressing these. In particular, we find that while hybrid systems can indeed exploit the complementary strengths of the two technologies, *it is the interfacing required between LAE and CMOS technologies that limits the scale and efficiency ultimately achievable by hybrid systems.* This leads to a focus on specialized architectures and circuits oriented around the specific challenges posed by interfacing, as discussed in the subsections below.



(a) Hybrid system hardware [52]. *(b) Audio detection performance.*

Figure 5. Demonstration of large-area microphone phased array.

A. Interfacing-driven Architectures

With regards to the challenges it poses, interfacing must be thought of in terms of physical interconnection, but also more broadly in terms of the architectural implications of bringing data from a large number of distributed sensing channels to localized ICs. Indeed, previous work has considered architectures wherein system scalability is achieved by tiling hybrid LAE-CMOS subarrays [41]. The potentially large number of tiles has motivated strategies for physical interconnection of silicon-CMOS ICs and LAE sheets, based on non-contact (capacitive/inductive) coupling. This enables assembly based on sheet lamination, avoiding the many metallurgical bonds that would otherwise be required between small rigid devices and large flexible sheets, for which no high-volume assembly approaches currently exist. But, more

generally, we point out the range of architectural challenges, which are illustrated in Fig. 6. For instance, these include, the need for sensor-localized amplification, sensor multiplexing/ sampling, modulation for signal/power transfer, etc.

While LAE TFTs offer limited performance in general, indeed motivating hybrid systems in the first place, focusing on such interfacing challenges allows us to consider specialized architectures, wherein TFT circuits and device optimizations can be thought of more selectively, to maximize system-level leverage under the device-level constraints. In fact, research on hybrid systems shows that TFTs can offer substantial leverage in addressing interfacing challenges, when approached in this way. Furthermore, such a system-level perspective can help identify important opportunities, in terms of TFT circuit topologies and device-level optimization, which have been overlooked by more traditional bottom-up perspectives alone.

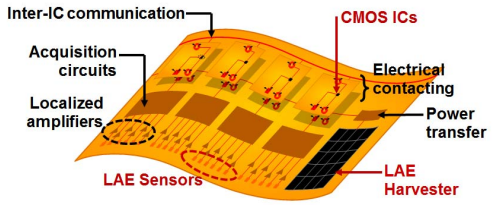


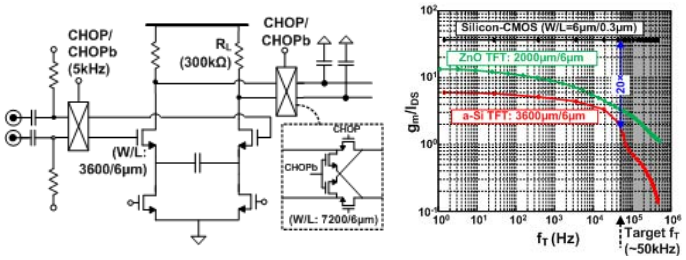
Figure 6. Illustration of hybrid-system interfacing challenges.

B. Circuits and Device Optimizations

To illustrate such a perspective, several examples are provided below. These correspond to critical TFT circuit functionality required for supporting interfacing-driven architectures, and they show how circuit topologies and device optimization can thus be pursued with more directed system-level objectives.

Low-noise TFT amplification. The distributed nature of LAE sensors, and the need to bring minute sensor signal to centralized silicon-CMOS ICs in hybrid systems, raises the need for sensor-localized low-noise TFT amplifiers. Unfortunately, structural defects in TFTs, due to low-temperature deposition, leads to increased density of traps in the semiconductor and semiconductor-dielectric interface. This results in high $1/f$ noise within TFTs [55]. Device up sizing can address this, as expected. However, such upsizing is opposed by the reduced quality of the gate dielectric, which again results due to low-temperature processing, thus causing elevated rate of TFT failures arising from pin holes [29].

Moving from the device level to the circuit level, an alternate solution is the use of chopper-stabilized amplifier topologies. But, chopper stabilization, modulating input signals to a higher frequency band, less affected by $1/f$ noise, is also challenging due to the performance limitations of TFTs. Nonetheless, the achievable TFT f_T's (Table I) suggest that modulation beyond practical $1/f$-corners is possible. The cost is lower transconductance efficiency (g_m/I_{DS}), due to biasing closer to the f_T limit. Fig. 7 shows analysis, which reveals this cost to be modest [29]. For the demonstrated amplifier topology in Fig. 7a, Fig. 7b shows the g_m/I_{DS} versus f_T for silicon CMOS and TFT technologies, under different biasing conditions. Since both g_m and I_{DS} are limited in TFTs, the overall transconductance efficiency is only moderately lower than that



(a) Amplifier circuit. *(b) g_m/I_{DS} for analysis.*

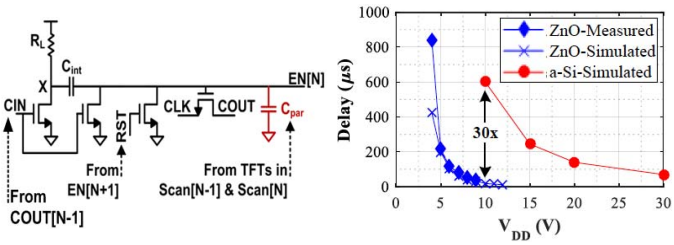
Figure 7. Low-noise TFT amplifier [29].

in silicon CMOS, and benefits are observed going from a-Si to a higher-performance ZnO TFT technology.

DC-to-AC power inversion. Power transfer from LAE harvesters, such as photovoltaics, to silicon-CMOS ICs, when exploiting scalable interfacing based on non-contact coupling in hybrid systems, requires power inversion. Though, switching topologies, popular in silicon CMOS, have the potential to achieve high power-transfer efficiency, their implementation using TFTs, as in the class-D stage demonstration in [38], faces reduced efficiently, due to TFT control-circuit losses, and low power-handling capability, due to TFT power-switch current limitations. On the other hand, an alternate topology, not conventionally considered in silicon CMOS, is the power LC oscillator, demonstrated in [39]. This can exploit the attributes of LAE devices in two ways. First, large area enables high-quality passives, such as planar inductors (i.e., large coils and wide traces), which mitigate the impacts of low-quality active devices, when used in LC oscillators. Second, through the turns ratio, inductive coupling enables high power transfer, from a low-current/high-voltage LAE domain to a high-current/low-voltage CMOS domain.

Going further, such alternate topologies drive the optimization of different device-level parameters compared to those that have traditionally been of primary focus. This can open up richer opportunities under the constraints of low-temperature processing. For instance, by absorbing TFT capacitances into the resonant tank, LC oscillators are not f_T, but rather f_{MAX} limited. Thus, in addition to f_T-oriented parameters such as semiconductor field-effect mobility, which is limited under low-temperature processing, we can focus on f_{MAX}-oriented parameters such as metal-gate resistance, which is more readily addressed under thermal constraints through geometry (thickness) and materials choices [56,57].

Scanning circuits for multi-sensor accessing. Given the potential for very large numbers of LAE sensors, scalable interfacing with silicon-CMOS ICs in hybrid systems requires scanning circuits, for sensor multiplexing. The absence of complementary TFT technology and need for scanning over many sensors, necessitates specialized circuit topologies with minimal static currents and minimal sensitivity to leakage currents, over the potentially long scanning periods. Fig. 8a shows a dynamic scanning-circuit element for sequential selection of sensors, where static currents are generated only in the element being selected, and leakage currents are designed to hold all other elements in the deselected state [58].



(a) Scanning-circuit element [58] *(b) Technology analysis [59].*

Figure 8. Analysis of selective TFT functionality in hybrid systems.

The circuit's speed is limited by an RC time constant, set by an output capacitor C_{int}, designed large to adequately pull up the parasitic capacitances of loading TFTs, and a load resistor R_L, designed large to ensure adequate voltage swing by the current of a pull-down TFT. Thus, the TFTs determine the scanning speed possible, which in turn impacts the number of sensors that can be supported under sampling-rate requirements. This enables direct assessment of technological enhancements. For instance, Fig. 8b analyzes the impact of moving from a-Si to ZnO technology [59]. In addition to higher semiconductor mobility, enabling higher speeds, ZnO enables deposition of both the semiconductor and the gate dielectric (Al_2O_3) via plasma-enhanced atomic-layer deposition (PEALD), as opposed to plasma enhanced chemical-vapor deposition (PECVD), required for a-Si semiconductor and gate dielectric (SiO_2) deposition. PEALD gives highly-conformal, well-controlled layers, permitting thinner gate dielectrics, allowing lower voltage (and thus lower power). As shown, substantial reduction of delay and V_{DD} (power) can thus be achieved for scanning-circuit functionality with such technological advances.

V. Information-Driven Hybrid-System Architectures

Given the interfacing challenges within hybrid systems described in Sec. IV and the focus on sensor inference for LAE technology motivated in Sec. II, this section explores architectural principles explicitly connecting these ideas. Namely, we note that inference over a large number of sensors implies that rather than data from individual sensors, *what is of primary interest is higher-level aggregated information, in the form of specific decisions, over all the sensors*. To actuate this idea towards addressing the interfacing challenges in hybrid systems, consider the canonical system for sensor inference, shown in Fig. 9. Such a system reduces high-dimensional data to specific decisions through feature-extraction and classification stages. In order to enhance the scalability of sensor interfacing, we can now think of drawing the line at different points in such a system. As in Sec. IV-A, this allows us to focus on selective TFT-circuit functionality through specialized topologies. But, even further, we can now exploit

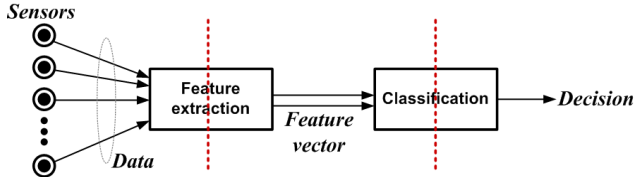


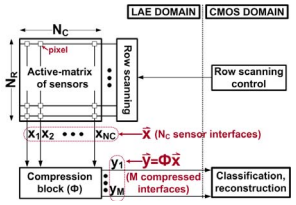
Figure 9. Canonical system for sensor inference.

powerful algorithmic tools for feature extractions and classification from machine learning and statistical signal processing. Illustrations are provided in the following subsections.

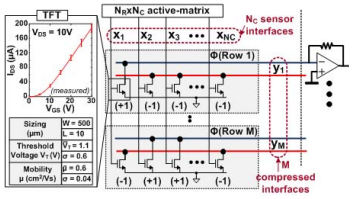
A. TFT-based Feature Extraction

Feature extraction corresponds to transforming data into a representation that enhances the generalization with which decisions about that data can be made, based on specific, well-defined metrics. In machine-learning systems, which learn how to make decisions based on similarity to previously observed data, a common approach is to transform data to a vector space, where similarity can then be assessed based on vector distances. For TFT-based feature extraction, this can shift the focus from acquiring sensor data to acquiring such distances. Noting that such distances are computable from vector inner products, this enables substantial relaxations, thanks to results from signal processing surrounding transformations that ensure the preservation of inner products. For instance, the specific information of inner products between vectors, rather than the more general information of the vector values themselves, allows for compression, which can in fact be achieved by trivial, possibly random, inner-product-preserving matrix projections [60].

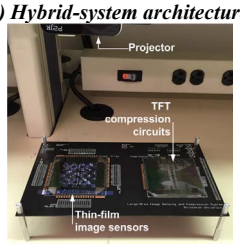
As an example, Fig. 10a shows a hybrid-system architecture where a simple compression block follows an active-matrix array of LAE image sensors [61]. As shown in Fig. 10b, following square-root reduction in the interfaces by the active matrix, the row-wise accessed data is further compressed by feeding into a TFT-implementation of matrix multiplication. Here, elements of each row in the matrix randomly correspond to +/-1, simply by hardwiring the drains of TFTs to a positive or negative current-summing node. In addition to a simple implementation, large TFT variations are tolerated, since the matrix elements themselves are meant to be random. Further, low TFT performance is overcome first by a highly parallel reduction architecture, and second because the dominant time constant, caused by the capacitance of the shared current-summing nodes, is reduced thanks to a virtual-ground condition induced by a transimpedance amplifier in the silicon-CMOS domain (which can be designed to have large open-loop gain, and thus low input impedance). Fig. 10c shows the



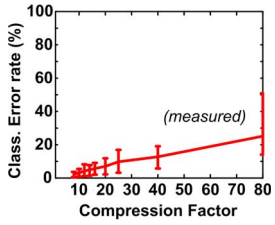
(a) Hybrid-system architecture.



(b) Random-matrix implementation.



(c) Demonstrated system.



(d) Classification performance.

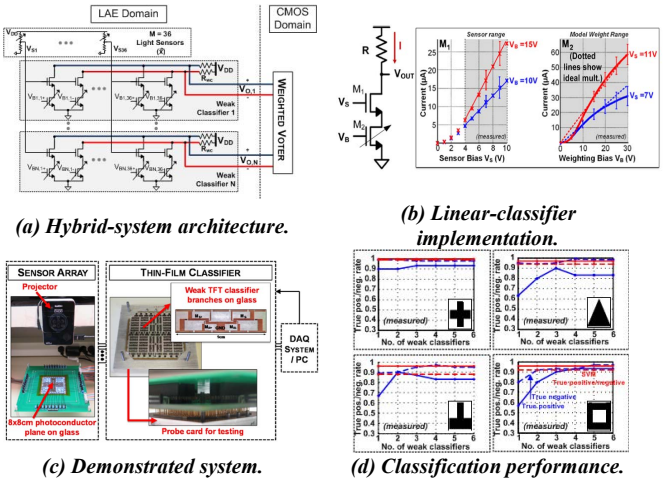
Figure 10. LAE-based feature-extraction system [61].

implemented image compression-and-detection system, integrating LAE photoconductors, and Fig. 10d shows the achieved image-classification performance on handwritten numerical digits from the MNIST dataset [62], demonstrating high compression ratios (error bars correspond to min/max performance across 10 digits).

B. TFT-based Classification

Classification corresponds to making a decision about data represented as a feature vector. In machine-learning systems, this is done by training a model using previous data, and evaluating a decision metric based on that model. Even well-generalized features can lead to complex feature-vector distributions, requiring complex models, which make TFT-evaluation infeasible. However, a class of algorithms from machine learning, referred to as boosting algorithms, allow for weak classifiers, which cannot generally be fit to such complex distributions, but which can be combined to form a strong classifier, capable of fitting to arbitrary distributions. As an example, [63] presents an algorithm referred to as Error-Adaptive Classifier Boosting (EACB). EACB extends the algorithm Adaptive Boosting (AdaBoost), whose theory allows for very weak classifiers (i.e., marginally better than 50/50 guessing), by exploiting iterative training in AdaBoost to not only overcome fitting errors in weak classifiers, but to also overcome errors due to non-ideal implementation of weak classifiers. Allowing both simpler and non-ideal implementations, makes TFT realization promising.

As an example, Fig. 11a shows a hybrid-system architecture where the outputs from TFT-implemented linear weak classifiers are provided to the CMOS domain for forming a strong classifier via weighted voting [64]. Linear classification ideally involves the product of input features with a weight derived from training, and then summation over all products. But, Fig. 11b shows that the simple implementation employed (where weights are stored by non-volatile charge trapping in the bottom TFT of a two-TFT stacks) exhibits substantial error in the multiplication transfer function. Fig. 11c shows the implemented image sensing-and-classification system, again integrating LAE photoconductors, and Fig. 11d shows that, despite the error, classification performance on simple shapes reaches the level of an ideal software-implemented support-vector machine (SVM) classifier.



(a) Hybrid-system architecture. *(b) Linear-classifier implementation.*

(c) Demonstrated system. *(d) Classification performance.*

Figure 11. LAE-based classification system [35].

VI. Conclusions and Outlook

AI systems have exhibited tremendous potential. But their extension from cyber-systems to real-world systems, interacting extensively with humans, is challenged by the efficiency and robustness with which such systems can learn and act. In addition to algorithmic solutions, a variety of technological solutions must be examined. This paper looks at technologies for large-scale, physically-integrated (PI) sensing, based on Large-Area Electronics (LAE). Initial research presented shows how thinking about algorithms in the context of the sensing technology, and the sensing technology in the context of algorithms, can enrich the design space for both.

While initial research provides compelling demonstrations of this synergy, a number of challenges remain on both the applications and system-platforms levels. Regarding the applications, with large-scale PI sensing exploiting spatial diversity and/or large cross section in sensing, how the specifications of each sensor change becomes an open question. Indeed, application level studies, for instance on the structural-monitoring sheet [65] and the acoustic-monitoring sheet [52], have shown that linearity and noise requirements on individual sensors can be relaxed in various ways thanks to the spatial diversity of sensing. Going further, studies on inference applications in AI systems, for instance in the large-area image sensing sheets [61,64], have shown that significant sensor variations can be tolerated thanks to statistical learning of detection models in the presence of such variations. This suggests the need for system specification strongly aligned with the application and application algorithms. Such application-oriented approaches to system design, in the case of large-scale sensing, face the challenge of high complexity on both levels, necessitating new design methodologies. Regarding the system platforms, while initial research has led to key design principles, and while fabrication capabilities for LAE systems are developing, further work and accessibility is needed in both areas. Of course, the design principles and fabrication capabilities must evolve in tight coordination, so that the broad creation of rich and differentiated applications can be supported. While such coordination has characterized initial efforts to some extent, such efforts are still in their infancy, and even tighter coordination will be required such efforts progress.

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