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Self-Aligned ZnO Thin-Film Transistors with 860 MHz f_T and 2 GHz f_{max} for Large-Area Applications

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High-frequency thin film transistors (TFTs) enable many important thin film circuits used in flexible large-area systems such as large bandwidth instrumentation amplifiers (related to f_T) and high-frequency oscillators (related to f_{max}) [1,2]. In [3] f_{max}=10GHz and f_T=2.9GHz were reported but using Si substrates and pulsed laser deposition for ZnO growth, which are incompatible with low-cost large-area processing on a meter scale. More modest reports of f_{max}=1GHz with sputtered IGZO on glass have relied on a very sensitive alignment process, impractical for fabrication over large substrates [4]. In this work we present a ZnO-channel TFT process fully compatible with flexible large-area substrates. We achieve an f_{max}=2GHz and f_T=860MHz by reducing source/drain (S/D) to gate overlaps (X_{ov}) and scaling channel lengths down to 500nm via a self-aligned process.

Both f_{max} and f_T depend on S/D to gate capacitances (C_{GS}, C_{GD}) as well as transconductance, g_m. Therefore, scaling X_{ov} reduces capacitance and scaling length (L) reduces capacitance while increasing g_m. Since $f_T \approx \frac{g_m}{2\pi(C_{GS}+C_{GD})} \propto \frac{1}{L\left(\frac{2}{3}L+2X_{ov}\right)}$, it scales more than linearly with length and nearly linearly with X_{ov} when X_{ov} is on the same order as L. f_{max} also depends on the gate resistance (R_G) as $f_{max} = \frac{1}{2}\frac{1}{\sqrt{R_G}}\frac{f_T}{\sqrt{2\pi f_T C_{GD}+1/r_0}}$, where r_0 is the small-signal output resistance. The gate resistance equals $R_{sheet}(1/3W + x_{tr})/(L + 2X_{ov})$, in which W is the channel width and x_{tr} is the length of the trace leading to the channel. Rewriting the equation for f_{max} in terms of L, W, and X_{ov}, we find that $f_{max} \propto \frac{1}{L\sqrt{L+2X_{ov}}}\frac{1}{\sqrt{(W/3+x_{tr})W}}\frac{1}{\sqrt{2\pi f_T C_{GD}/W+1/(Wr_0)}}$. How f_{max} ultimately depends on L and X_{ov} is set by whether the $f_T C_{GD}$ term or the $1/r_0$ term dominates. In our case, $1/r_0$ is on the order of 10^{-6} whereas $f_T C_{GD}$ is on the order of 10^{-4}-10^{-5} and, therefore, dominates. Consequently, f_{max} scales as $1/\sqrt{L}$.

We fabricated ZnO TFTs on 3”x3” glass with a staggered bottom gate structure. To reduce the gate resistance, we evaporated a Cr/Al/Cr stack with thicknesses 10/160/30nm to achieve an $R_{sheet} = 0.95\Omega/\text{sq}$. After patterning and etching the gate, a dielectric/channel/passivation Al_2O_3/ZnO/Al_2O_3 (40/10/35nm) stack was deposited by plasma-enhanced atomic layer deposition (PEALD) at 200°C. The source and drain regions are patterned using a self-alignment process in which the photoresist is exposed through the substrate with the gate metal acting as the mask (previously demonstrated for a-Si in [5]), conveniently utilizing the transparency of metal oxides (Fig. 1). We also pattern a second layer of photoresist to isolate source/drain between each transistor, in this way eliminating the need for an extra etch step. Through self-alignment, 0.6 µm overlaps are achieved (Fig. 2). In addition, the overlap reduces the channel length below the length of the gate. 0.5 µm channel lengths (measured by microscopy) are thus achieved with conventional large-area lithography. A key feature of this approach, in contrast to previous ZnO work, is that overlaps remain small even if the substrate dimensions change slightly during processing, as can occur when processing on plastic.

Typical TFT DC characteristics are shown in Fig. 3. Field-effect mobility, μ_{FE}, is approximately 8 cm^2/Vs and g_m=0.5mS when measured at V_{GS}=V_{DS}=6V, and C_{ox}=180nF/cm^2. f_T and f_{max} were extracted by measuring s-parameters with an Agilent E5061B network analyzer (Fig. 4). We varied channel lengths from 7.5 to 0.5 µm, and widths from 200 to 50 µm to characterize the effect of scaling. Fig. 5 shows how f_{max} and f_T scale with length. f_T scales as expected, and f_{max} slightly better than predicted, indicating that contact resistance is negligible down to very small channel lengths and overlaps. Scaling with width is also as predicted by modeling (Fig. 6). At V_{GS}=7.5V and W/L=50/0.5, we achieve an f_{max}=2GHz and f_T=860MHz. The use of self-alignment is critical for this result since 5µm overlaps typical of large-area manufacturing would increase the overlap capacitance by 8x, decreasing f_T by 5x and f_{max} by 3x for L=0.5µm. . While f_{max}=10GHz was previously achieved, it was accomplished with nc-ZnO, having a $\mu_{FE} = 100cm^2/Vs$. Despite the fact that our mobility is over 10x less, our f_{max} is only 5x less, indicating the strength of our process for achieving high frequencies. To the best of our knowledge, our f_{max} and f_T are the highest for metal-oxide TFTs compatible with manufacturing on plastic.

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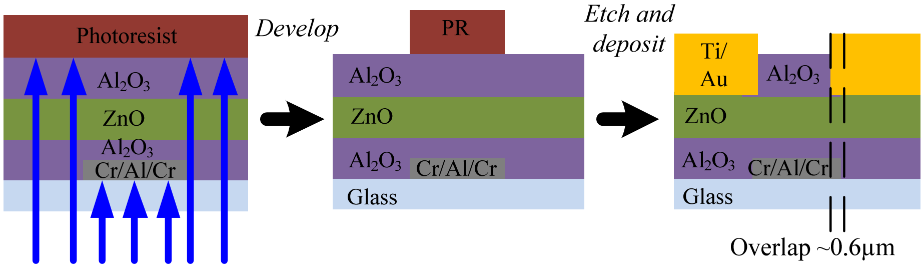

Figure 1. Self-alignment process. Source and drain are patterned using the gate metal itself, eliminating large overlap between S/D and gate needed to compensate for misalignment when using a separate mask for patterning.

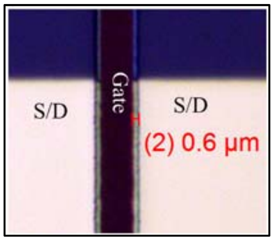

Figure 2. Micrograph of self-aligned TFT with X_{ov}=0.6µm.

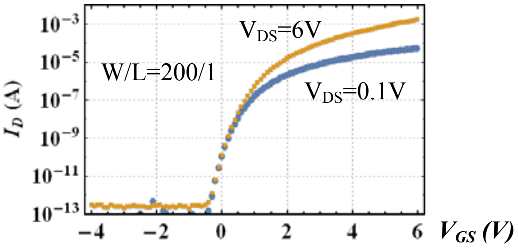

Figure 3. Typical transfer curve for self-aligned TFT.

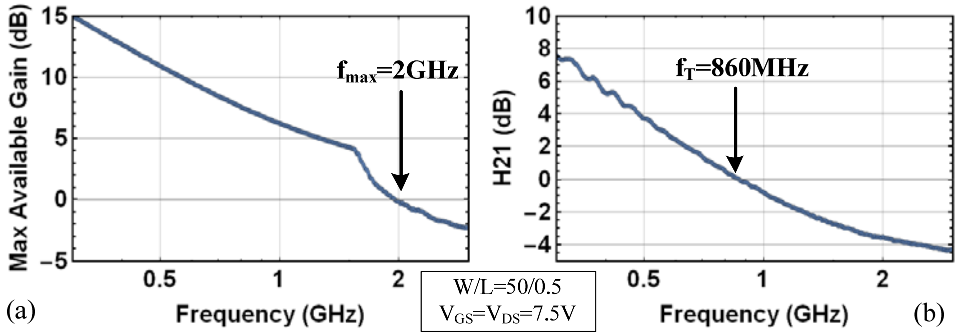

Figure 4. (a) Max available gain showing an f_{max} of 2GHz. (b) Current gain, showing an f_T=860MHz. Both (a) and (b) measured for W/L=50/0.5 at V_{GS}=V_{DS}=7.5V.

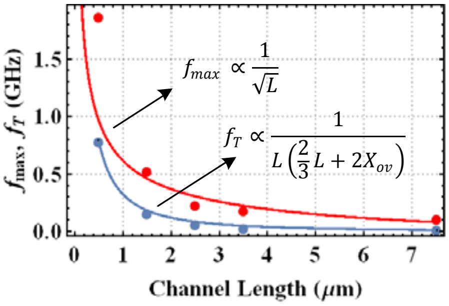

Figure 5. Experimental results for f_{max} and f_T dependence on channel length. W=50µm, V_{GS}=V_{DS}=7V. Nearly ideal scaling indicates low contact resistance down to L=0.5µm.

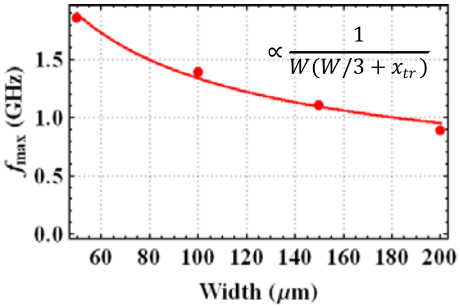

Figure 6. Measured f_{max} dependence on channel width scaling. L=0.5µm, V_{GS}=V_{DS}=7V. Large x_{tr}=50µm diminished benefit of reducing channel width.

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