Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability

Alex Z. Kattamis, Kunigunde H. Cherenack, Bahman Hekmatshoar, I-Chun Cheng, Helena Gleskova, James C. Sturm, and Sigurd Wagner

***Abstract*—The stability of thin-film transistors (TFTs) of hydrogenated amorphous-silicon (a-Si:H) against gate-bias stress is improved by raising the deposition power and temperature of the silicon nitride gate dielectric. We studied the effects of power density between 22 and 110 mW/cm^2 and temperature between 150 °C and 300 °C. The time needed to shift the threshold voltage by 2 V varies by a factor of 12 between low power and low temperature, and high power and high temperature. These results highlight the importance of fabricating a-Si:H TFTs on flexible plastic with the SiN_x gate dielectric deposited at the highest possible power and temperature.**

***Index Terms*—Amorphous-silicon (a-Si:H), electrical stability, flexible substrate, plasma power, silicon nitride gate dielectric, thin-film transistor (TFT).**

I. Introduction

HYDROGENATED amorphous-silicon (a-Si:H) thin-film transistors (TFTs) are widely used in today's active-matrix liquid crystal displays (LCDs) as pixel switches. For LCDs, the a-Si:H TFT backplane is deposited on glass at temperatures of up to 350 °C [1]; but as the deposition temperature ($T_{\rm dep}$) is reduced to make a-Si:H TFTs compatible with flexible plastic substrates, the threshold voltage (V_T) becomes less stable under gate-bias (V_G) stress [2], [3]. In fact, the V_T stability is increased by a factor of ∼5 when $T_{\rm dep}$ of the a-Si:H TFT stack is raised from 150 °C to 250 °C [4], [5]. In gate-bias space, two stability regimes are observed for a-Si:H TFTs [6], [7]. At low V_G (low electric field strength), the V_T instability is caused by defect creation and annihilation in the a-Si:H channel layer. In the high-field regime, the V_T instability is dominated by charge injection into the silicon nitride (SiN_x) gate insulator [8], [9].

Here, we report the effect on V_T stability of varying the excitation power (RF, 13.56 MHz) used in the plasma-enhanced chemical vapor deposition (PECVD) of the SiN_x gate dielectric. This letter follows an earlier work on minimizing the leakage current through SiN_x gate dielectric layers deposited at low temperature [10]. The deposition power ($P_{\rm dep}$) used for PECVD of SiN_x has an effect on built-in strain [11], [12]. As the $P_{\rm dep}$ is increased, the film's built-in stress becomes more compressive. Therefore, the built-in strain in the SiN_x gate dielectric of a-Si:H TFTs made on polyimide foil can be adjusted to reduce the overlay misalignment in the device layers [11]. This letter was motivated by the concern that the TFTs with optimized built-in stress in SiN_x gate dielectrics may not exhibit the best electrical stability.

Manuscript received February 26, 2007; revised May 7, 2007. The review of this letter was arranged by Editor J. Sin.

The authors are with the Department of Electrical Engineering and Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, NJ 08544 USA.

Digital Object Identifier 10.1109/LED.2007.900078

II. Experiments

We made a-Si:H TFTs at 150 °C and 300 °C by standard PECVD processes. The 150 °C samples were made on a 50-μm-thick Kapton E polyimide foil [3], and the 300 °C TFTs were made on a 75-μm-thick high temperature clear plastic [5]. Five samples were made. The 150 °C TFT sets, samples (1–3), had SiN_x gate dielectrics deposited at RF power densities ($P_{\rm dep}$) of 22, 53, and 110 mW/cm^2 (electrode area = 227 cm^2), and the two 300 °C sets, samples (4, 5), at 22 and 88 mW/cm^2. Deposition conditions are summarized in Table I. The a-Si:H TFTs were fabricated in a standard bottom-gate staggered nonself-aligned source–drain (S/D) geometry [3]. Channel width and length were $W = 80$ μm and $L = 40$ μm. Layer thicknesses are inscribed in the cross section of Fig. 1. The polymer substrate was first passivated with 200 nm of PECVD SiN_x on the front and the backside. The passivation was deposited at 150 °C for samples (1–3) and 300 °C for samples (4, 5). The gate and source-drain metal each were 50 nm of Cr deposited by thermal evaporation. The a-Si:H TFT stack consisting of ∼300-nm SiN_x gate dielectric, 200-nm intrinsic (i) a-Si:H channel layer, and 50-nm n$^+$ a-Si:H doped S/D deposited according to sample. For samples (1–3), the SiN_x dielectric was deposited using a H_2 diluted recipe [10], which has been shown to yield better quality films at low temperatures (150 °C). The flow ratios were $SiH_4 : NH_3 : H_2 = 1 : 10 : 44$, $SiH_4 : H_2 = 1 : 1$, and $PH_3 : H_2 : SiH_4 = 0.01 : 1 : 7$ for the SiN_x, i a-Si:H, and n$^+$ a-Si. For samples (4, 5), the SiN_x was deposited without dilution. The flow ratios were $SiH_4 : NH_3 = 1 : 9$, SiH_4, and $PH_3 : H_2 : SiH_4 = 0.01 : 1 : 7$ for the SiN_x, i a-Si:H, and n$^+$ a-Si. The i a-Si:H and n$^+$ a-Si:H were all deposited at 17 mW/cm^2. The etch rates in buffered oxide etchant (BOE, $HF : NH_4 : H_2O = 1 : 4 : 5$) [13] and refractive indexes (by ellipsometry) were measured on gate dielectric layers deposited separately on Si wafers.

The TFTs were electrically stressed using an HP4155A parameter analyzer, by applying a positive gate-bias voltage with source and drain grounded. We chose to use $V_{\rm DS} = 0$ V since this produces larger threshold shifts particularly in the low-field regime [14]. After each gate-bias step, the TFT transfer curve was plotted for $V_{\rm DS} = 100$ mV and $V_{\rm GS}$ from −15 to 30 V. We chose V_T as the voltage at which the curve passes through $I_D = 5$ pA. In the first series, separate TFTs were stressed for

TABLE I
DEPOSITION CONDITIONS FOR THE a-Si:H CHANNEL LAYER AND THE SiN_x DIELECTRIC LAYERS

	i a-Si:H Channel Layer			SiN_x Gate Dielectric		
TFT Sample #	*Power Density (mW/cm^2)*	*Temp. (°C)*	*Source Gas Ratio*	*Power Density (mW/cm^2)*	*Temp. (°C)*	*Source Gas Ratio*
1	17	150	SiH_4:H_2 = 1:1	22	150	SiH_4:NH_3:H_2 = 1:10:44
2	17	150	SiH_4:H_2 = 1:1	53	150	SiH_4:NH_3:H_2 = 1:10:44
3	17	150	SiH_4:H_2 = 1:1	110	150	SiH_4:NH_3:H_2 = 1:10:44
4	17	280	SiH_4	22	300	SiH_4:NH_3 = 1:9
5	17	280	SiH_4	88	300	SiH_4:NH_3 = 1:9

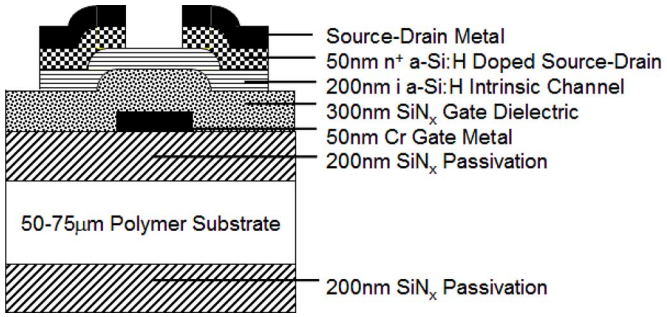

Fig. 1. Cross section of the bottom-gate staggered source-drain a-Si:H TFT deposited on a polymer substrate, used in this letter.

600-s stress time ($t_{\rm stress}$) at different gate-bias field ($E_{\rm stress}$) strengths. In the second series, separate TFTs were stressed under V_G of 10^7 V/m (low field) and 10^8 V/m (high field) for $t_{\rm stress}$ up to 10 000 s.

III. RESULTS

A decrease in etch rate is associated with an increase in SiN_x film density and a decrease in its hydrogen content [15]. In Fig. 2(a), the etch rate of the SiN_x versus $P_{\rm dep}$ is plotted for the five samples of Table I. The etch rate for Si_3N_4 deposited by CVD at 900 °C is shown for comparison [15]. The index of refraction increases rises with increasing plasma power, as shown in Fig. 2(b), which also indicates a reduction in hydrogen content [12], [15].

In Fig. 3, ΔV_T is plotted versus $E_{\rm stress}$. The ΔV_T is plotted versus $t_{\rm stress}$ in Fig. 4 for both the low-field (10^7 V/m) and high-field (10^8 V/m) conditions. For comparison, Fig. 4 also includes results from the study in [3] for an a-Si:H TFT on Kapton E made at 150 °C using an 88 mW/cm^2 plasma power for the SiN_x.

At high bias-stress fields, Figs. 3 and 4 exhibit large differences in ΔV_T, but not at low fields. The spread in ΔV_T below 1×10^7 V/m in Fig. 3 is less than 0.2 V, but as the gate-bias field is increased, the spread in ΔV_T increases. At 2×10^8 V/m, ΔV_T in the 150 °C samples (1–3) is reduced by 2 V when going from low to high PECVD power. Increasing the $T_{\rm dep}$ from 150 °C to 300 °C (4, 5) reduces ΔV_T by as much as 6 V. The pronounced effect of high gate bias on ΔV_T results from charge injection into the dielectric at high field. Raising the $T_{\rm dep}$ also reduces ΔV_T as has been reported earlier. Fig. 4

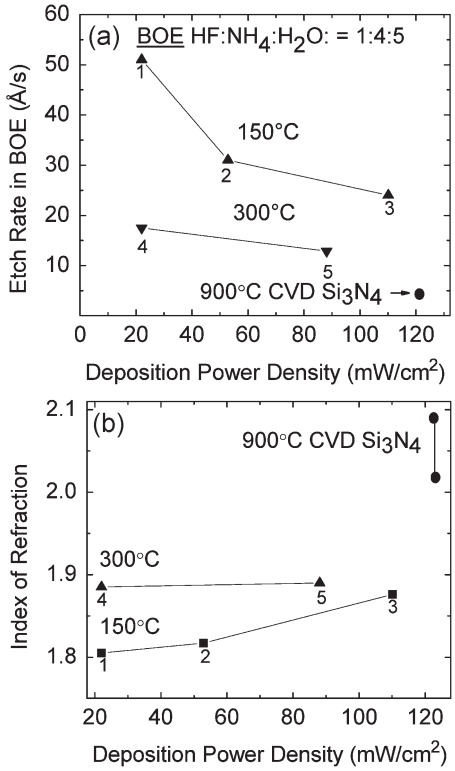

Fig. 2. (a) Etch rate in BOE versus SiN_x deposition power density and temperature. The etch rate for 900 °C CVD Si_3N_4 is taken from the study in [14]. (b) Index of refraction versus SiN_x deposition power and temperature. The value for CVD SiN_x is taken from the study in [15].

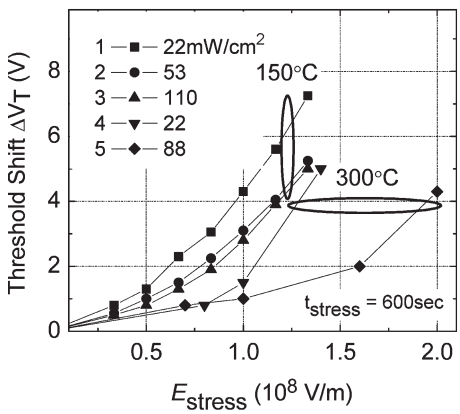

Fig. 3. Threshold voltage shift versus gate-bias field, using a 600 s $t_{\rm stress}$.

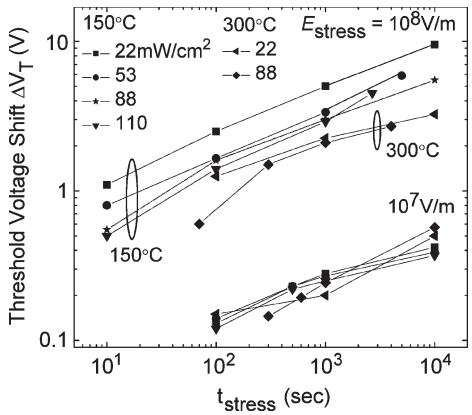

Fig. 4. Threshold voltage shift versus $t_{\rm stress}$. The two sets of curves are for gate-bias fields of 10^7 and 10^8 V/m. A curve from the study in [3] at 10^8 V/m for 88 mW/cm^2 deposition has been added.

makes clear that in the low-field regime, the spread in ΔV_T is small regardless of $P_{\rm dep}$ and temperature. This observation supports the published conclusion that ΔV_T in this bias regime results from the formation of defects in the a-Si:H channel material. The dangling-bond density in high-quality i a-Si:H deposited between 150 °C and 250 °C is $\sim 2 \times 10^{15}$ cm^{-3}, and it does not vary much with temperature [7]. The difference in ΔV_T is equally small. In the high-field regime, the differences between samples are pronounced.

We convert the reduction in ΔV_T to the increase in $t_{\rm stress}$ needed to reach a certain ΔV_T. For the purpose of illustration, we choose $\Delta V_T = 2$ V. At 150 °C, increasing the $P_{\rm dep}$ from 22 to 53 mW/cm^2 (1, 2) lengthens $t_{\rm stress}$ by a factor of 3.5, and a further increase to 110 mW/cm^2 by another factor of 2.5. Depositing at 300 °C (4, 5) brings yet another factor of 1.4. These reductions in ΔV_T correlate with the reduction in etch rate and increase in refractive index. It is evident that raising the $P_{\rm dep}$ raises the TFT stability against threshold voltage shift. The data from the study in [3] for a 150-°C TFT with 88-mW/cm^2 SiN_x gate dielectric fit between the 53 and 110 mW/cm^2, samples (2, 3), as expected. This enhancement of TFT stability, which is obtained by increasing $P_{\rm dep}$, is nearly identical at the temperatures of 150 °C–300 °C.

Previous work has shown that if the deposition conditions favor formation in the plasma of aminosilanes, $Si(NH_2)_n$, the hydrogen that is incorporated into the SiN_x becomes bonded to nitrogen instead of silicon [16], [17]. N–H bonding may reduce charge injection and thereby reduce the high-field V_T shift. Our sample 5 (300 °C/110 mW/cm^2) possibly exhibits this effect, because its etch rate in BOE of ~ 12 Å/s is almost identical to that found in [16].

We found that the stability of a-Si:H TFTs against electrical gate-bias stress is raised by increasing the deposition power for the SiN_x gate dielectric. Earlier, we showed that the deposition power can be used to control the mask overlay alignment in TFT fabrication on free-standing substrates, often by depositing at low power to compensate thermal strain [11]. These conflicting requirements suggest that the dimensional control of free-standing substrate dimension should be assigned to the substrate passivation (buffer) layers rather than the TFT gate dielectric.

IV. Conclusion

For maximum stability, the SiN_x gate dielectric of a-Si:H TFTs must be deposited at the highest possible temperature and deposition power. Because the SiN_x deposition power also is used to adjust the stress in the TFT/flexible substrate structure, it is advisable to adjust stress and TFT stability independently. This can be done by adjusting stress in the SiN_x buffer layers that serve for substrate passivation, and depositing the SiN_x gate insulator for maximum stability.

Acknowledgment

The authors would like to thank the Unites States Display Consortium for support of this work and the DuPont Company for technical collaboration. One author, A. Z. Kattamis, would like to thank the Princeton Plasma Physics Laboratory for a fellowship.

References

[1] T. Tsukada, "Active-matrix liquid-crystal displays," in *Technology and Applications of Amorphous Silicon*, R. A. Street, Ed. Berlin, Germany: Springer-Verlag, 1999, pp. 7–93.

[2] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 18, no. 2, pp. 683–689, 2000.

[3] H. Gleskova and S. Wagner, "DC-gate-bias stressing of a-Si:H TFTs fabricated at 150 °C on polyimide foil," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1667–1671, Aug. 2001.

[4] K. Long, A. Z. Kattamis, I-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, "Stability of amorphous-silicon TFTs deposited on clear plastic substrates at 250 °C to 280 °C," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 111–113, Feb. 2006.

[5] K. H. Cherenack, A. Z. Kattamis, B. Hekmatshoar, J. C. Sturm, and S. Wagner, "Amorphous silicon thin-film transistors fabricated at 300 °C on a clear plastic substrate foil," *IEEE Electron. Device Lett.*, 2007. submitted for publication.

[6] M. J. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753–2763, Dec. 1989.

[7] R. A. Street, *Hydrogenated Amorphous Silicon*. Cambridge, U.K.: Cambridge Univ. Press, 1991.

[8] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286–1288, Mar. 1993.

[9] M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 51, no. 16, pp. 1242–1244, Oct. 1987.

[10] H. Gleskova, S. Wagner, V. Gašparík, and P. Kováč, "Low-temperature silicon nitride for thin-film electronics on polyimide foil substrates," *Appl. Surf. Sci.*, vol. 175/176, pp. 12–16, 2001.

[11] I-C. Cheng, A. Kattamis, K. Long, J. C. Sturm, and S. Wagner, "Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates," *J. Soc. Inf. Disp.*, vol. 13, no. 7, pp. 563–568, 2005.

[12] S. K. Ghandhi, *VLSI Fabrication Principles: Silicon and Gallium Arsenide*, 2nd ed. New York: Wiley, 1994.

[13] Phillipsburg, NJ: Mallinckrodt Baker Inc. [Online]. Available: http://www.jtbaker.com

[14] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 188–190, Apr. 2004.

[15] W. Kern and R. S. Rosler, "Advances in deposition processes for passivation films," *J. Vac. Sci. Technol.*, vol. 14, no. 5, pp. 1082–1099, Sep. 1977.

[16] D. Smith, A. Alimonda, C. Chen, S. Ready, and B. Wacker, "Mechanism of SiN_xH_y Deposition from NH_3-SiH_4 plasma," *J. Electrochem. Soc.*, vol. 137, no. 2, pp. 614–623, 1990.

[17] D. Murley, R. Gibson, B. Dunnett, A. Goodyear, and I. French, "Influence of gas residence time on the deposition of nitrogen-rich amorphous silicon nitride," *J. Non-Cryst. Solids*, vol. 187, pp. 324–328, 1995.