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Phosphorus Doping and Sharp Profiles in Silicon and Silicon-Germanium Epitaxy by Rapid Thermal Chemical Vapor Deposition

Min Yang,[a] Malcolm Carroll,[a] J. C. Sturm,[a,*,z] and Temel Büyüklimanli[b]

[a]*Department of Electrical Engineering, Center for Photonics and Optoelectronic Materials, Princeton University, Princeton, New Jersey 08540, USA*
[b]*Evans East, East Windsor, New Jersey 08520, USA*

In situ phosphous doping of silicon epitaxy from 700 to 1000°C by low pressure rapid thermal chemical vapor deposition in a cold wall system, using dichlorosilane as the silicon source, has been investigated. At a high phosphine flow rate, the growth rate of silicon decreases dramatically (by ~60%) and the phosphorus incorporation level saturates. A significant persistence effect of phosphorus after turning off phosphine is observed. However, a sharper transition and higher doping level are observed in $Si_{1-x}Ge_x$ layers grown at 625°C. Improvement of the phosphous profile in silicon to ~13 nm/decade is demonstrated by reactor cleaning and *ex situ* etching of the wafer surface during a growth interruption after phosphorus-doped epitaxy. Despite the growth interruption, an *in situ* 800°C bake at 10 Torr in hydrogen before regrowth can give an oxygen- and carbon-free interface without excessive dopant diffusion.

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Low temperature (≤800°C) silicon epitaxy by chemical vapor deposition (CVD) has been applied to a variety of silicon devices. In contrast to boron doping in silicon with high concentration (>10^{20} cm^{-3}) and sharp profiles (5-10 nm/decade on both leading and trailing edges),[1,2] high concentration n-type doping with an abrupt profile has always been difficult. It has been reported that phosphine and arsine severely depress the silicon growth rate, and that residual dopant in the chamber and phosphorus segregation on the wafer surface can also cause an unintentional doping tail after the n-type dopant gas is turned off.[3-11] Most n-type doping studies employed silane or disilane as the silicon source gas. Dichlorosilane (DCS) n-type studies have not been widely reported in the literature. Although Sedgwick *et al*.[12,13] reported that at atmospheric pressure, growth rate enhancement and sharp profiles were achieved using dichlorosilane and phosphine/arsine, it is well known that using dichlorosilane or other chlorine-containing sources at low temperatures (600-800°C) in low pressure CVD (LPCVD) leads to similar problems as silane and disilane.[14-16] Recently, Churchill *et al*.[17] successfully grew arsenic modulation doping in Si/SiGe heterostructures by interrupting the SiGe growth while the surface was exposed to dopant gas and then resuming the growth, similar to that described in Ref. 18. The doping level was controlled by the exposure time, temperature, and dopant gas partial pressure. Ismail *et al*. used a growth interruption after n^+ silicon epitaxy by ultrahigh vacuum (UHV) CVD[19] to improve the phosphorus profile. The main idea included purging the system with hydrogen after turning off phosphine and meanwhile, taking samples outside growth chamber and etching them in diluted HF before reloading. However, the interrupted growth caused an oxygen spike at the interface,[20] limiting potential device applications.

While the epitaxial growth of both Si and now $Si_{1-x}Ge_x$ for integrated circuits widely uses DCS as the silicon source, the phosphorus incorporation and profile problems have not been widely reported with DCS. Therefore, in this paper, we present *in situ* phosphorus doping in both Si and SiGe epitaxial layers grown by CVD using DCS at temperatures of 625-800°C. Similar to the growth with silane and disilane, at a high phosphine flow rate, the growth rate is reduced and phosphorus incorporation begins to saturate. Sharper and higher phosphorus doping in $Si_{1-x}Ge_x$ samples are observed. Various surface treatments during the growth interruption for epitaxial silicon is studied to create sharp phosphorus profiles. We find that after etching a 10-50 Å surface away from the n^+ silicon epitaxial layer outside the growth chamber, the phosphorus profile improves from 155 nm/decade in the untreated sample to 13 nm/decade for the growth at 700°C with 5×10^{-4} standard cubic centimeters per minute (sccm) phosphine flow. Growing a sacrificial wafer reduces the residual phosphorus in the growth chamber, improving the background doping from 10^{18} to 10^{17} cm^{-3}. An *in situ* low temperature cleaning (800°C) is used before regrowth. An oxygen- and carbon-free interface is achieved, enabling various device applications.

Growth Rate and Phosphorus Levels

The epitaxial silicon layers of all samples in this paper were grown on silicon (001) substrates in a rapid thermal CVD (RTCVD) system.[21] Dichlorosilane (26 sccm) and phosphine are used as the silicon and phosphorus sources. The phosphine was diluted to 100 ppm in hydrogen, but the phosphine flow rates reported in this paper are those of only the phosphine calculated by the measured flow rate of the diluted source and the source concentration. The growth pressure is 6 Torr with a hydrogen flow of 3 Lpm. A typical phosphorus doping profile without any growth interruption is plotted in Fig. 1. It was measured by secondary ion mass spectroscopy (SIMS) using a 3 keV Cs primary ion beam. The SIMS measurement errors in the depth scales and concentrations are in the range of 5-10% and 15-20%, respectively. Three all-silicon samples were grown at 700, 800, and 1000°C, respectively, with constant dichlorosilane and hydrogen flow rate and constant temperature and pressure for each sample. The phosphine flow was first turned on for a period of 1000 s for a flow rate of 5×10^{-4} sccm, and then turned off for 1000 s, with dichlorosilane on the entire time. This 1000 s-on/1000 s-off cycle was then repeated for phosphine flow rates of 1×10^{-3}, 3×10^{-3}, and 1×10^{-2} sccm. Identical experiments were done at 800°C (90 s intervals) and 1000°C) (20 s intervals).

The silicon growth rate at 700 and 800°C as a function of phosphine flow rate is plotted in Fig. 2a. The silicon growth rate is reduced at high phosphine flow rate by 60% for both 700 and 800°C growth, which is qualitatively similar to that using silane or disilane sources in both CVD and gas source molecular beam epitaxy systems.[3,5-7,9-11,22-30] There are fewer works using dichlorosilane source, but similar phenomena have been observed with both arsenic[14] and phosphorus[15] doping using dichlorosilane in silicon-selective epitaxy at 775-1050°C. In the case of silane, the explanation given[4,22,31] is that at temperatures higher than 400°C (the desorption temperature of hydrogen), a high level of phosphorus accu-

* Electrochemical Society Active Member.
z E-mail: sturm@ee.princeton.edu

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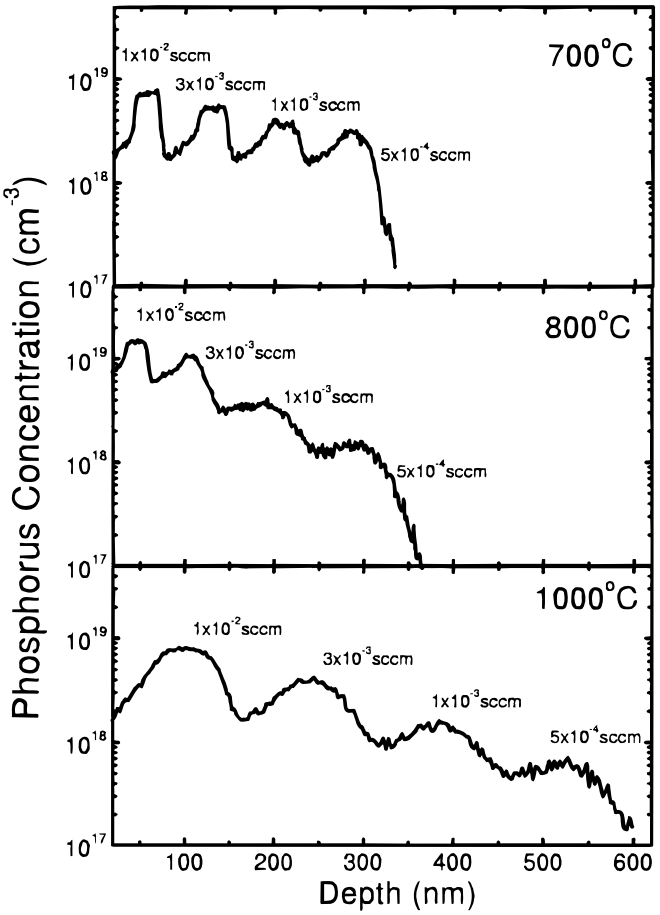

Figure 1. Phosphorus profiles from SIMS measurements for samples grown by RTCVD at 700, 800, and 1000°C using DCS and PH_3. The PH_3 flow was switched on and off periodically, giving four peaks in each sample, corresponding to PH_3 flow rates of 5×10^{-4}, 1×10^{-3}, 3×10^{-3}, and 1×10^{-2} sccm.

mulates at the silicon surface during the CVD process and blocks free active sites on the surface, thus reducing the surface reaction.

Figure 2b shows the peak phosphorus levels observed by SIMS as a function of the phosphine flow rate for 700, 800, and 1000°C growth temperatures. For the silicon layers grown at 800 and 1000°C, the doping level is in line with the phosphine flow rate when the flow rate is low. At high phosphine flow, despite presumably high phosphorus levels on the surface (significantly depressing the growth rate), the amount of phosphorus incorporated is small (1.4×10^{19} cm^{-3} for 1×10^{-2} sccm at 800°C), and the phosphorus doping level approaches saturation in contrast with other dopants such as boron. For the silicon layer grown at 700°C, the phosphorus concentration goes as the flow rate to the 0.3 power. In the case of silane, Jang *et al.*[25] reported that the P_2 dimer formation upon increasing of phosphine limits silane adsorption and prevents monatomic phosphorus incorporation into silicon despite a high degree of surface coverage, although P_2 dimer formation is still debatable.[5,32] In our work, for a phosphine flow rate less than 3×10^{-3} sccm, higher phosphorus incorporation is observed at lower growth temperatures consistent with the trend reported in Ref. 9, 24, 33, 34, and 35. It is possibly attributable to the enhanced desorption of phosphorus from a silicon surface with increasing temperature when $T > 550$°C.[4,36] However, when phosphine flow rate increases to 1×10^{-2} sccm, the highest phosphorus incorporation level occurs at a growth temperature of 800°C. Furthermore studies are necessary to fully understand phosphorus incorporation into silicon epitaxial layers.

Phosphorus profiles for a multilayer sample with phosphorus doped $Si_{1-x}Ge_x$ alloys separated by nominally undoped silicon layers are shown in Fig. 3. The SiGe alloys were grown at 625°C with germane (105 sccm for $x = 0.2$ and 30 sccm for $x = 0.1$) and DCS (26 sccm), while the silicon layers were grown at 700°C. At the end of each silicon layer and start of each SiGe layer, the dichlorosilane flow was left constant and the wafer temperature was lowered from 700 to 625°C. The germane and phosphine were then turned on simultaneously. At the end of the SiGe layers, the germane source was first shut of, and the temperature was raised 30 s later to 700°C to grow silicon. (The silicon growth rate of 625°C with dichlorosilane is ~4 Å/min.) The phosphine flow rate is chosen to be 5×10^{-4} sccm for all the SiGe layers. The exact point at which the phosphorus source was turned off varied, as shown in Fig. 3. The phosphine was turned off in the center of each SiGe layer, except for the middle SiGe layer where phosphine was turned off simultaneously with germane. We did not grow any undoped SiGe layers in these experiments, but the growth rate for 5×10^{-4} sccm phosphine flow rate is similar to that previously observed in our lab for undoped SiGe layers under the same condition.[37] Higher phosphorus incorporation in SiGe alloys than that in Si is observed. The phosphorus level increases with the germanium content: 2.5×10^{19} cm^{-3} in $Si_{0.8}Ge_{0.2}$, *vs.* 1.3×10^{19} cm^{-3} in $Si_{0.92}Ge_{0.08}$, *vs.* 2×10^{18} cm^{-3} in silicon. The observed enhancement of phosphorus incorporation in $Si_{1-x}Ge_x$ has also been observed using silane.[11,25] Chen *et al.* attributed the effect solely to the increased hydrogen desorption rate in the presence of germanium.[11] However, this explanation is not convincing because the increased hydrogen desorption is known to increase

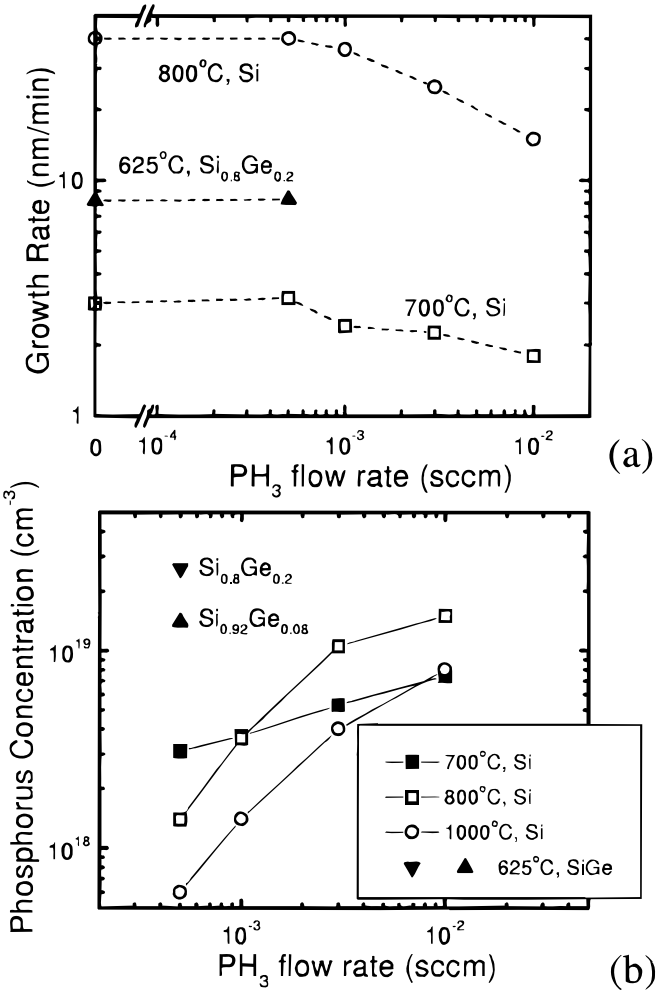

Figure 2. (a) Growth rate and (b) phosphorus peak concentration as a function of phosphine flow rate for the growth of silicon at 700, 800, and 1000°C, and $Si_{0.8}Ge_{0.2}$ at 625°C.

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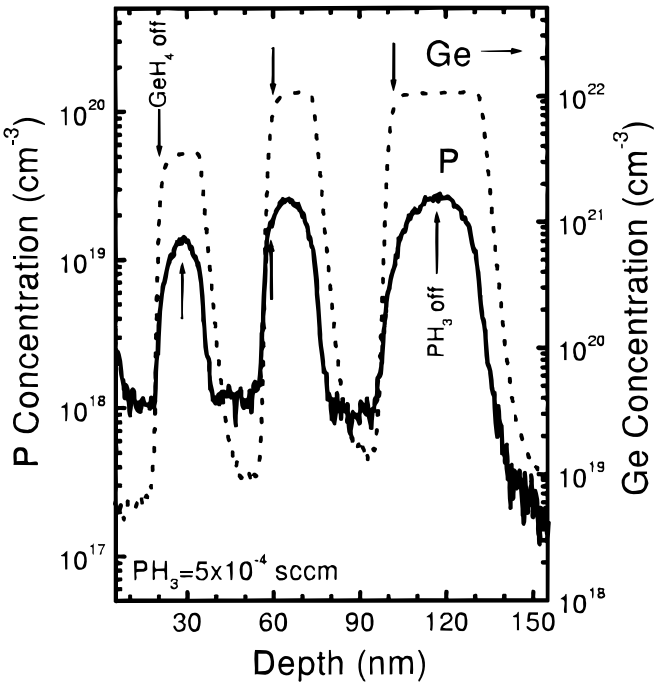

Figure 3. Phosphorus doping profiles (by SIMS) in $Si_{1-x}Ge_x$ epitaxy layers grown at 625°C with a PH_3 flow rate of 5×10^{-4} sccm. The SiGe layers are separated by silicon layers grown at 700°C.

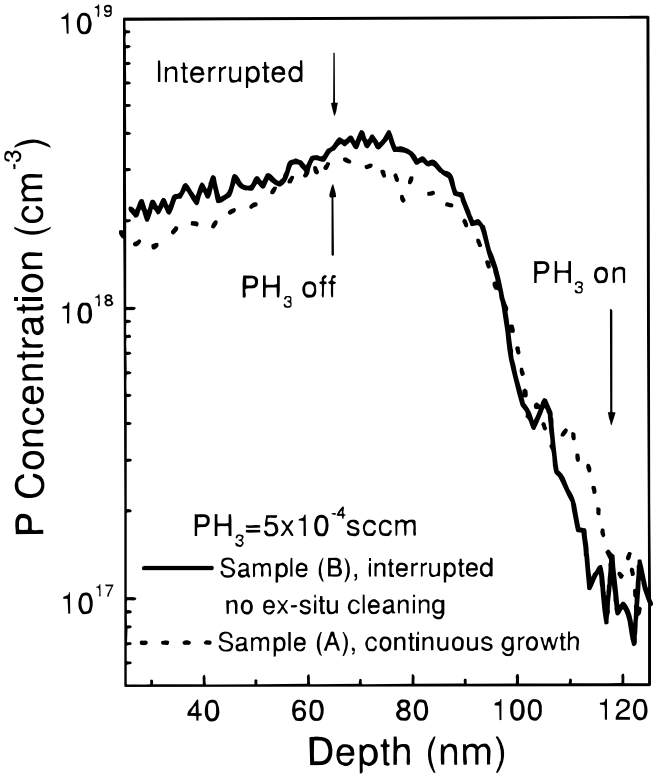

Figure 4. Phosphorus profiles (by SIMS) from sample A (using conventional continuous growth) and sample B (interrupted growth without any *ex situ* cleaning), grown at 700°C, with phosphine flow rate of 5×10^{-4} sccm. Profile of sample A is replotted from Fig. 1.

the growth rate, which would decrease doping level. Jang *et al.*[25] attributed the effect of germanium to the fact that P_2 dimers are hindered by germanium, so that the fraction of monatomic phosphorus is increased, leading to increased phosphorus incorporation.

Interface Abruptness

The phosphorus profile for the sample grow at 700°C is replotted in Fig. 4 as a dashed line. The phosphine flow rate was 5×10^{-4} sccm, giving a peak phosphorus concentration of 3×10^{18} cm^{-3}. At the leading edge, when the phosphine was turned on, the transition slope is about 19 nm/decade. When the phosphine was turned of in the middle of the silicon layer, however, the phosphorus doping density was above 10^{18} cm^{-3} in the 70 nm silicon layer above the intentionally doped layer, yielding a slope for the decay of the phosphorus concentration of 155 nm/decade (trailing edge). Sharper profiles are observed at higher phosphorus flow rate for a given growth temperature, as shown in Fig. 1. For example, at 700°C, the transition at the leading edge is 13.7 and 51 nm/decade for phosphine flow rates of 1×10^{-2} and 1×10^{-3} sccm, respectively, while the trailing edge of 1.37 and 93 nm/decade. Furthermore, sharper phosphorus profiles also occur at lower growth temperature for a given phosphine flow rate. For example for a 1×10^{-2} sccm phosphine flow rate, the transition slope at the trailing edge is 45 and 91 nm/decade at 800 and 100°C, respectively, while the slope at the leading edge is 19 and 45 nm/decade. The transient response of the phosphine/silane doping profiles have been studied by Kamins *et al.*[16] on the slow transition at the leading edges. Reif *et al.*[35] reported that at high temperatures (T = 1000-1080°C) in the mass transport-limited regime, the decay length of the phosphous profile is proportional to the silicon deposition rate, similar to the result in this work using dichlorosilane: lower growth temperature and high phosphine flow rate lead to lower growth rate and thus result in the sharper phosphorus profiles we observed. The physical mechanisms dominating the transient process are related to the time needed by the adsorbed layer to reach the new steady-state population of dopant species. Slower deposition rate leads to shorter thickness to achieve this condition. The decay rate at 800°C for low phosphorus flows is especially poor, worse than that at 1000°C, perhaps due to the fact that the phosphorus can evaporate from the surface to some degree at 1000°C but not at 800°C.

As seen in Fig. 1 after introducing phosphine, the phosphorus background doping level in the subsequent unintentionally doped silicon layers is higher than 5×10^{17} cm^{-3} in all cases. At lower temperature and higher phosphine flow rate, the background doping level is even higher. The high level of background doping after turning off phosphine has also been reported by Bashir *et al.*[38] The characteristics of slowly decaying profiles (especially on the trailing edge) and high background doping levels effect of phosphorus doping significantly limit its device applications. There may be three mechanisms of this memory effect: (*i*) auto-doping from residual phosphorus inside the growth chamber, (*ii*) the high fraction of phosphorus on the wafer surface, which results from the high phosphorus adsorption coefficient on silicon surface mentioned in the previous paragraphs and the phosphorus segregation at the moving growth interface,[38] and (*iii*) solid-state diffusion of phosphorus. The third reason can be ruled out at or below 800°C due to the low diffusion coefficients. The first mechanism is supported by the observation the after a high phosphine flow, a significant phosphorus background doping level has been observed in subsequent wafers grown in the same chamber. Similar phenomena have also been published using silane.[5,19,39]

In the case of SiGe, as mentioned above, the germanium is thought to reduce phosphorus coverage on the wafer surface and reactor surfaces, and thus results in sharper phosphorus profiles in $Si_{1-x}Ge_x$ than those in silicon epitaxial layers. Sharper n-type doping profiles have been observed in $Si_{1-x}Ge_x$ alloy (*vs.* Si) using silane.[18,25] In our case, for the same phosphine flow (5×10^{-4} sccm), the transition is much faster in $Si_{1-x}Ge_x$ layers than that in silicon. The leading edge of the phosphorus profiles in $Si_{0.8}Ge_{0.2}$ alloys is only 6.8 nm/decade, as shown in Fig. 3. However, there is also a slow decay rate of phosphorus in the SiGe layers when phosphine is turned off. But phosphorus profile falls rapidly when switching to silicon growth at 700°C, which is obvious comparing the two trailing edges of the phosphorus profiles in $Si_{0.8}Ge_{0.2}$ layers. The transition is sharper when phosphine and ger-

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Table I. Various surface treatments for samples studied in this paper.

Sample	Continuous *vs.* interrupted growth?	Remove wafer from growth chamber?	Sacrificial wafer during interruption?	Oxidation in $H_2SO_4 + H_2O_2$ and etch in HF	*In situ* cleaning in 3 Lpm H_2
A	continuous	No	—	—	—
B	interrupted	No	No	No	Cold 15 min 6 Torr and 800°C 45 s 10 Torr
C	interrupted	Yes	Yes	No	800°C 45 s 10 Torr
D	interrupted	Yes	Yes	Yes, once	800°C 45 s 10 Torr
E	interrupted	Yes	No	Yes, 5 times	800°C 45 s 10 Torr
F	interrupted	Yes	Yes	Yes, 5 times	800°C 90 s 10 Torr

mane are switched off simultaneously. This may be due to the lower growth rate or low incorporation of surface phosphorus into silicon layers as discussed before.

Improvement of Phosphorus Profiles

To identify the dominant mechanism of phosphorus persistent effect on silicon epitaxial layers and to eliminate its effect, especially on the trailing edge, the growth was interrupted after the phosphorus-doped layer and various steps were applied to clean the wafer surface or the reactor surfaces. The surface treatments studied here are listed in Table I. All the samples discussed in the following were grown at 700°C with n-type doping by using 5×10^{-4} sccm phosphine and 26 sccm dichlorosilane. It was reported that phosphine adsorption decreases to 10% of its maximum value at 800°C.[4] To test if baking at 800°C would help to remove residual phosphorus in the chamber and on the wafer surface, the n-type growth of sample B (identical to sample A in dashed line in Fig. 4) was interrupted by turning off phosphine and dichlorosilane and cooling the wafer down to room temperature. Hydrogen (3 Lpm) was flowed for 15 min to purge the chamber (6 Torr), followed by an 800°C bake at 10 Torr for 45 s in 3 Lpm hydrogen. Another 70 nm silicon without additional phosphine was grown at 700°C after the interruption. No obvious improvement in the phosphorus profile is observed (solid line in Fig. 4). We conclude that the 800°C bake does not remove phosphorus from the wafer surface and/or that the residual phosphorus source is on the reactor walls, whose temperature is estimated at a few hundred degrees Celsius. This kind of growth interruption and *in situ* hydrogen purge has been used widely in devices after n-type doping with silane,[39] but no significant influence on the dopant profile was found in some reports.[16,38]

To more thoroughly clean the sample surface and the growth chamber, samples C and D were removed from the growth chamber after identical n-type growth as samples A and B. A sacrificial wafer was then grown to getter residual phosphorus in the growth chamber. The sacrificial wafer included a 1 μm silicon layer grown with dichlorosilane at 1000°C and a 300 nm $Si_{0.65}Ge_{0.35}$ layer at 625°C from dichlorosilane and germane, without flowing any dopant gases. The low temperature SiGe layer was added because we believe germanium can getter phosphorus residual in the reactor, as previously mentioned. Sample C was dipped in diluted HF (50:1) before reloading into the growth chamber in order to remove any possible native oxide after exposure to air. The sample was baked at 800°C for 45 s in 3 Lpm hydrogen at 10 Torr before the 700°C undoped Si regrowth. However, the phosphorus doping profile is not improved (shown in Fig. 5). Sample D was soaked in H_2SO_4:H_2O_2 (2:1) for 20 min before the HF dip. The chemical oxide grown on the sample consumes 10-20 Å silicon surface and thus, hopefully any high concentration phosphorus on the wafer surface as suggested in Ref. 19. After reloading, the same *in situ* cleaning and 700°C undoped epitaxy was performed. SIMS measurements show that in the upper undoped silicon layer, the phosphorus concentration is now successfully lowered to 10^{17} cm^{-3} in sample D with a sharp transition (Fig. 5). Thus, we conclude that removal of 10-20 Å silicon surface is effective in bringing down the background doping at a rate of 20 nm/decade. The phosphorus spike is induced by the oxygen contamination at the interrupt interface due to insufficient *in situ* cleaning after growth interruption.

To investigate the role of the sacrificial wafer in changing the background doping in the growth chamber, sample E was grown the same way as sample D, except that no sacrificial wafer was grown during the growth interruption and that the chemical oxidation/etching step was repeated five times. The phosphorus doping profile is shown in Fig. 6. Although the doping density drops at 17 nm/decade from 3×10^{18} cm^{-3}, the doping level in the upper Si layer is till above 5×10^{17} cm^{-3}. The results from sample C, D, and E indicate that in order to achieve sharp phosphorus doping profile and low doping density in the following epi layers, both sacrificial wafer growth to reduce the background doping in the growth chamber and removal of 10-50 Å silicon surface are important. Combining these two methods of surface etching and a sacrificial wafer growth, the result of sample F is given in Fig. 6 along with the continuously grown sample A for comparison. After reloading the wafer before further growth, the sample was cleaned at 800°C at 10 Torr in 3 Lpm hydrogen for 90 s. It has been reported that this low temperature cleaning procedure before regrowth leads to an impurity-free interface.[40] As shown in Fig. 6, the phosphorus trailing edge of sample F

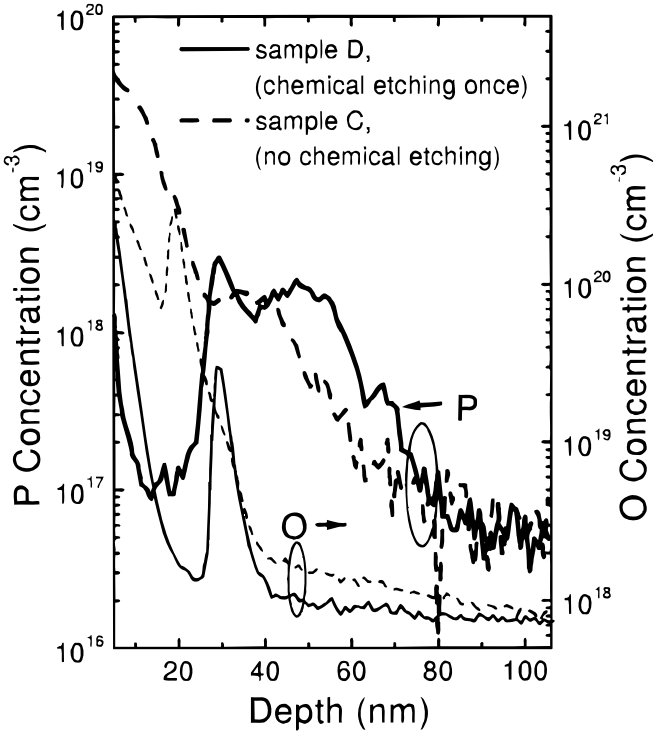

Figure 5. Phosphorus profiles (by SIMS) from sample C (without chemical etching) and sample D (with chemical etching) to demonstrate the effect of *ex situ* etching. During the growth interruption, a sacrificial wafer was grown in the reactor in both cases.

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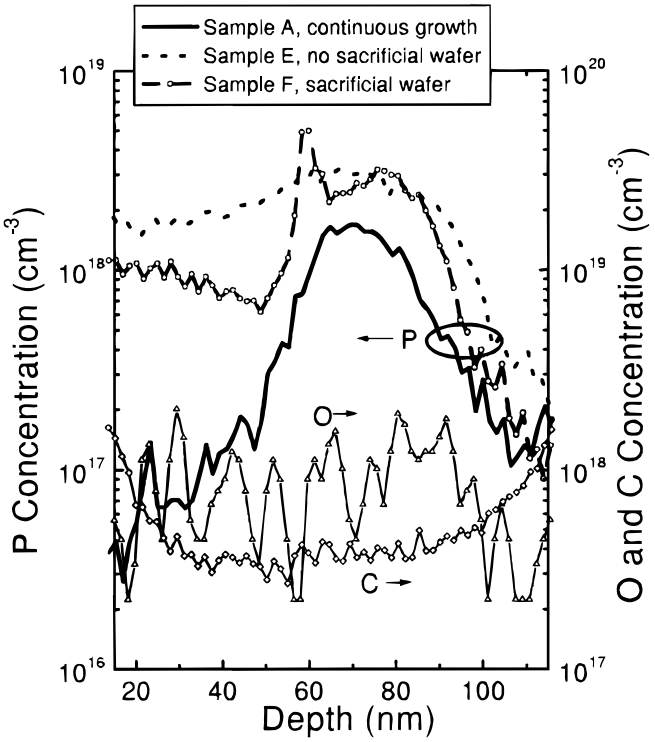

Figure 6. Phosphorus profiles (by SIMS) from sample E (without sacrificial wafer growth) and Sample F (with a sacrificial wafer growth) with *ex situ* etching of both of the wafer surfaces. Phosphorus profile from the continuously grown sample A is replotted for reference. Oxygen and carbon profiles of sample F are also plotted. Note the *in situ* clean before regrowth is longer for sample F than that for sample C, D, and E.

is now 13 nm/decade *vs*. 155 nm/decade in sample A. The doping level in the upper silicon layer is as low as 5×10^{16} cm^{-3}. At the interrupted interface, no oxygen or carbon spikes are observed by SIMS. Note that this cleaning process has a thermal budget which is low enough to avoid any excessive diffusion of the existing dopant profiles, as can be seen by the similar transition rates of the lower phosphorus interface in all samples. This method allows us to realize devices such as sub-100 nm vertical metal oxide semiconductor field effect transistors, where very tight control of the phosphorus profile is required, without any excess leakage associated with a contaminated interface.[41]

Summary

In situ phosphorus doping in Si (700-1000°C) and SiGe (625°C) alloys grown by RTCVD have been studied using dichlorosilane as the silicon source. Increasing phosphine flow leads to a decreasing growth rate and saturation of phosphorus level in silicon layers. Significant background doping and slow transition are also observed in silicon, while higher doping levels and sharper transitions are possible in SiGe. Ultrasharp phosphorus profiles have been achieved by removing the phosphorus from both the wafer surface and the reactor chamber after n^+ epitaxy. Using an *ex situ* chemical etching of 10-50 Å silicon surface, a sacrificial wafer growth, and a maximum temperature of 800°C *in situ* cleaning, a phosphorus doping profile of 13 nm/decade has been demonstrated for silicon layers grown at 700°C, without oxygen and carbon contamination. Such a capability will be useful in the growth of device profiles.

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References

1. B. S. Meyerson, F. K. LeGoues, T. N. Nguyen, and D. L. Harame, *Appl. Phys. Lett.*, **50**, 113 (1987).
2. P. J. Roksnoer, J. W. F. M. Maes, A. T. Vink, C. J. Vriezema, and P. C. Zalm, *Appl. Phys. Lett.*, **58**, 711 (1991).
3. D. W. Greve, *Mater. Sci. Eng.*, **B18**, 22 (1993).
4. B. S. Meyerson and M. L. Yu, *J. Electrochem. Soc.*, **131**, 2366 (1984).
5. D. W. Greve and M. Racanelli, *J. Electrochem. Soc.*, **138**, 1744 (1991).
6. L. D. Madsen and L. Weaver, *J. Electrochem. Soc.*, **137**, 2246 (1990).
7. H. Kurokawa, *J. Electrochem. Soc.*, **129**, 2620 (1982).
8. J. H. Comfort and R. Reif, *J. Appl. Phys.*, **65**, 1053 (1989).
9. A. J. Learn and D. W. Foster, *J. Appl. Phys.*, **61**, 1898 (1987).
10. W. Ahmed and D. B. Meakin, *J. Cryst. Growth*, **79**, 394 (1986).
11. L. P. Chen, G. W. Huang, and C. Y. Chang, *Appl. Phys. Lett.*, **68**, 1498 (1996).
12. T. O. Sedgwick, P. D. Agnello, D. N. Ngoc, T. S. Kuan, and G. Scilla, *Appl. Phys. Lett.*, **58**, 1896 (1991).
13. P. D. Agnello, T. O. Sedgwick, M. S. Goorsky, and J. Cotte, *Appl. Phys. Lett.*, **60**, 454 (1992).
14. T. Y. Hseih, H. G. Chun, and D. L. Kwong, *Appl. Phys. Lett.*, **55**, 2408 (1989).
15. Y. Ohshita and H. Kitajima, *J. Appl. Phys.*, **70**, 1871 (1991).
16. T. I. Kamins and D. Lefforge, *J. Electrochem. Soc.*, **144**, 674 (1997).
17. A. C. Churchill, D. J. Robbins, D. J. Wallis, N. Griffin, D. J. Paul, and A. J. Pidduck, *Semicond. Sci. Technol.*, **12**, 943 (1997).
18. B. Tillack, D. Krüger, P. Gaworzewski, and G. Ritter, *Thin Solid Films*, **294**, 15 (1997).
19. K. Ismail, S. Rishton, J. O. Chu, K. Chan, and B. S. Meyerson, *IEEE Electron Device Lett.*, **14**, 348 (1993).
20. J. O. Chu, K. Ismail, and S. Koester, in *Proceedings of the 40th Electronic Materials Conference*, Virginia (1998).
21. J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, *J. Vac. Sci. Technol. B*, **9**, 2011 (1991).
22. B. S. Meyerson and W. Olbricht, *J. Electrochem. Soc.*, **131**, 2361 (1984).
23. F. C. Eversteyn and B. H. Put, *J. Electrochem. Soc.*, **120**, 106 (1973).
24. J. A. del Alamo and R. M. Swanson, *J. Electrochem. Soc.*, **132**, 3011 (1985).
25. S. M. Jang, K. Liao, and R. Reif, *Appl. Phys. Lett.*, **63**, 1675 (1993).
26. A. Baudrant and M. Sacalotti, *J. Electrochem. Soc.*, **129**, 1109 (1982).
27. M. L. Hitchman and W. Ahmed, *Vacuum*, **34**, 979 (1984).
28. R. F. C. Farrow, *J. Electrochem. Soc.*, **121**, 899 (1974).
29. C. A. Chang, *J. Electrochem. Soc.*, **123**, 1245 (1976).
30. R. Malik, E. Gulari, P. Bhattacharya, K. K. Linder, and J. S. Rieh, *Appl. Phys. Lett.*, **70**, 1149 (1997).
31. N. Maity, L. Q. Xia, and J. R. Engstron, *Appl. Phys. Lett.*, **66**, 1909 (1995).
32. Y. Wang, X. Chen, and R. J. Hamers, *Phys. Rev. B*, **50**, 4534 (1994).
33. J. Bloem, *J. Cryst. Growth*, **31**, 256 (1975).
34. J. Bloem, L. J. Giling, and M. W. M. Graef, *J. Electrochem. Soc.*, **121**, 1354 (1974).
35. R. Reif, *J. Electrochem. Soc.*, **129**, 1122 (1982).
36. M. L. Yu, D. J. Vitkavage, and B. S. Meyerson, *J. Appl. Phys.*, **59**, 4032 (1986).
37. P. M. Garone, J. C. Sturm, P. V. Schwartz, S. A. Schwarz, and B. J. Wilkens, *Appl. Phys. Lett.*, **56**, 1275 (1990).
38. R. Bashir, A. E. Kabir, and P. Westrom, *Appl. Phys. Lett.*, **75**, 796 (1999).
39. K. Ismail, J. O. Chu, K. L. Saenger, and B. S. Meyerson, *Appl. Phys. Lett.*, **65**, 1248 (1994).
40. M. Carroll, M. Yang, and J. C. Sturm, Abstract 523, The Electrochemical Society Meeting Abstracts, Vol. 99-1, Seattle, WA, May 2-6, 1999.
41. M. Yang, C. Chang, M. Carroll, and J. C. Sturm, *IEEE Electron. Device Lett.*, **20**, 301 (1999).